PROCEEDINGS OF SCIENCE

The ALICE Pixel Sensor Upgrade

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The inner tracking system (ITS2) of the ALICE experiment is foreseen to be upgraded during the Long Shutdown 3 of the Large Hadron Collider (LHC). First data are expected to be taken during Run 4 with the upgraded High-Luminosity LHC. The planned ITS3 detector will be based on stitched, wafer-scale Monolithic Active Pixel Sensors (MAPS), bent to radii of 18, 24, and 30 mm and fabricated on 300 mm wafers in a 65 nm CMOS Imaging technology. They will be thinned down to below 50 µm and held in place by carbon foam spacers, resulting in an unprecedented material budget of O(0.05%) X/X_0 per layer. This contribution will present the detector concept, summarise the results of the R&D program, including most recent 65 nm prototypes, and provide an outlook on the path towards the final sensor development.

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1. Introduction

The current Inner Tracker System (ITS2) of the ALICE experiment at the LHC consists of seven layers of MAPS [1]. Each layer consists of ALPIDE chips [2], manufactured in a 180 nm CMOS Imaging technology, and additional components for cooling, data, power and mechanical support. For the inner layers of the ITS2 the actual silicon sensors make up only about 14% of the total material budget, as shown in Fig. 1. The ITS3 project of the ALICE collaboration [3] aims to upgrade the current inner tracking system by replacing the innermost layers with a new detector featuring wafer-scale, bent MAPS. The upgrade foresees to remove cooling components, flexible circuit boards and minimise mechanical support structures. This would provide a significant reduction of the material budget from 0.35% X/X_0 down to below 0.05% X/X_0 and leaves essentially only the silicon itself in the active volume. In addition, the distance to the interaction point will be reduced from currently 23 mm to 18 mm. This requires the beam pipe to be replaced. The tracking and vertexing performance are expected to be enhanced significantly. As can be seen in Fig. 2, the tracking efficiency would improve significantly, especially in the low transverse momentum region, and the pointing resolution would increase by a factor of 2 across the full range of interest of transverse momentum.

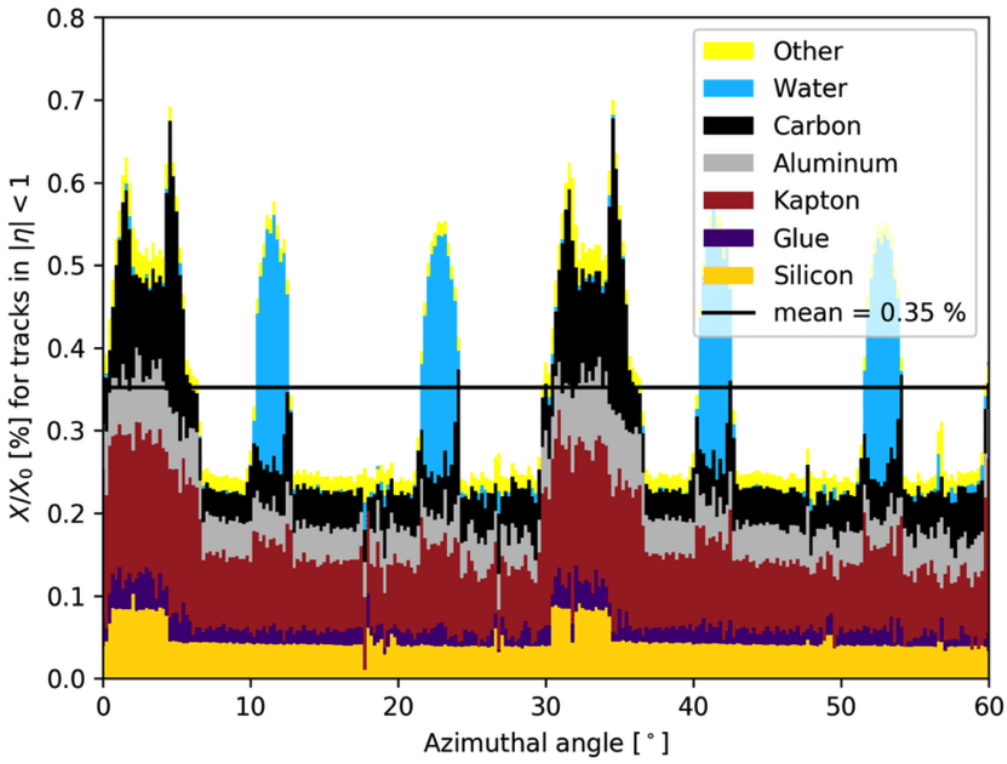

Figure 1: Material budget of the innermost layer of ITS2. The silicon sensor itself makes up only one seventh of the total material (orange). Taken from [3].

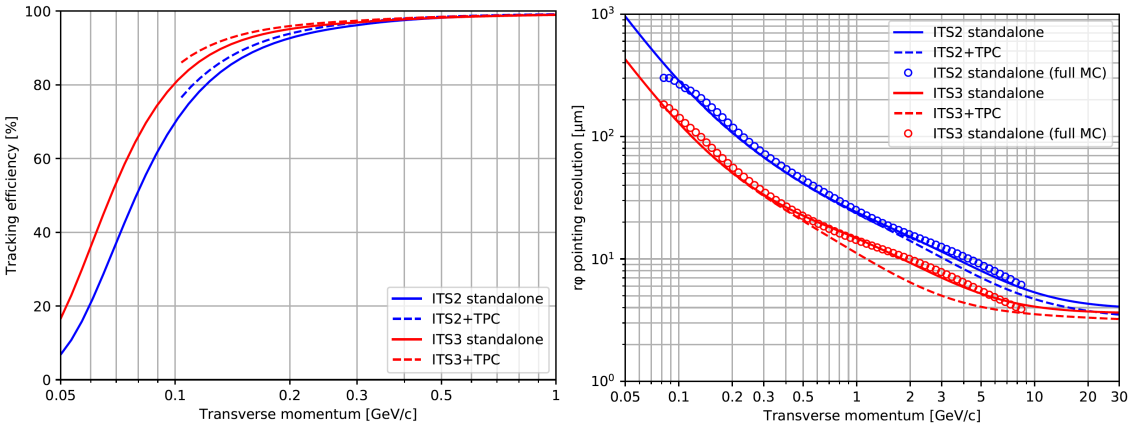

Figure 2: Track finding efficiency (left) and pointing resolution in rφ (right) as a function of transverse momentum. Taken from [3].

2. Detector concept and layout

The new vertex detector will be composed of three layers with radii of 18, 24 and 30 mm with each individual layer consisting of two bent half-cylinders. A CAD drawing of the layout of one half cylinder is shown in Fig. 3. For this purpose new wafer-scale sensors are developed and manufactured in the Tower Semiconductor 65 nm CMOS Imaging process [4, 5]. To reach wafer-sized sensors the project foresees to employ stitching technology [6, 7]. In this photolithographic process multiple design structures are stitched together on silicon wafers. This procedure overcomes limitations of the wafer steppers that make exposures in a relatively small area of a wafer and enables manufacturing of die sizes up to the wafer dimensions.

These sensors will be thinned down to 50 µm or less to allow for the bending of silicon. The final sensor needs to reach a length of 27 cm along the z-axis and more than 9 cm in the azimuthal direction. The new sensor with lower power density will allow to move away from the water cooling used in the current Inner Barrel of the ITS2 to a purely air cooled detector. The mechanical stability will be provided by the bending of the silicon and carbon-foam support structures. These structures are made from two different kinds of ultra-light weight carbon foam. Longerons along the z-axis of each half cylinder are made up of very low density and low thermal conductivity foam, whereas rings at the endcap interfacing the flexible printed circuit boards and airflow guides consist of higher density but highly thermally conductive carbon foam.

3. Bent sensors and mechanical integration

The operation of a bent sensor has been proven to be feasible [8]. Readily available ALPIDE sensors bent to the different ITS3 target radii have been operated in different laboratory setups and test beams. These tests have confirmed experimentally that a high detection efficiency is maintained over a wide operating range when the sensors are bent. An example of one of the more complex test beam setups is pictured in Fig. 4. Silicon dummy chips that were cut from real, but unprocessed, 300 mm wafers and thinned down to 50 µm or below are now routinely bent and used in mechanical prototypes and engineering models. These models address questions in regards to the mechanical

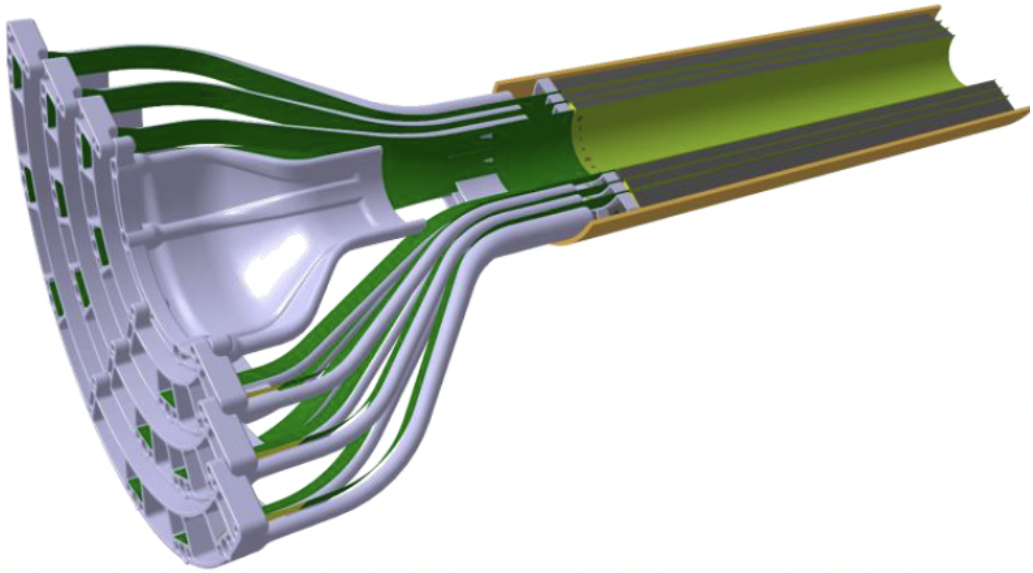

Figure 3: Layout of one half of ITS3. The detector will consists of 6 sensors in total (3 layers, 2 sensors per layer).

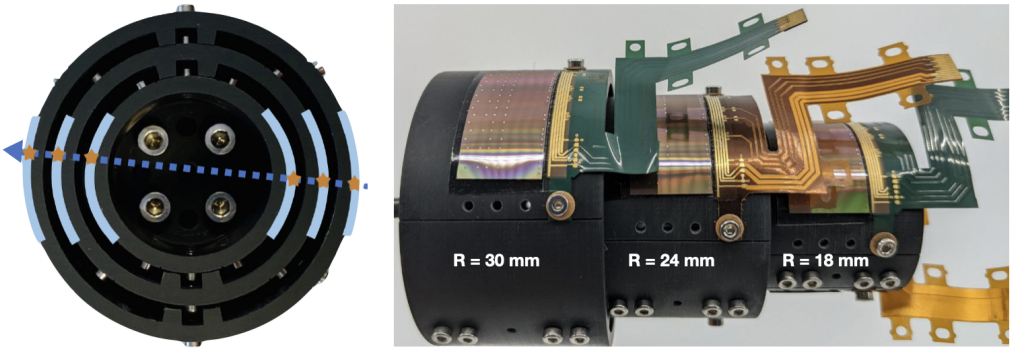

Figure 4: Views of a test beam setup with six bent ALPIDE sensors bent to the ITS3 target radii.

integration. One such mechanical integration prototype of a ITS3 half barrel can be seen in Fig. 5. Setups featuring small sensor prototypes manufactured in 65 nm CMOS Imaging processes are constructed and under study.

4. Sensor prototype characterization

For the ITS3 new wafer-scale sensors are being developed. Before full size prototypes are manufactured, radiation test structures, analog building blocks and fully functional pixel matrices with different front end designs and pixel pitches are designed and validated. The most complex of these small scale structures is the digital pixel test structure (DPTS), measuring 1.5 mm × 1.5 mm and featuring a matrix of 32×32 pixels with a pixel pitch of 15 µm × 15 µm. The DPTS is characterized in test beam and laboratory setups [9]. Results on the efficiency and the fake-hit

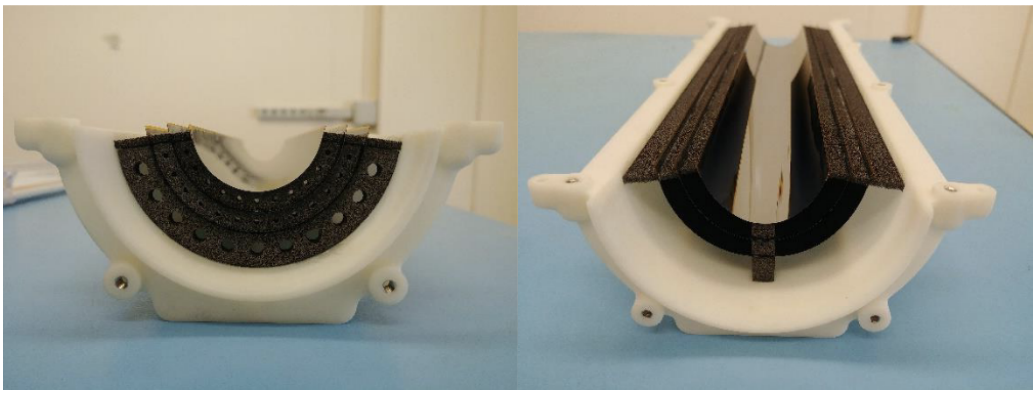

Figure 5: Views of a mechanical integration prototype of a half barrel of the ITS3.

rate (FHR) for different irradiation levels obtained in test beam campaigns with 10 GeV/c positive hadrons are presented in Fig. 6. The FHR is defined as the number of hits per pixel per second without any external stimuli as the chip operates in a continuous readout. With the exception of two sensors the detection efficiency stays above 99% up to a threshold of about 150 e^- and the FHR starts increasing substantially at thresholds below around 100 e^-. The two sensors not following these trends are consistent with the expectation that the largest effect of the non-ionising and ionising radiation damage is on the charge collection and the noise (front-end) performance, respectively. Although the 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor shows notable performance deterioration, it can still be operated at 99% efficiency at the temperature of +20 °C.

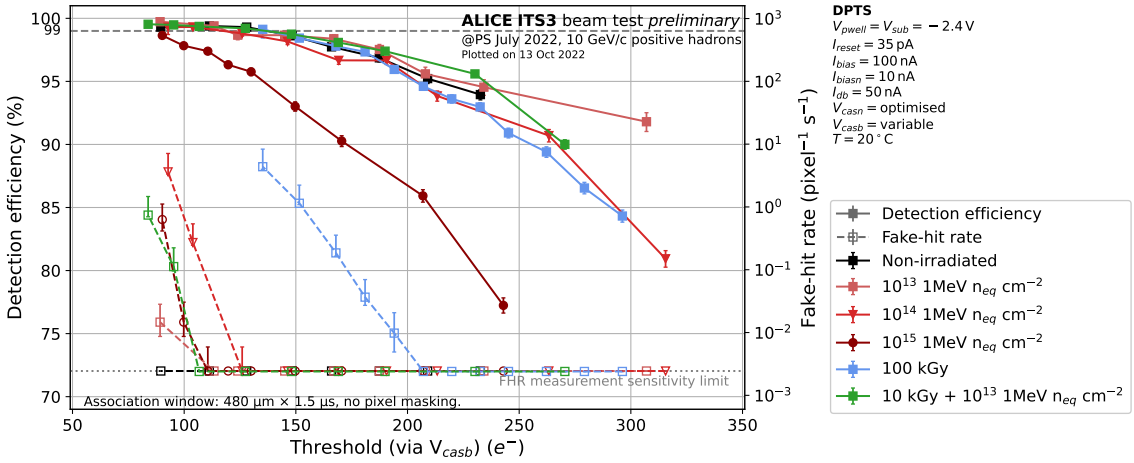

Figure 6: Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) of the DPTS at +20 °C for different irradiation levels as a function of average threshold. Taken from [9].

5. Summary

The ITS3 R&D program has already passed important milestones. The feasibility of bent MAPS and the assembly and integration of wafer-scale, bent thin silicon layers has been proven. Prototype sensors in 65 nm technology are being characterized and important performance aspects

have been validated. Next the ITS3 R&D will move to wafer-scale stitched sensor prototypes which were already taped out at the end of 2022.

Acknowledgments

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