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BOSS :

BEAM OFFSET SIGNAL SUPPRESSOR FOR THE BOOSTER TRANSVERSE FEEDBACK

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The transverse feedback of the Booster consists of several modules. One of the modules is the BOSS, which derives delta - signals from an electrostatic PU. These signals consist partly of transverse instability signals and partly of common mode signals arising from the closed orbit beam position. The BOSS detects any variations in the slowly changing beam position during a cycle and by feedback suppresses the closed orbit signal from the spectrum, thus avoiding saturation of the rest of the transversal feedback system, when the beam is off centre. The fast changing instability signals are passed unhindered through to the rest of the chain.
Due to the continuos increasing intensity in the Booster over the last 20 years, and a demand for higher bandwidth, lower noise and better suppression, the BOSS was developed and installed to replace the original module with similar function, named the COS.

Geneva, Switzerland
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1 The BOSS in the transverse feedback system.

The purpose of the transverse feedback (TFB) system is to damp coherent transverse oscillations. This is done by detecting the beam position at one position in the ring and by deflecting the beam an odd number of ¼ betatron periods later. A block diagram of the system is seen in fig. 1.

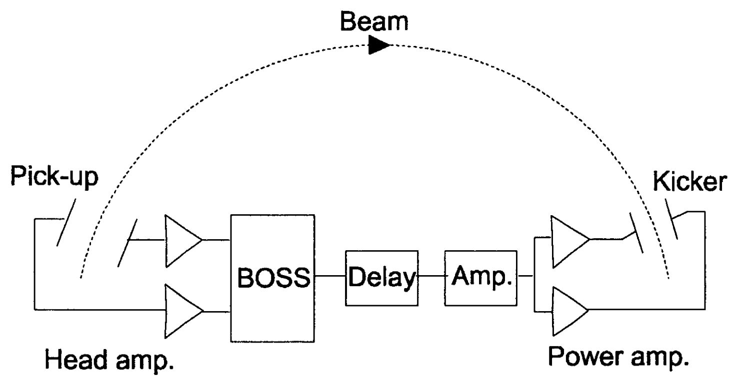

Figure 1. The transverse feedback system.

The purpose of the BOSS is to suppress (attenuate) any signals arising from the closed orbit (changing slowly) and to amplify the fast changing signals from the transverse instabilities. This means, for the perfect BOSS, that there will be no output if the beam displacements are slow, the Beam Offset Signal is fully suppressed, but a signal arising from fast position change (instability) must be amplified and fed back onto the beam with the correct phase. The beam offset signal suppression is therefore one of the main parameters for the BOSS and it is defined in [1].

$$S_{\text{suppression}} = \frac{A_{diff} \cdot V_{diff\ in}}{V_{out}} \qquad [1]$$

The PUs which are used in the Booster TFB have a half aperture of 70mm and when the beam is off centre by ~ 30% (20mm), the output of the PU for a beam of $8 \cdot 10^{12}$ Protons will be 2.5V on one PU electrode and 1.4V on the other. With a differential gain in the TFB system of ~ 80dB, 1 MW power amplifiers would be needed without suppression of the position signal. The present power amplifiers are 100W and are far from being saturated thanks to the effectiveness of the BOSS.

The BOSS also provides a part of the necessary gain needed in the TFB system. Low noise is important as well as linear phase up to 100MHz. More detailed circuit data is given in table 2.

2 Circuit description

A block diagram of the BOSS is shown in fig. 2. It is based on a principle developed by C. Christiansen[1]. From the two input signals (e_1, e_2) a Δ- and a Σ-signal are generated. Multiplying the saturated sum signal with the output from the differential amplifier makes a synchronous detector. i.e. one gets a DC and the double bunch repetition frequency. The dc component of the multiplier output signal, is proportional to the amplitude of the bunch repetition frequency (beam position signal/common mode) and after low pass filtering it is used to control the gain of the two input amplifiers. The feedback is made to minimise the amount of bunch repetition frequency out of the BOSS, and such that it can only follow "slow" changes in the input difference signal. The reason to use a saturated sum signal (square wave) is to minimise the loop gain dependency on beam intensity.

2.1 The suppression

The suppression can be limited by at least three things: The total transfer function [2]; the common mode rejection ratio (CMRR) of the difference amplifier and time delay differences in the input lines before the difference amplifier. The resulting suppression of the system will depend on all three factors.

2.1.1 The transfer function

An approximation of the lower part of the differential frequency response [2] and time response [3] of the system are given by:

- The forward gain $\mathbf{A_{diff}}$.
- The attenuation in the FET attenuators when the beam is in the centre: $\alpha_{FET\text{-}1.5V}$.
- The change in attenuation for a change in the feedback voltage: $\alpha_{\Delta FET}$.
- The gain in the feedback: β.
- The 3dB cut off frequency of the lowpass filter: ω_0.

The high end of the frequency band is flat up to about 100MHz and is not taken into account in the transfer function.

The frequency (<10MHz) response is given by:

$$H_{LF}(s) = \frac{V_{out}}{e_2 - e_1} = \alpha_{FET-1.5V} \cdot A_{diff} \cdot \frac{s + \omega_o}{s + (1 + \frac{1}{3}|e_1 + e_2| \cdot \alpha_{\Delta FET} \cdot \beta \cdot A_{diff}) \cdot \omega_o} \quad [2]$$

Where e_1 and e_2 are the input voltages from the head amplifiers (no DC). The factor $1/3|e_1+e_2|$ is the product of the saturated sum signal and a sum signal.

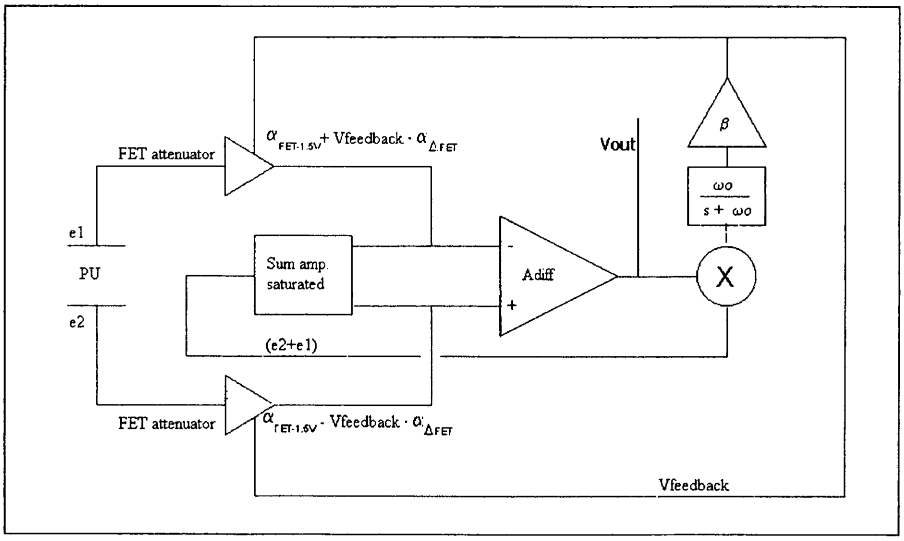

Fig. 2: Circuit block diagram.

[1] A frequency-selective self balancing bridge CERN/PS/B/80-6

The transfer function [2] has in this approximation one zero and one pole frequency. The zero frequency is given by the 3dB frequency of the low pass filter. The pole frequency is the 3dB frequency of the low pass filter multiplied by a *factor*. Assuming this *factor* to be bigger than 1, the function is a high pass function, which will let the fast beam movements through while suppressing the slow ones.
The transfer function for the differential signals has two fixed points: the gain in the pass band and the zero frequency given by the 3dB cut off frequency of the low pas filter. This can be seen in fig. 3, where the response is plotted for different *factors* i.e. the value of the bracket in the denominator of [2].

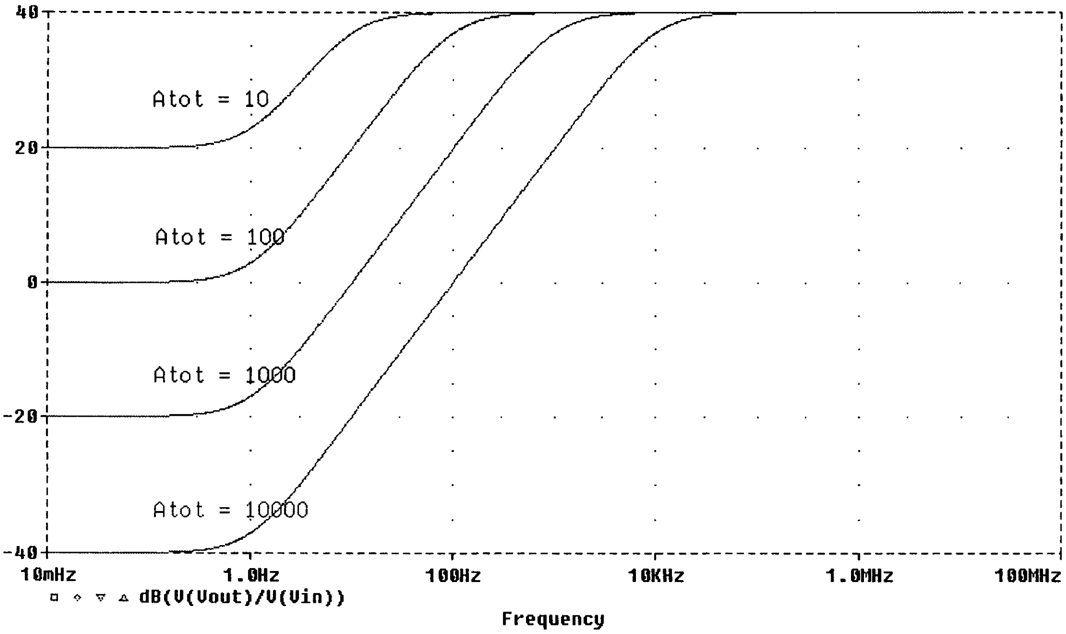

Figure 3: The frequency response for different gains.

The suppression is the difference between passband gain and stopband gain. With the system approximation being of first order, the slope between the zero and the pole frequency is 20dB/decade. The fact that the value | e2 + el | is in the transfer function, means that when the beam intensity decreases, the suppression will also decrease. But since the decrease in suppression is proportional to the decrease in beam intensity, the output level from the stopband will not increase. The pole frequency must be designed such that, at max. intensity it will not influence low frequency cut off of the transverse feedback system.

2.1.2 The CMRR

The feedback will only make the signals on the input of the difference amplifier equal in amplitude. If the common mode rejection ratio (CMRR) of the difference amplifier is not big enough it will limit the suppression. The CMRR must be high in the frequency range used. The range is given by the RF i.e. the number of bunches, the particle speed and the speed change for the particles during acceleration (PSB $\beta_{injection} \approx 0.05$, $\beta_{ejection} \approx 0.8$).

2.1.3 Delay difference

Phase and delay errors in the input cables between the PU and the difference amplifier will limit the suppression. Looking at the subtraction of two sine waves with equal amplitudes but with a phase difference φ:

$$S = \sin(\omega_b \cdot t) - \sin(\omega_b \cdot t - \varphi)$$
$$\Downarrow \text{ at } t = 0$$
$$S_{peak} = \sin(\varphi)$$

With t = 0 the difference between the two sine waves are max. (the peak amplitude).
This means that with a phase difference the signal can't be suppressed to less than sin(φ) of its peak.

A difference in delay t_d will cause phase error:

$$\varphi = t_d \cdot \omega_b \qquad [RAD]$$

This gives with the max. frequency (ω_b) of the PS Booster of 2·π· 1.7MHz · harmonic number, h (We have h = 2) = 2·π· 3.4 MHz the following max. suppression of 1st harmonic.

t_d [Sec]	φ [RAD / °]	S_{factor} [times]	S_{factor} [dB]
4.7 nS	0.1 / 5.74	0.1	20
470 pS	0.01 / 0.573	0.01	40
47 pS	0.001 / 0.057	0.001	60

Table 1. Delay vs. Suppression at 3.4MHz.

47pS corresponds to approx. 1cm of cable difference. In the Booster transverse feedback, trombones are used to adjust the cable lengths. But also the phase response (group delay) of the attenuators in front of the difference amplifier is very important.

2.2 The step response

The step response [3] for a differential step is approximately (assuming high gain) given by the pole frequency.

$$L^{-1}\left[\frac{1}{s}\cdot\frac{s+\omega_z}{s+\omega_p}\right] =$$

$$e^{-\omega_p \cdot t} + \frac{\omega_z}{\omega_p}(1-e^{-\omega_p \cdot t}) \approx \qquad [3]$$

$$e^{-\omega_p \cdot t} \ |\omega_p >> \omega_z$$

In the Booster BOSS the step response time is made approx. 4mS, this makes the system able to follow slow beam movements, but not the fast ones. The achieved step response is not purely 1st order as predicted here, some ringing does occur.

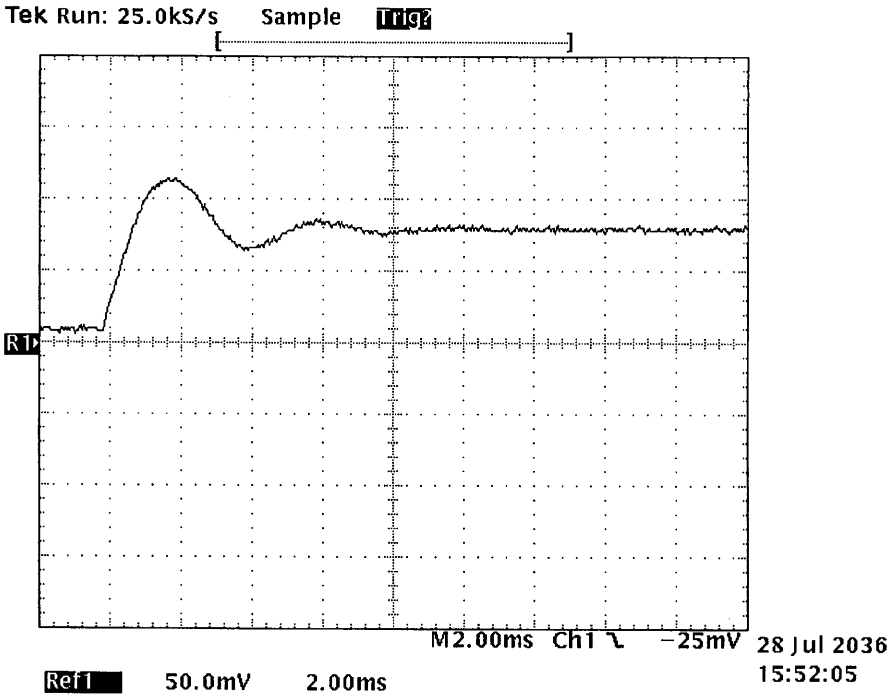

Figure 4. The measured step response

3 Circuit details

The circuit diagram can be seen on page 9, and is described below.

3.1 FET attenuator

The input attenuators are made using a junction FET in its ohmic region. For the equivalent input noise of the system, it is a bad idea to start with an attenuator (in our case of -10dB) and not an amplifier, but the achieved equivalent input noise of 4.5nV/sqrt(Hz) is acceptable.
We have chosen the attenuators since they offer a "gain" change without change of group delay, which is not the case with available variable gain amplifiers.
AC feedback is used on the FET's in order to reduce distortion and the resistor values are chosen to give minimum total attenuation. Each FET has an attenuation range of 8dB to 12dB, this enable a beam displacement of ±20 mm to be accommodated. A variable capacitor is introduced between the input and the gate, giving a variable zero in the frequency characteristic. This is used to minimise the phase/group delay change when changing the attenuation.
To obtain maximum common mode rejection the PCB design of the two input paths is very important. The PCB is made so that the two input attenuators have the same electrical length and parasitic capacities.

3.1 Differential amplifier

The differential amplifier is made as an instrumentation amplifier. This gives identical loading of each FET attenuator, and allows one to add gain before the actual differential amplifier (common mode gain =1), and in this way improve the total CMRR.
The PCB layout of the instrumentation amplifier is also made symmetrical.

3.2 Output amplifiers

The output amplifier is made with Avantek GPD amplifiers, which offer a series of cascadable amplifiers giving the output power of 15dBm needed. After the first amplifier an ohmic splitter is used to provide a feedback signal. This signal is fed back to the multiplier in a 50Ω matched cable, giving the needed delay to match the delay in the sum signal path.

3.3 Sum amplifier

The sum signal is amplified to give a square wave to the input of the multiplier; this is done using a logarithmic amplifier with a limited output, AD606. To avoid spikes on the power supply this device has a separate power supply and the ground plane is separated from the analog ground plane. For the same reason the input level is reduced, otherwise at max. beam intensity the switching can be seen on all analog signals.

3.4 Multiplier

The Multiplier used is an AD834. The current output of this is transformed into a voltage using an operational amplifier. Since the circuit must work down to DC, resistor attenuators inside the feedback loop of the OP-amp are used to suppress the high DC voltage on the AD834 output.
Due to the very high DC gain in the feedback an offset adjustment is introduced in the multiplier network. Any DC offset will be seen by the feedback system as output from the synchronous detector (multiplier) and will limit the suppression.

3.5 Integrator and feedback

Standard integrator coupling is used. The nominal voltage on the FET gates are –1.5Vgiving 10dB of attenuation with a centred beam. This voltage reference is added to the feedback signal by using sum and difference amplifiers in such a way that the two feedback signals are in anti-phase.

4 Circuit data:

Z_{in}	50 Ω
SWR_{in} @ 10MHz	< 1.05
Maximal input level[1]	3 Vpp
Max differential input[2]	4dB
Suppression factor typ. @ 1MHz[3]	60 dB
Differential signal bandwidth 5° linearity error	100KHz – 100 MHz
Differential signal bandwidth 3 dB	1KHz – 80MHz
Gain to OUT1 / OUT2	40dB / 20 dB
Z_{out}	50 Ω
Equivalent input noise per channel	4.5 nV/√Hz
Vout (1dB compression)	15dBm
Step response time[4]	4mS

Table 2: Circuit data.

Note 1:

The maximal input level is given as common mode levels. When looking at the output of the suppressor the 2nd harmonic will increase with increasing input levels. The maximal input level is here given for the value where the 2nd harmonic is as big as the suppressed 1st harmonic.

Note 2:

The attenuators in the input stage will only stay with a constant group delay within a given attenuation range. This means if the beam is too far off centre, delay differences in the attenuators will limit the suppression.

Note 3:

The suppression factor is given by formula [1]. The value here is measured with a 1MHz sine wave on one input of 8dBm and 6dBm on the other, simulating a beam offset. The voltage difference on the inputs is calculated from the power levels. If there were no suppression this voltage would see the full voltage gain of the system. The suppression is here taken to be the difference between the voltage that would have come out with no suppression compared with what does come out.

Note 4:

The step response has some ringing i.e. is not a simple 1st order function. The step response time is given as the time when the response has less then 10% error.

5 Circuit diagram