Serial Powering Scheme and Performance Analysis for Innermost Layer (L0) for ATLAS ITk modules

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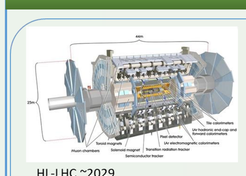
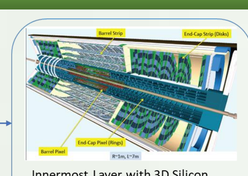
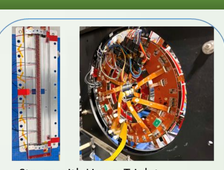
Overview



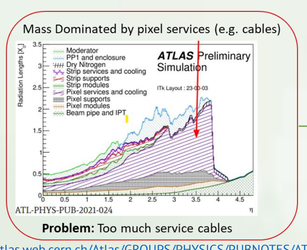
HL-LHC ~2029
Instantaneous Luminosity ~7.5×10^{34} cm^{-2}s^{-1}
@200 Interactions/BC

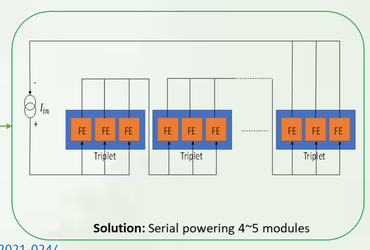


Innermost Layer with 3D Silicon Detectors



Staves with Linear Triplet modules and Rings with Ring Triplet Modules



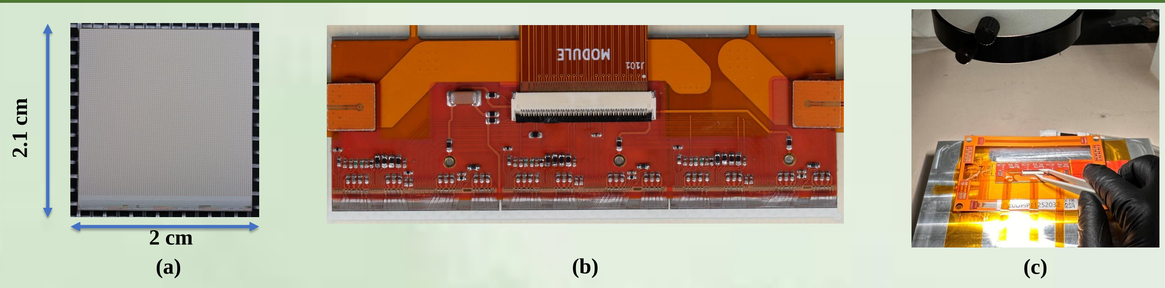


https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PUBNOTES/ATL-PHYS-PUB-2021-024/

After ten years of massive success, the Large Hadron Collider (LHC) at CERN is going for an upgrade to the next phase, the High Luminosity Large Hadron Collider (HL-LHC) which is planned to start its operation in 2029. To withstand projected harsh radiation environment, it was proposed to make the innermost layer [L0] of the new Inner Tracker (ITk) with 3D silicon sensor modules, which will have a radiation tolerance of more than 1×10^{16} n_{eq}/cm^2 with a TID of 9.9 MGy, where each 3D sensor will be bump-bonded to a Front End (FE) chip to form a bare module, and three bare modules will be powered in parallel in a triplet module.

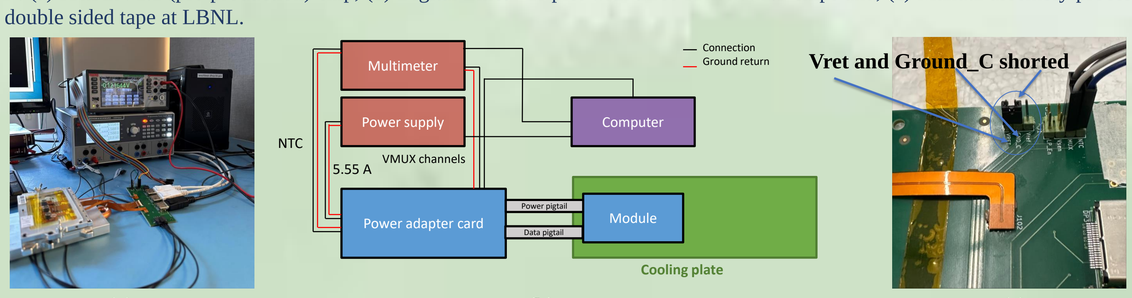
The L0 layer will have 396 triplet modules. To reduce cable material and improve detector performance, 3 to 5 triplets (depending on the location in the detector) will be powered in series. The FE chip implements a number of features (like a shunt-low-dropout regulator and over-voltage and under-shunt protection) needed to guarantee stable operation of the detector with this powering scheme. In this study, we powered in series 4 triplets based on the pre-production ATLAS FE chip for HL-LHC. We ensured that the chosen operational parameters are within our theoretical specs and result in stable operation of the modules within serial power chain. Triplets were also powered in Low Power mode (LP), used to operate the module at lower current, and their performance was tested without cooling requirement. The performance of the under-shunt and over-voltage protection were also analyzed.

Triplet DAQ Setup



(a) (b) (c)

Fig. 1 : (a) ITkPixV1.1 (pre-production) chip, (b) Digital Linear Triplet with three ITkPixV1.1 chips and, (c) Manual assembly process with double sided tape at LBNL.



(a) (b) (c)

Fig. 2: (a) Data acquisition setup for triplet at LBNL with HMP4040 power supply and DMM600 multimeter with ten channel scanner card, (b) Schematic of the DAQ setup, the whole system is automized with the help of LabRemote software and, (c) Grounding scheme to bring both module ground and DAQ ground at the same level.

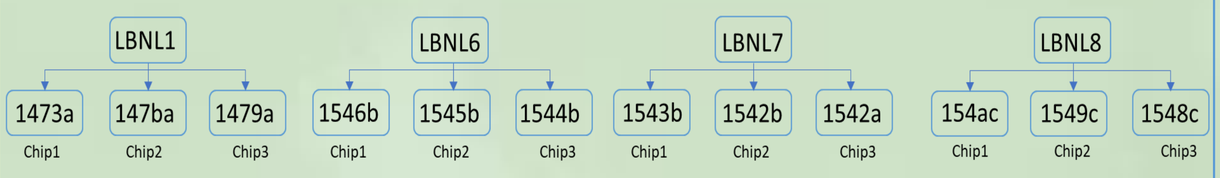
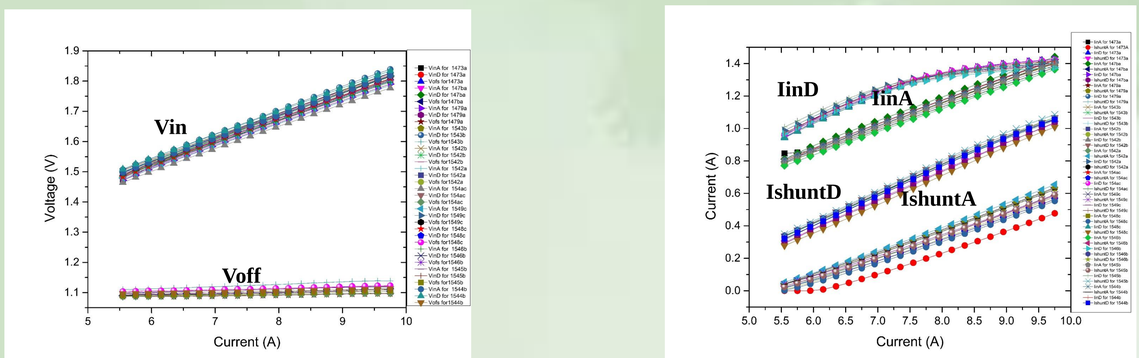


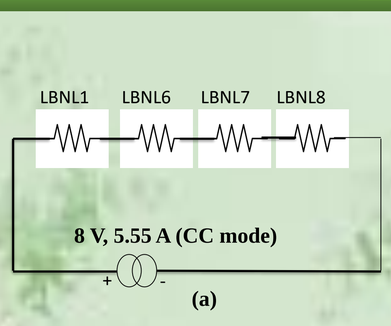
Fig. 3: Triplets used in this study and its component chips. Thes names are given locally, all of them has been assembled at LBNL manually with double sided tape. Chip names are derived from wafer name and position at the wafer.



(a) (b)

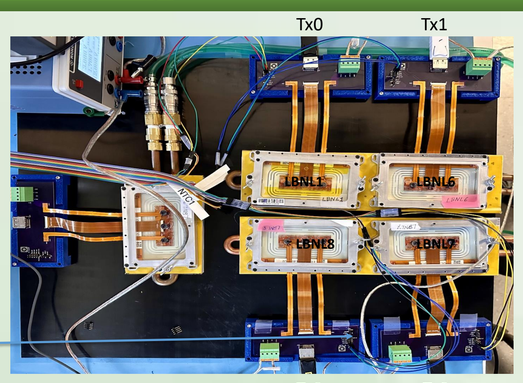
Fig. 4: (a) Digital and Analog Front End (FE) input voltage vs module input current curve for all the chips enlisted at figure 3. Input current was varied from 5.55 A (nominal operational current) upto 9.75 A. Measurements were taken from chip Vmux. All the chips showed same trend and good SLDO characteristics for VinD and VinA. (b) Input and Shunt current (both Digital and Analog FE) vs module input current curve. Trend is similar for almost all the chips, where Digital current is higher than Analog current. Input currents are calculated from the measured voltage from chip Vmux.

Serial Power Chain Setup



(a)

Ground Shorting Jumper to close the loop



(b)

Fig. 5: (a) Schematics of how four triplets are arranged to make a serial power chain. (b) Physical picture of the serial power chain, four triplets are connected with four transmission lines of four channel ohio card, attached with the FPGA. The fifth one is not connected.

LP mode and OVP

(a) (b)

Fig. 6: (a)Front End input voltages vs module input current at Low Power (LP) mode. The module was powered at LP mode, where Voffset is pushed higher by adding a square pulse provided by the FPGA, so that chip can operate minimally at a lower power. The current is varied from 1.8 A upto 10 A, in reverse order, that's why the temperature increased rapidly at high current, and gradually decreased with decrease of current.. From 2 A to 9 A, chip showed a very good linear SLDO behavior. Around 9 A, the input voltages get saturated at 2 V, because the chip has a safety feature called Over Voltage Protection (OVP), which stops chip to have more input voltage then 2 V. As all the chips showed same behavior, only one has been showed here. (b) All the chips in serial power chain have similar effect at LP mode, and the OVP kicked in at around 9 A.

Serial Power Chain Output

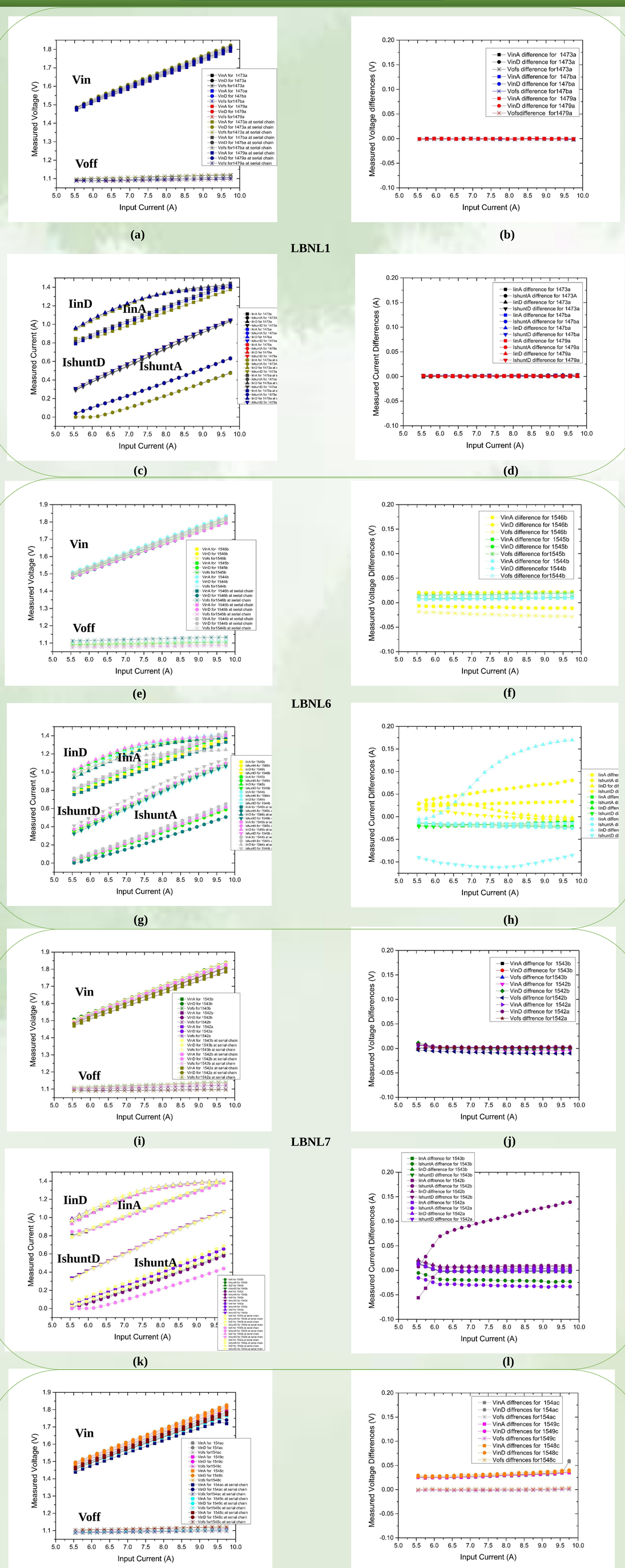


Fig 7: FE input voltages vs module input current (a, e, i, m) of four triplet modules as single module and as a part of serial power chain and the differences between two conditions (b, f, j, n); FE input currents vs module input current (c, g, k ,o) of the same triplets as a single module and as a part of serial power chain and the differences between two conditions (d, h, l, p). The differences for LBNL1, i.e. the first triplet of the chain is negligible. For LBNL6, which is second in the chain is in the range of 20 mV and 200 mA current, and increases with the increase of input current, could be an effect of temperature rise. The differences reduces further for LBNL7 and 8, as the third and fourth triplet of the chain.

Conclusion

Four triplets were connected in serial power chain to estimate the power consumption behavior at the detector. The power consumption at nominal operational conditions are found to be comparable with prediction and the deviation from independent triplet is minimal. The LP mode is also functioning, and the over voltage protection scheme is working as the prediction.

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