

Charge collection and efficiency measurements of the TJ-Monopix2 DMAPS in 180 nm CMOS technology

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Monolithic CMOS pixel detectors have emerged as competitive contenders in the field of high-energy particle physics detectors. The use of commercial processes offers high-volume production of such detectors. A series of prototypes has been designed in a 180 nm Tower CMOS process with depletion of the sensor material and a column-drain readout architecture. The latest iteration, TJ-Monopix2, features a large $2 \times 2 \text{ cm}^2$ matrix consisting of 512×512 pixels with $33.04 \mu\text{m}$ pitch. A small collection electrode design aims at low power consumption and low noise while the radiation tolerance for high-energy particle detector applications needs extra attention. With a goal to reach radiation tolerance to levels of NIEL damage of $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$, a modification of the standard process has been implemented by adding a low-dosed n-type silicon implant across the pixel in order to allow for homogeneous depletion of the sensor volume. Recent lab measurements and beam tests were conducted for unirradiated modules to study electrical characteristics and hit detection efficiency.

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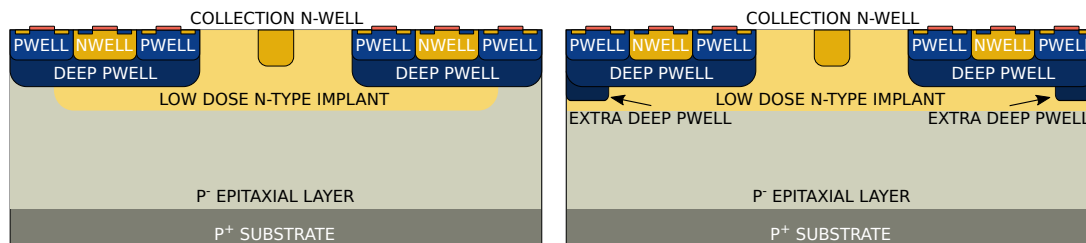
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1. Introduction

In recent years, advances in CMOS technologies have fueled the development of a new generation of monolithic active pixel sensors (MAPS) with fast readout and high radiation tolerance by depleting the charge sensitive volume [1]. These depleted MAPS (DMAPS) devices are therefore an interesting candidate for high-energy particle physics experiments with high radiation environments and high particle rate. Depletion is achieved by either using high-voltage add-ons in the CMOS technology and/or high resistivity substrates. The increasing availability of these features in commercial CMOS processes could combine the features of the detector concept with possibly faster and cheaper production than common hybrid pixel detectors for the mentioned purposes. The idea behind and measurements results from one of multiple DMAPS prototypes, TJ-Monopix2 [2, 3], will be presented in the following.

2. Design of TJ-Monopix2

TJ-Monopix2 is the latest DMAPS prototype from the TJ-Monopix development line which is based on the ALPIDE pixel detector developed for the ALICE ITS upgrade [4]. It is fabricated in the same 180 nm commercial CMOS process provided by Tower Semiconductor¹. A modification of the process used for ALPIDE has been implemented to increase the radiation tolerance to levels $\geq 1 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ by adding a low dose n-type implant for homogeneous growth of the depletion zone with applied bias voltage. In measurements on first prototypes with this modification, a drop in hit detection efficiency was observed after irradiation [5, 6]. This could be improved significantly by adding a gap in the n-type blanket or a deep p-type implant in the pixel corners to shape the electrical field towards the collection electrode [7]. The cross-sections of these two sensor designs is shown in fig. 1. Additionally, chips have been produced on Czochralski



(a) Modification with gap in low dose n-type implant below low pixel electronics. (b) Modification with continuous n-type implant and deep p-type implant below pixel electronics.

Figure 1: Cross-section variants of modified sensor process for TJ-Monopix2.

silicon to increase the available depletable volume compared to the thickness of the epitaxial layer ($O(10 \mu\text{m})$). Measurements on Czochralski silicon chips in TJ-Monopix1 showed a further increase in hit detection efficiency after irradiation [8].

TJ-Monopix2 follows a small collection electrode approach with a pixel capacitance of about 3 fF. The pixels of size $33 \mu\text{m} \times 33 \mu\text{m}$ are read out using an established synchronous column-drain technique from the FE-I3 readout chip [9]. Further changes from the predecessor

¹<https://towersemi.com>

TJ-Monopix1 include an improved front-end design, a new pixel masking scheme and a 3-bit DAC for local threshold tuning. With these changes the threshold is expected to be reduced by a factor of 3 while improving the threshold dispersion and noise behavior.

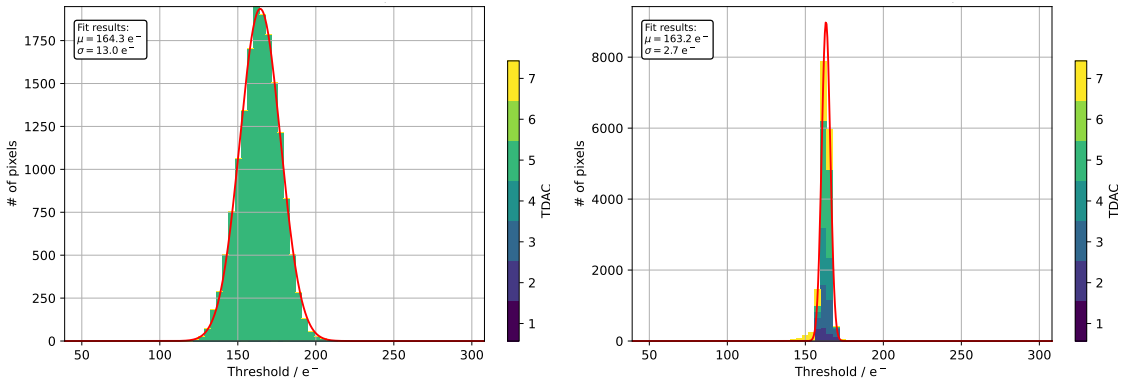
The digital periphery contains logic for register configuration, data handling and LVDS output drivers. Slow control is done via a command protocol and decoder that was taken from the RD53B readout chip [10]. Both pixel and register data is 8b10b encoded in a frame-based data stream which allows operating the chip with four differential data lines.

3. Injection-based threshold and noise measurements

Initial tests have been performed in a laboratory setup to measure the threshold and noise performance of TJ-Monopix2. All of these values are extracted from injecting different amounts of charge into the pixel a given number of times and recording the amount of registered hits n_{hits} . The response function is a smeared step function of the form

$$n_{\text{hits}}(q) = \frac{1}{2} \cdot n_{\text{injections}} \cdot \left(\text{erf} \left(\frac{q - q_{\text{thr}}}{\sigma \sqrt{2}} \right) + 1 \right) \quad (1)$$

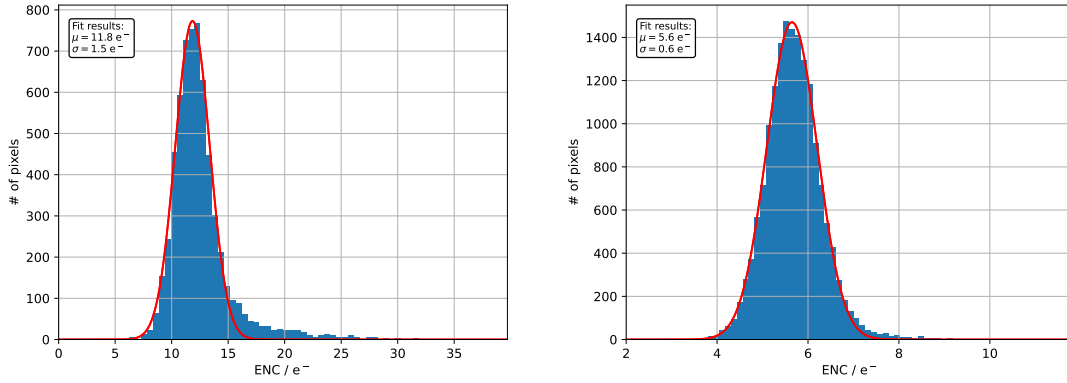
with q the injected charge amount, $n_{\text{injections}}$ the number of consecutive injections of q and q_{thr} the charge at the threshold. σ denotes the gaussian smearing of the step function which is defined as the electronic noise of the pixel. The threshold is defined as the charge at which 50% of the injected hits are recorded from the pixel. Histogramming the individual thresholds from each pixel leads to the distribution shown in fig. 2a. The distribution has a mean value of $164 e^-$ and a width



(a) Threshold distribution before in-pixel threshold tuning. (b) Threshold distribution after in-pixel threshold tuning.

Figure 2: Threshold distribution of TJ-Monopix2 before and after adjusting the in-pixel threshold DAC to lower the dispersion. Color-coded is the value of the DAC setting for every pixel.

of $13 e^-$ which is defined as the threshold dispersion. By adjusting the threshold DAC in each pixel in order to even out the deviations from the target threshold, the threshold dispersion can be reduced significantly. The resulting distribution after this so-called tuning process is shown in fig. 2b. While the mean threshold stays basically the same, the dispersion could be reduced by a factor of almost 5. Both the mean threshold and threshold dispersion are significantly lower than in TJ-Monopix1, where losses in hit detection efficiency could be observed due to too large thresholds [8].



(a) Noise distribution of TJ-Monopix1 with noticeable tail (b) Noise distribution of TJ-Monopix2. There is no observable tail and lower noise overall.

Figure 3: Noise distribution of TJ-Monopix1 (left) and TJ-Monopix2 (right) for comparison.

The corresponding histogram of the electronic noise is depicted in fig. 3. As a comparison, the distribution from the predecessor TJ-Monopix1 is included, where a large tail towards higher values was observed that led to a high operational threshold in order to limit the amount of noisy pixels. It can be seen, that this tail is largely removed with slight changes to the analog front-end, which in turn lowers the threshold for a regular operation of the chip.

4. Hit detection efficiency measurements

Two different pixel variations were investigated regarding their hit detection efficiency, that will be presented in the following – a DC-coupled, more standard design which makes up most part of the matrix and an AC-coupled investigative design realized in only a few columns of the matrix. While the former was measured in more detail, some first results of the latter are included as well.

4.1 Standard DC-coupled pixel flavor

First measurements to determine the hit detection efficiency have been performed in a 5 GeV electron beam at the DESY II testbeam facility at DESY, Hamburg [11]. Three unirradiated modules were tested with different sensor geometries: two chips with 30 μm thick epitaxial silicon and the two geometries depicted in fig. 1 as well as one chip built on 300 μm Czochralski silicon with a gap in the low dose n-type implant (see fig. 1a). It should be noted that the different substrate materials offer different sensor thicknesses and therefore charge-sensitive volume depending on the depletion. The measurements are not targeting a comparison between different types of silicon.

Figures 4a and 4b show the recorded cluster charge for a chip with epitaxial layer and with Czochralski substrate. It can be observed that the collected charge is about 25 % larger in the Cz sample, because the depletion depth is only limited by the thickness of the sensor (300 μm) which is by far not fully depleted, but more depleted than the 30 μm thick epitaxial layer in the other chip.

The average cluster size is significantly larger in the Cz sample as well which results in a high spatial resolution due to charge-weighted clustering. The cluster size distributions for the same samples as above are depicted in figs. 4c and 4d. While cluster size 1 is predominant in the epitaxial

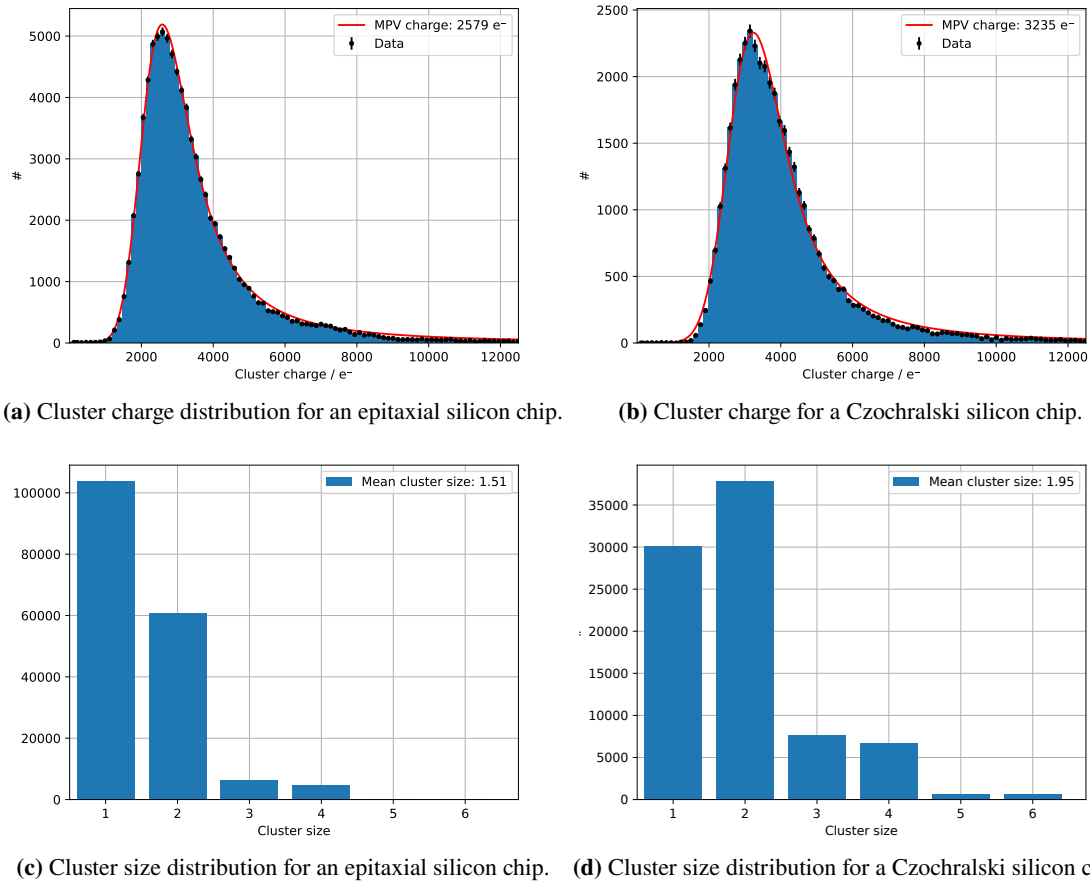


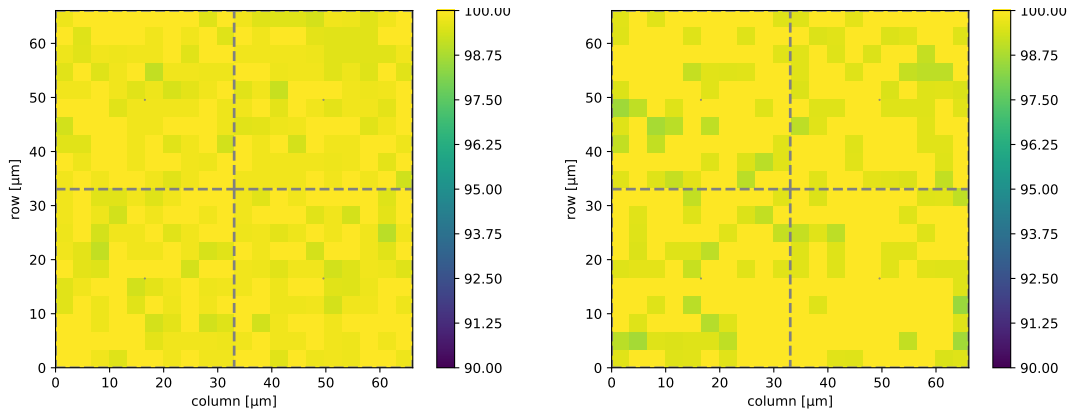
Figure 4: Cluster charge and size distributions for a chip with 30 μm epitaxial silicon (left) and 300 μm Czochralski silicon (right) at -6 V bias voltage. The latter can be depleted further than 30 μm resulting in a larger cluster charge and size. Both chips were operated at a threshold of 200 e⁻.

sample, the Cz sample has mainly clusters of size 2. The corresponding average cluster size is 1.55 and 1.95, respectively. Taking the pointing resolution of the beam telescope into account, an intrinsic spatial resolution of 8.6 μm could be achieved in a Czochralski silicon sample.

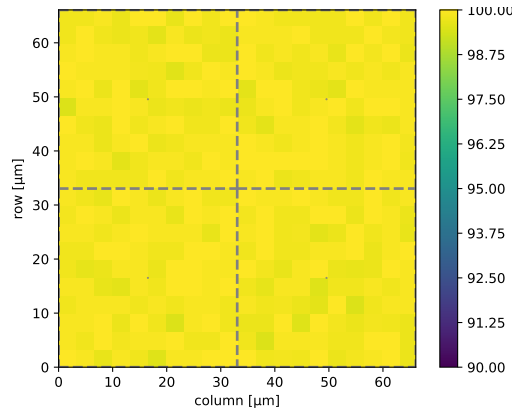
The hit detection efficiency was measured with a beam telescope with six MIMOSA26 planes and a FE-I4 time reference plane which are all connected to a trigger logic unit to synchronize individual detector hits time-wise. The efficiency for all three modules is shown in fig. 5 where the result for every pixel was mapped onto a two by two pixel cell to increase the statistics to see possible effects or efficiency losses within a single pixel. All samples were running at a threshold of about 200 e⁻ and achieve a hit detection efficiency around 99.80 % with slight deviations within the error (estimated < 0.1 %). There are no losses observable in the pixel corners or between pixels.

4.2 AC-coupled pixel flavor

Another pixel variation with different analog front-end was tested as well to determine its performance in a particle beam. In this design the (positive) bias voltage is applied via a diode on the top side of the chip and connected to the charge collection n-well. To avoid breakdown of the front-end electronics due to the high voltage ($\leq 50\text{ V}$) on that well, the input signal is AC coupled to



(a) (99.80 ± 0.10) % efficiency for a chip built on epitaxial silicon with gap in n-layer modification from fig. 1a. (b) (99.79 ± 0.10) % efficiency for a chip built on Czochralski silicon with gap in n-layer modification from fig. 1a.



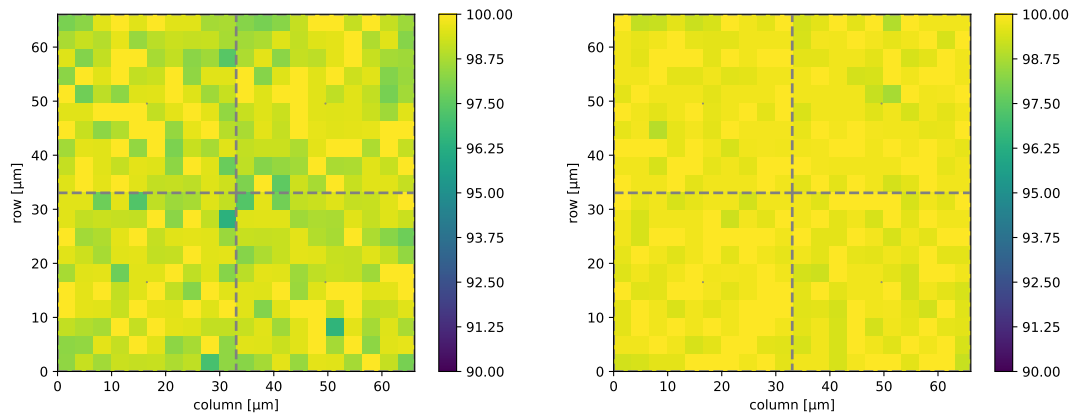
(c) (99.85 ± 0.10) % efficiency for a chip built on epitaxial silicon with additional p-well modification from fig. 1b.

Figure 5: Hit detection efficiencies for different substrate materials with different thicknesses and sensor geometries. Results were mapped onto a 2×2 pixel array for higher statistics and in-pixel resolution. The chips were operated with -6 V bias voltage and at a $200 e^-$ threshold.

the amplifier. This approach can potentially deplete the substrate further due to the higher voltage than what can be applied in the standard pixel design. The hit detection efficiency was measured for different bias voltages and is shown in fig. 6. At 5 V the efficiency is already above 99 % and reaches the same value as for the DC coupled pixel flavor of 99.85 % at or before 25 V bias voltage. This is, taking the slightly higher threshold into account, in agreement with the expectation that there should be no noticeable difference in hit detection efficiency before irradiation between the two pixel flavors. The larger applicable bias voltage could prove superior after irradiation to achieve more depletion and therefore higher charge signal.

5. Conclusion

In summary, the performance of TJ-Monopix2 shows a significant improvement in threshold value and dispersion compared to TJ-Monopix1, although the former is higher than its design value



(a) $(99.21 \pm 0.10)\%$ efficiency of an AC-coupled pixel flavor at 5 V bias voltage and $250 e^-$ threshold. (b) $(99.85 \pm 0.10)\%$ efficiency of an AC-coupled pixel flavor at 25 V bias voltage and $200 e^-$ threshold.

Figure 6: Hit detection efficiency of an AC-coupled pixel flavor at (6a) 5 V and (6b) 25 V bias voltage.

($120 e^-$). With the measured amount of charge in the sensor the threshold is still small enough to detect a majority of hits even from large clusters before irradiation. The large signal compared to the small pixel leads to a large cluster size and therefore high spatial resolution, where chips on Czochralski substrate perform slightly better due to the larger sensor volume. For the tested sensor materials with different thicknesses and sensor geometries, the hit detection efficiency is around 99.8% or better in all cases. The modified front-end version with bias applied on the charge collection node achieves similar values for the hit detection efficiency while providing a larger headroom in bias voltage to achieve efficient performance after radiation damage. The results for irradiated modules will be presented in a forthcoming publication.

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