Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Salvador Ventura Gonzalez
on behalf of the ATLAS Liquid Argon Calorimeter group

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Outline

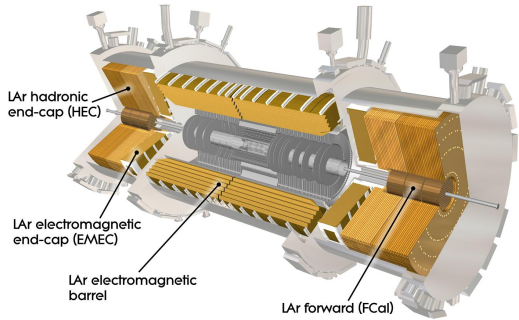
LAr and HL-LHC

Liquid Argon calorimeter

- Detector in the ATLAS experiment at CERN.
- Sampling calorimeter to measure energy deposited by electrons, photons and hadronic jets.
- Liquid Argon as active medium.
- ∼182,500 readout channels.

High Luminosity LHC (HL-LHC)

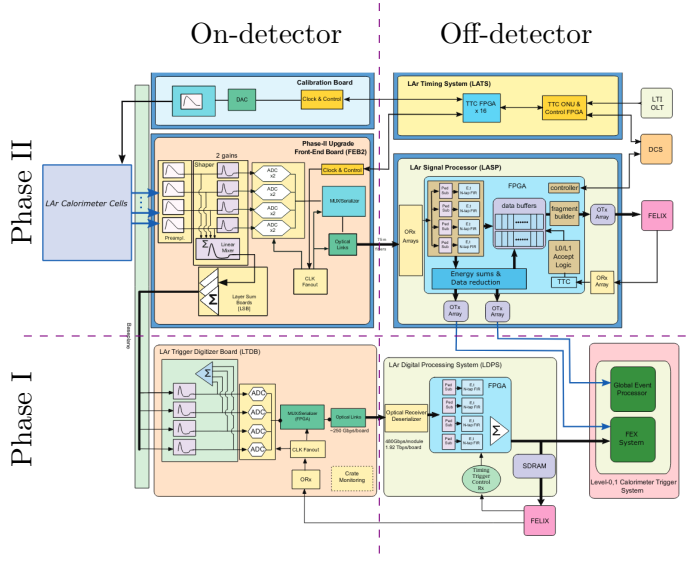
- 5 to 7x the nominal luminosity. Up to 200 collisions per bunch crossing.
- Scheduled to begin in 2029.



LAr read-out electronics for HL-LHC

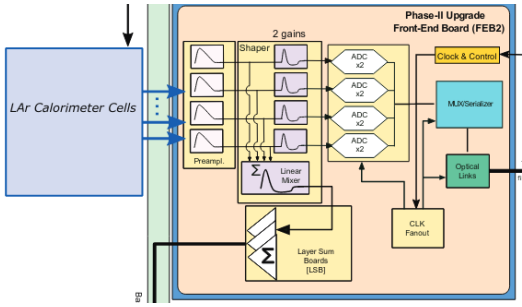
- Under the HL-LHC conditions, the read-out is required to:
  - Provide full LAr data for physics and necessary trigger improvements.
  - Withstand high radiation doses (max. TID ∼1-2 kGy).
- Upgrades in two phases:
  - Phase I (2016-2021):
    Trigger digitization and processing.
    Under final commissioning. See Marin Furukawa's talk.
  - Phase II (2020-2026):
    Calibration, digitization and signal processing for energy reconstruction.
    Under development.

This presentation is focused on Phase-II upgrades



On-detector electronics, **Front End Board (FEB2)**

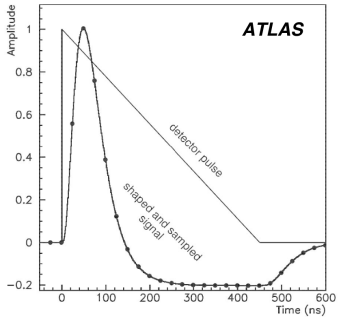
- Shape and digitize signals for both trigger and energy reconstruction.
- Handle the 16-bit dynamic range of calorimeters with two gain scales at 40 MHz.
- Serialize data for the LAr Signal Processor (LASP) board.
- Provide analog signal for Layer Sum Board (LSB).
- Main components: **ALFE** V2 (Pre-amplifier/Shaper), **COLUTA** V4 (ADC), and lpGBT (optical link).
- Must be stable for max irradiation of 1.4 kGy (TID), 4.1x10^{13} n_{eq}/cm^2 (NIEL).

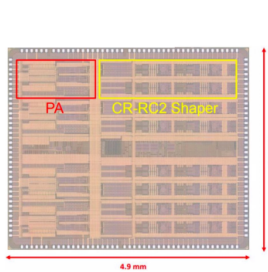


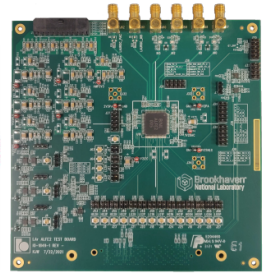
On-detector electronics, **Front End Board (FEB2)**

ALFE2: Preamplifier and Shaper

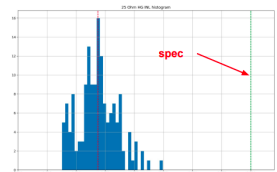
- Custom ASIC in 130 nm CMOS TSMC.
- 16-bit range, gain ratio ∼23.
- CR-RC^2 shaping.
- Differential ouputs for ADC and LSB
- **Key specifications such as INL, ENI and PSRR have been greatly exceeded in latest ALFE2 ASIC.**



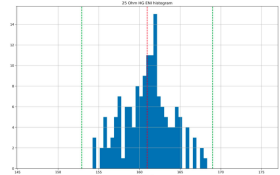




INL



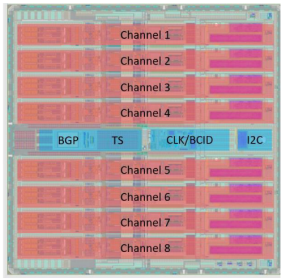
ENI

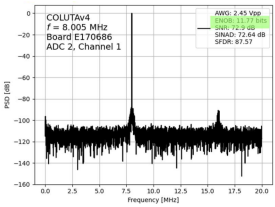


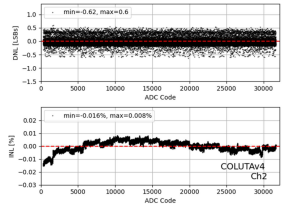
On-detector electronics, **Front End Board (FEB2)**

COLUTA V4 ADC

- 8 channels, 15-bit ADC, 40 MSPS
- 4th version of custom ASIC, 65 nm CMOS technology
- MDAC+SAR+DDPU architecture
- ENOB>11
- **In pre-preduction phase, mass production automated testbenches under development**.

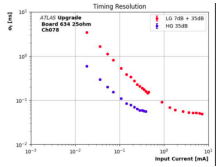


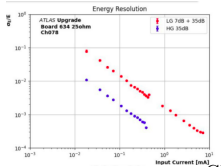




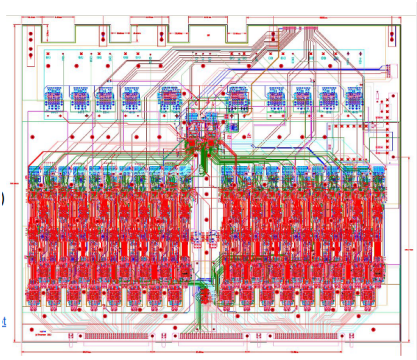
On-detector electronics, **Front End Board (FEB2)**

- Slice testboard
  - **ALFE**, **COLUTA** and optical links integrated.
  - 32 channels.
  - Control and readout on all channels tested.
  - Meet specifications for energy resolution ($\sim$0.02%), and time resolution ($\sim$50 ps for large pulses).



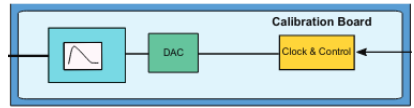


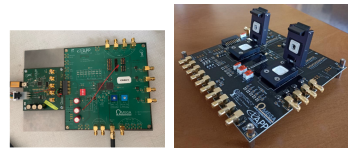
- **FEB2 v1.0 board**
  - 128 channels.
  - **In PCB fabrication step.**

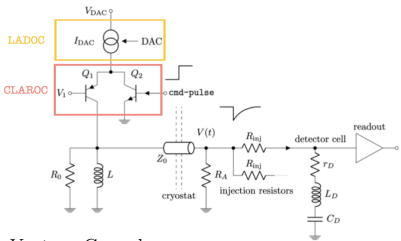


On-detector electronics, **Calibration board**

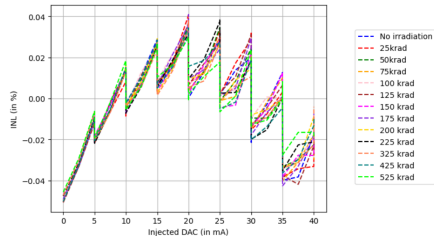
- Injects calibrated physics-like pulses for read-out electronics calibration.
- Custom made chips:
  - **CLAROC**, high frequency switch to create a pulse similar to LAr detector output. Fabricated on HV SOI CMOS XFAB 180nm technology.
  - **LADOC**, control current and DAC, TSMC 130 nm technology.
- CLAROCV4 and LADOCV2 under irradiation testing.
- **First version of calibration board CAD ongoing**.





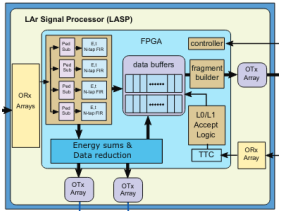


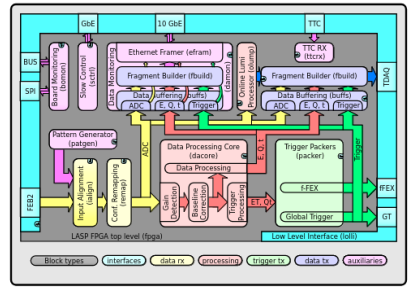
LADOC irradiation test INL under 0.1%



Off-detector electronics, **LAr Signal Processor (LASP)**

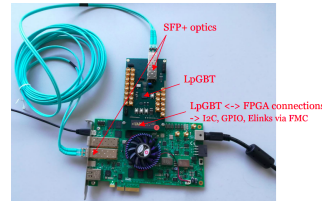
- DSP on signals from FEB board to compute signal energy and time stamping.
- ATCA blade with 2 FPGAs + Smart Rear Transition Module (SRTM)
- Firmware development well under way.
- The off-detector electronics will receive in total 345 Tbps of data via 33000 links at 10 Gbps.
- ML techniques to be used in FPGAs to mitigate the consequences of pile-up increase while computing energy reconstruction (see Johann Voigt's talk).
- **LASP T1 and T2 demonstrator under testing**.

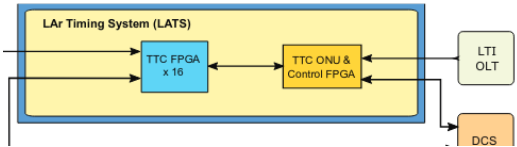


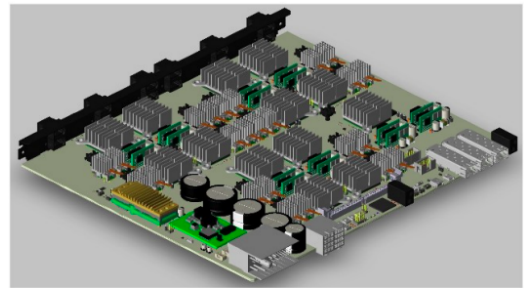


Off-detector electronics, **LAr Timing System (LATS)**

- Trigger, Timing and Control (TTC) for the on-detector boards using lpGBT protocol.
- LATournett boards under development:
  - Central control FPGA
  - 12 matrix FPGAs for communication with FEB2.
- Firmware validated on Cyclone10 DevKit
- Power-up sequence verified with POWERv2 board.
- LpGBTv0 FMC board to test Cyclone10/lpGBT communication.
- **First LATournett PCB to be fabricated this year.**







Summary

- Several challenges imposed by the HL-LHC conditions are being addressed on the phase-II upgrades for the LAr detector.
- Radiation-tolerant custom made ASICs for on-detector electronics on their final versions after exhaustive testing campaigns.
- Work has been done to integrate the ASICs and other components (for both on-detector and off-detector electronics) in testboards to evaluate its performance, as well as for FW and SW development.
- First versions of on-detector (FEB, Calibration) and LATs boards to be fabricated soon.
- Introducing ML techniques for FPGAs to achieve trigger and processing goals.
- The upgrades are well under way and on track for the deployment in 2026.

Thanks!