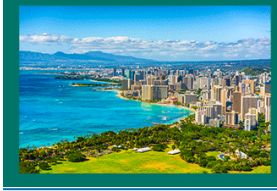
Buried Layer Low Gain Avalanche Diodes



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Buried Layer Low Gain Avalanche Diodes

A. Apresyan[4], G. Giacomini[1], R. Heller[4], M. Mannelli[3], R. Islam[2], Ronald Lipton[4], A. Tricoli[1], and W. Chen[1]

[1] Brookhaven National Laboratory, Upton, NY 11973
[2] Cactus Materials, Tempe, AZ 85284
[3] CERN, Geneva; Switzerland.
[4] Fermilab, P.O. Box 500, Batavia, Il 60510

E-mail: lipton@fnal.gov

Abstract. We report on the design, simulation and test of Low Gain Avalanche Diodes (LGADs) which utilize a buried gain layer. The buried layer is formed by patterned implantation of a 50-micron thick float zone substrate wafer-bonded to a low resistivity carrier. This is then followed by epitaxial deposition of a $\approx$ 3 micron-thick high resistivity amplification region. The topside is then processed with junction edge termination and guard ring structures and incorporates an AC-coupled cathode implant. This design allows for independent adjustment of gain layer depth and density, increasing design flexibility. A higher gain layer dopant density can also be achieved by controlling the process thermal budget, improving radiation hardness. A first set of demonstration devices has been fabricated, including a variety of test structures. We report on TCAD design and simulation, fabrication process flow, and preliminary measurements of prototype devices.

1. Introduction

An important development in recent years has been the recognition that silicon detectors with moderate intrinsic gain can extend the capabilities of silicon tracking detectors. The Low Gain Avalanche Diode (LGAD) is a device with moderate avalanche gain that can provide excellent time resolution and has prospects for excellent spatial resolution as well [1][2][3][4]. The current generation of LGADs, intended for HL-LHC [5][6] incorporate designs are optimized for fast timing, but suffer from some weaknesses:

- A large ($\approx$ 50 micron) region is needed around each pixel to moderate the field near the pixel edge and prevent premature breakdown.
- Radiation tolerance is limited by acceptor removal. Non-ionizing radiation deactivates dopants in the gain layer, reducing gain and eventually requiring voltages that risk single event burnout.
- The basic structure is formed by high energy implants are made through the top surface to define the gain region. These "reach through" implants are limited in geometry and resulting implant density

New variants can expand the design space, solve existing issues, and provide new opportunities. These new device designs include AC LGADs, inverted LGADs, and implantation variants including co-deposition of carbon. [7][8][9].

In this note we describe an alternate process which has the potential to expand the design space for these devices allowing for a dense, deep buried layer avoiding high-energy implantations.

2. LGAD process and Buried Layers

Standard LGADs are fabricated using a high energy implant through the surface to form a p-type high field multiplication region. The depth of the multiplication region is limited by the implant energy and the density is limited by straggling and diffusion. A deep Junction Termination Extension (JTE) implant is needed to limit the fields near the pixel edge to avoid premature breakdown. In the Buried Layer LGAD (BL-LGAD) we implant the gain layer on a base wafer and then add an epitaxial deposition to form the avalanche region. This allows more control of depth and implant density at the cost of some fabrication complexity. If the buried implant is patterned to terminate inside the cathode we can also eliminate the edge JTE implants. In this work we combine studies of a BL-LGAD with topside AC-coupling, which eliminates the inter-pixel gaps required in the current generation of devices.

3. Simulation

Candidate LGAD designs are simulated with Silvaco TCAD – a finite element 2D simulation. We use a full process simulation including implantation, annealing and epitaxy steps. Figure 1a shows the structure and electric field of a BL-LGAD device with a 2.5 micron gain region and drift region thickness of 50 microns. The thin, lightly doped gain region depletes quickly. The field in that region changes as $\frac{\partial E_{gain}}{\partial V_{bias}} = \frac{1}{t_{epi}}$. After the gain layer depletes the field extends to the drift region and the field increases as $\frac{\partial E_{gain,drift}}{\partial V_{bias}} = \frac{1}{t_{detector}}$ resulting in the fields shown in figure 1b. The doping and device thicknesses can then be tailored to achieve a saturated carrier velocity in the drift region and high enough field in the gain region to provide the desired gain and response operating point.

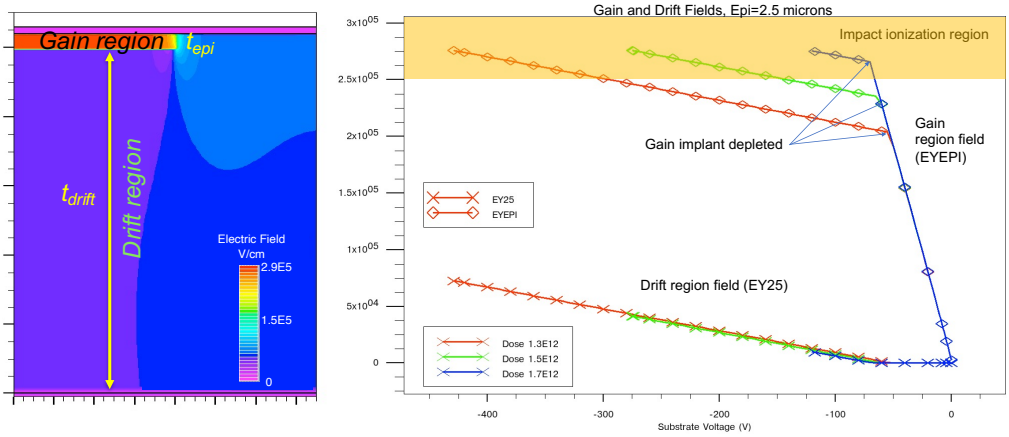

Figure 1. a) Two dimensional TCAD model of a buried layer LGAD showing the internal electric field in the epitaxial gain region and the drift region. b) Internal fields at the midpoints of the drift (crosses) and gain (diamonds) regions as a function of applied bias voltage for gain layer dose values of $1.3\times10^{12}(red), 1.5\times10^{12}(green)$ and $1.7\times10^{12}(blue)/cm^2$. The field needed for avalanche gain is outlined in light orange.

We model the gain of the device by tracking the ionization integrals derived from the electron-hole pair generation rates in the semiconductor [10].

$$R = \alpha_n|J_n| + \alpha_p|J_p|,\ II = \int_0^W \alpha_p e^{(\int_0^x(\alpha_p-\alpha_n)dx'}dx,\ Gain = \frac{1}{1-II} \tag{1}$$

Where R is the impact ionization generation rate, α_p and α_n are the ionization coefficients for holes and electrons, and II is the ionization integral. Figure 2 shows the gain calculated from ionization integrals for various values of gain layer thickness and dose.

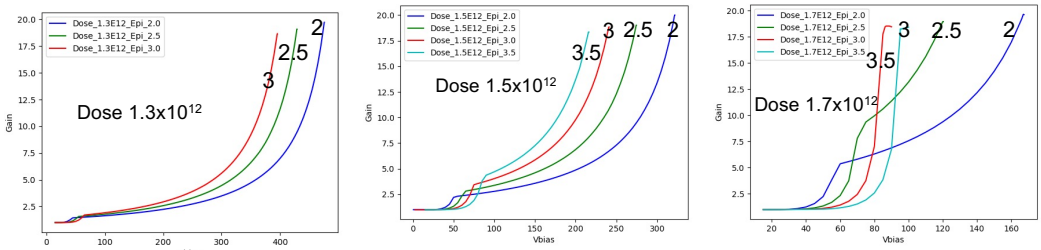

Figure 2. Gain as a function of applied bias for gain layer doses of a) 1.3×10^{12}, b) 1.5×10^{12}, c) $1.7 \times 10^{12}/cm^2$. The epitaxial thickness for each curve is labeled.

The simulation should be taken as indicative of trends rather than a quantitative prediction until it is calibrated to real sensors. It also suffers from lack of resolution near II=1 giving practical cutoff in the simulation at gain of about 20.

4. Prototype Run

An initial BL-LGAD prototype run was fabricated in 2020. For this run Cactus Materials handled the wafer bonding and epitaxy and Brookhaven National Laboratory designed the sensors and performed most of the processing [11]. A low resistivity four inch base wafer was directly bonded to a float-zone wafer, the float zone wafer thinned to $50\mu m$, and polished. A patterned gain layer with a boron dose of $1.75 \times 10^{12}/cm^2$ was implanted followed by a rapid thermal anneal. Three microns of high resistivity epitaxial silicon were then deposited. Later simulation indicates that these values are too large and a thinner epitaxy and reduced dose would provide improved operating margins. Processing was completed with the fabrication of the lightly doped n-type cathode implant JTE, oxide, metal and passivation layers. Scanning acoustic microscopy and secondary ion mass spectroscopy of the structures showed good wafer bonding and the expected implant densities.

Post-fabrication inspection revealed a high density of stacking faults in the epitaxy. This appears to be due to poor surface quality following the rapid thermal anneal. Subsequent prototype processing with a more standard oven anneal seems to have solved this problem. However the stacking faults cause high currents in the existing prototypes, especially in the large area devices, and limit the overall device quality and yield in this run. Full-wafer probe testing of all devices also showed high currents in some, but not all, diode-only structures suggesting that the high currents we observe originate from stacking faults rather than the gain layer.

5. Test Beam Results

A sample 2×2 mm device was exposed during the 2020/2021 test beam run at Fermilab [12]. The device under test was a 200 micron pitch detector with 50 micron-wide aluminum strips biased to 350 volts. Figure 3 summarizes the results. The prototype BL-LGAD suffers from low gain compared to other devices tested, with typical signals of 20 mV compared to $> 50mV$ for commercial devices. This limits the overall performance, however we still achieve reasonable time resolution and good position resolution. We note that the test beam device was operated well beyond the operating point simulated in section 2. We expect to measure gain more carefully with a laser system when laboratory facilities are again available.

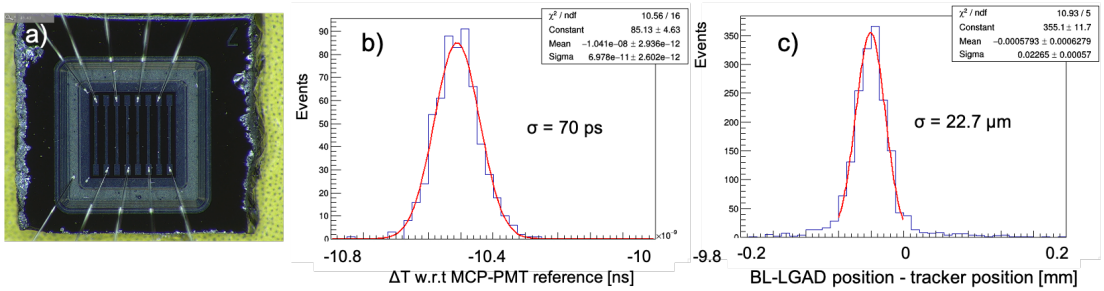

Figure 3. a) Photograph of the strip BL-LGAD bonded to it's readout board b) Time of arrival of the BL-LGAD signal with respect to the microchannel plate reference. c) Position as measured by charge sharing of adjacent strips with respect to the extrapolated track ($\approx 12\mu m$ extrapolated track resolution).

6. Conclusions

Despite the issues with stacking faults initial results for the BL-LGADs are encouraging, with moderate gain and promising time and spatial resolution. Planned Laboratory laser testing will help establish the systematic performance of these prototypes and inform the design of the next batches under fabrication. The BL-LGAD can combine with other developments, such as AC coupling, double-sided designs, multiple internal layers (i.e. the deep layer LGAD [13]) and 3D integration to expand the design toolbox for these promising new detectors.

7. Acknowledgments

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