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Radiation-hard ASICs for data transmission and clock distribution in High Energy Physics

Paulo Moreira *, Szymon Kulis

CERN, European Center for Nuclear Research, Switzerland

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ABSTRACT

Today's high-energy physics colliders host experiments that rely on transmission of massive volumes of data (exceeding tens of tera bytes per second) for physics analysis. From the 1990's to date, custom data links and Application Specific Integrated Circuits (ASICs) have been developed to address the specific needs of the on-detector transmission systems, namely radiation hardness, low mass and low power consumption. This paper reviews the most significant of those developments with particular emphasis on data transmission ASICs developed for the LHC experiments.

Contents

* Corresponding author.
E-mail addresses: paulo.moreira@cern.ch (P. Moreira), szymon.kulis@cern.ch (S. Kulis).

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1. Introduction

With the advent of high-energy high-luminosity colliders [1] and in particular with the approval of the LHC construction in June 1994 [2], it became evident that the on-detector electronic systems would need to be radiation hard to survive the required 10 years experiments' life time [3]. The approach used by the space industry [4] of relying on industry-qualified radiation hard Commercial Off-The-Shelf components (COTS) or of qualifying consumer electronics components was evidently not suited to the High-Energy Physics (HEP) programmes where radiation doses far exceed those encountered in space and the component count would mean prohibitive system costs. Needless to say that most functions required to implement the experiments could not be found in the consumer's market although this was certainly not the case for the data communications system where industry, though not able to provide the required radiation hard components, was ahead of the HEP needs [5,6].

This scenario sparked a series of developments tailored to the LHC experiments [7]. In many cases they profited either from the availability of radiation hardened technologies [8] or, later, from the intrinsic radiation hardness that some of the sub-μm CMOS technologies offered when combined with radiation hardening design techniques [3,9].

In the specific case of communications links (data, control, trigger and timing), embracing microelectronics at the time of the LHC approval opened the possibility of embedding devices such as Phase-Locked Loops (PLL), Delay-Locked Loops (DLL), PIN-Receivers, Laser/VCSEL drivers and Transceivers in the detectors systems. These days considered as "bread and butter" in any ASIC development those devices were, at the time, a novelty in the HEP field.

This paper addresses the ASIC developments that were made during the LHC era (roughly the last thirty years to date) dedicated to data transmission between the on-detector and off-detector systems. Most systems addressed in this paper concern digital data transmission, reflecting the global trend, with the notable exception of the CMS-Tracker analogue optical links [10]. A more generic account, spanning further back in time, can be found in [11] that reviews the evolution of various digital data links technologies used in HEP up to the early 2000's.

The next section will discuss the architecture of optical links with emphasis on HEP applications. The following section discusses the techniques used to achieve robust operation in a radiation environment and the trade-offs those imply. This will be followed by a survey of HEP ASICs implementations, focusing on designs that were, are or will be in use in the final system implementations (although others are mentioned where considered relevant). The paper concludes with a brief overview of current research.

2. HEP links architecture

HEP detectors require a diversity of communication links interconnecting front-end modules or ASICs and off-detector systems for trigger, data, control and data storage [11]. The focus of this work is on data links between the on-detector and off-detector systems which tend to be organized as shown in Fig. 1. Both the downlink (off to on-detector) and the uplink (on to off-detector) are present with the downlink carrying detector control data (including detector configuration and calibration), triggers and other time-synchronous signals. Hidden in the architecture is the transmission of the clock signal that, almost always, is not transmitted individually but is recovered from the downlink serial data stream. This clock can often be considered the master clock of the system, as is e.g. the LHC bunch crossing clock. The uplinks close the loop of the experiment's control systems plus carry the experimental data collected by the front-end detectors.

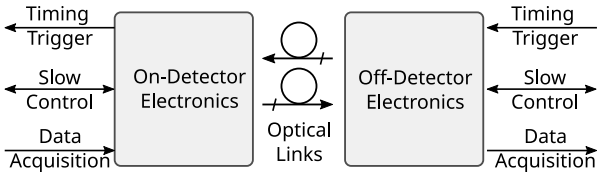

Fig. 1. HEP generic detector-to-counting room link architecture.

2.1. Trigger links

Trigger links have specialized requirements. In the case of the LHC, the shortening of the bunch crossing time from tens of microseconds, in e.g. LEP, to tens of nanoseconds in LHC and the large physical dimensions of the CMS and ATLAS detectors meant that at any given instant different parts of a detector actually see images from different events. To manage this situation, the idea of pipelining, early introduced at HERA [12] and the Tevatron [13], was necessarily used in the LHC data collection architectures. Such pipelines must maintain the ordering in which data in different events are generated and therefore a precise distribution of timing information to all stages of the pipeline had to be devised. This required the introduction, in the LHC experiments, of new fine-timing distribution systems with low latency, low jitter and phase adjustment capabilities. The requirement of precise timing distribution was conducive to de introduction of embedded and distributed electronics in the detectors. Prior to LHC, almost all timing and distribution systems were based on wiring precisely cut cables to different parts of the experiments. Apart from the large cost, the massive amount of material that would be required made that approach unfeasible for the LHC experiments. Instead, LHC has seen the first experiments where the timing of each of the million channels could be adjusted with sub-nanosecond resolution, simply by modifying a few configuration parameters in the embedded chips from a master computer controller. This was only possible by the introduction of novel (in the HEP field) ASICs with low phase-noise PLLs and programmable Delay Locked Loops (DLL) like the ones in the TTCrx [14] and the PHOS4 [15].

2.2. An unified architecture

Although in the past physically independent links were used for transmission of the different types of data (detector data, control, trigger and timing) for the LHC upgrades it became widely accepted that this distinction needs only to be logical and a single link can carry all the information needed at the benefit of system simplicity, cost and reliability [16].

Given the different nature of the data carried by the up and downlinks the bandwidth requirements are asymmetric with the uplinks requiring higher bandwidths due to the heavy load that the physics data represents (e.g. [17]).

A specific requirement for the HEP downlinks is that of fixed and deterministic latency. That is, HEP downlinks are used to provide timing information to the detectors and event tagging signals (or commands). It is important that, after system calibration, drifts of the timing signals are minimal and, moreover, that upon system re-initialization all the clocks and timing signals will be guaranteed to be at their calibration state, namely with a known phase/delay in relation to the master clock. For uplinks this requirement is not always true but systems participating in trigger event building tend to rely on fixed and deterministic latency links.

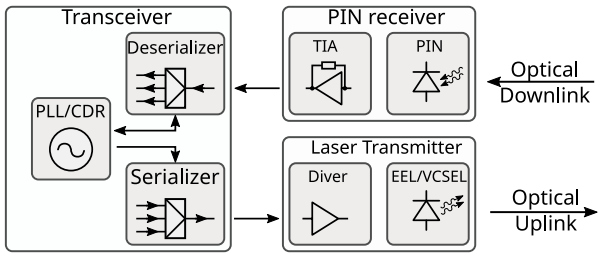

Fig. 2. Typical binary-data optical-link architecture.

Although Fig. 1 represents a typical configuration, including transmission of trigger data, some systems are moving away from this classical picture and are adopting a "trigger-less" data acquisition architecture [18]. Such systems allow for the triggering to be made off-detector in software using complex trigger algorithms free of latency constraints. The consequence is that all the data must be transmitted off the detector requiring massive uplink bandwidths which, for example, in the case of LHCb is 4 TByte/s [18].

The need for higher bandwidths due the increase of the physics data volume or the adoption of trigger less systems, pushed the developments of the data transmission ASICs towards higher data rates [19–21].

An important constraint on HEP data transmission systems, represented in Fig. 1, is the fact that the on-detector systems must be radiation hard while the off-detector systems are exposed to mild or no radiation. This imposes diametrically opposed constraints on both ends of the system. Off-detector COTS components can, and should, be used while for the on-detector systems custom developments must be made and the components, both the ASICs and the optoelectronics devices, must be qualified for radiation tolerance.

Typically the ASICs are designed using technologies that have been previously selected for their advantageous radiation tolerance characteristics and by additionally employing radiation hardening by design techniques [3,9]. Their radiation tolerance relies thus on the selected technology, the circuit design techniques and finally, their qualification by evaluating a relatively small number of samples for radiation hardness against Total Ionizing Dose (TID) and Single Event Effects (SEE).

For the optoelectronics devices a different path is followed where a survey of COTS devices available is made, samples acquired and tested for radiation. Once suitable devices are identified, a contract is made with the manufacturers that secures the manufacturing and supply of devices with the desired radiation tolerance characteristics [22].

The use of COTS in the counting room forces the on-detector ASICs to accommodate industry data transmission standard protocols [19,21,23]. However the use of FPGA based systems has allowed some flexibility and, within constraints, the development of ad-hoc protocols to build SEE robust data links [24].

2.3. Data transmission building blocks

The components needed to build a digital data transmission optical link are illustrated in Fig. 2. They typically include a transceiver, an Edge Emitting Laser (EEL) or a Vertical Cavity Surface Emitting Laser (VCSEL) transmitter and a P-Intrinsic-N (PIN) photodiode receiver [25]. The roles of these parts is as follows:

Transceiver: optical links transmit binary data as a stream of bits (serial data). The conversion of parallel binary data into a serial stream is a process called serialization (or time-division multiplexing) and the reverse process de-serialization. Transceivers implement those two processes. However, practical data transmission requires more than simple serialization and de-serialization with data framing, line coding/decoding and forward error correction also implemented by the transceivers [25]. Moreover, transceivers include a Phase-Locked Loop (PLL) to generate the high frequency clocks needed for the serializer or to recover the clock from the incoming serial data stream, an operation commonly known as Clock and Data Recovery (CDR). Although described here as a single object, in some systems the transceiver function is split between receiver and transmitter ASICs.

Laser transmitter: for transmission over optical fibres a laser transmitter, composed of a driver and an EEL or VCSEL, is used to convert the electrical signal representing the serial bit stream into an optical signal.

PIN receiver: a combination of a PIN-photodiode and a transimpedance amplifier (TIA) is used to convert the optical signal back into an electrical signal.

Wavelengths typically used for data transmission are 850, 1300 and 1550 nm. The shorter wavelength is used in conjunction with multi-mode fibres for relatively short distances ($\leq$ 300 m) and low data rates ($\leq$ 10 Gbps). Long haul ($\geq$ 10 km) high speed transmission ($\geq$ 10 Gbps) requires the use of single mode fibres and the longer wavelengths (lower attenuation and/or lower dispersion). To date HEP optical links span distances smaller that 300 m and operate at data rates up to 10 Gbps. This has allowed the use of multi-mode fibres and optoelectronics components [22,26]. Future links foreseen to operate at higher frequencies will need to be single mode systems to avoid hitting the dispersion limit [27].

A detailed review of optoelectronics link components for HEP can be found in this issue [28] and will thus not be further discussed in this article.

3. Designing communications ASICs for radiation tolerance

The components mentioned above are functionally the same for data centres, telecommunications or HEP links. The radiation environments of the particle physics detectors however impose specific constraints on the design of those components related to the robustness against TID and SEEs. Optical links, for system efficiency, tend to operate at the fastest speed possible for a given technology node. Designing for TID and SEE robustness, however, imposes penalties on the maximum achievable speeds and power consumption.

3.1. TID robustness

Designing for TID robustness has been an evolutionary path that included the use of specially hardened technologies [8,29]. However, the advent of sub-μm technologies opened the possibility of designing TID robust circuits using main-stream CMOS technologies provided that some constraints are followed during circuit layout [30].

The use of Enclosed Layout Transistors (ELT) has allowed to effectively minimize the leakage currents between the source and drain of NMOS transistors that are induced by ionizing radiation, in technologies without Shallow Trench Isolation (STI) (e.g. 0.25 μm CMOS). Additionally, p-substrate guard-rings surrounding n-diffusion were successfully employed to prevent the turn-on of parasitic Field Oxide (FOX) transistors [30]. These measures were not needed for PMOS devices since for these ionizing radiation does not induce drain–source leakage.

The ELT geometries came at the cost of bigger than minimum transistor widths (W) and minimum achievable W/L (> 2) ratios. The use of non minimum width devices is not penalizing from the point of view of speed since high frequency operation requires the gate capacitance ($g_m \propto C_g$) to dominate the circuit parasitic capacitances. However it impacts the power consumption of the ASICs since power dissipation is directly proportional to the circuit capacitances (gate, drain/source diffusions and interconnects). Additionally, the presence of the guard rings resulted in relatively larger circuits and thus in higher interconnects loading (when compared with non-ELT layouts). Examples of ASICs designed using these techniques can be found in [7].

Another phenomena that pushed towards the use of large devices is the degradation of the transconductance (g_m) with TID. This affects

both the NMOS and PMOS devices, the latter being more sensitive. For example in a 65 nm CMOS technology, a minimum size NMOS device suffers a degradation of 20% of the saturated drain current while for a PMOS the current degrades by 60%, at 2 MGy TID [31]. It is also shown that devices with non-minimum L and W suffer relatively less g_m degradation when compared with minimum size devices [30,32,33]. High-frequency circuits require the use of minimum gate length (L) to achieve the highest operation speeds. Consequently, relatively large W devices have to be selected, not only to minimize the relative amplitude of the leakage currents of NMOS devices, but also to reduce the impact of TID on the transconductance of both NMOS and PMOS devices. A comparative study [34,35] made on ring-oscillators in a 65 nm CMOS technology, points clearly to the need of using large W devices. In this study, for example, a ring oscillator built with transistors $W_n = 150$ nm and $W_p = 150$ nm has seen its frequency reduced by 35% at 4 MGy while one built with $W_n = 300$ nm and $W_p = 600$ nm degrades only by 25%. The same study shows a consistent and monotonic increase of the radiation tolerance with W for all the device types included (high, regular and low threshold voltage).

For the technologies currently being used or considered for the HEP projects ($\lesssim 130$ nm) shallow tench isolation has rendered obsolete the use of substrate guard rings between n-diffusions. Additionally, the use of ELT devices is not as critical for TID tolerance as used to be for older technologies (e.g. 250 nm). However, for the same size, ELT devices prove to be more robust against radiation both for leakage and g_m degradation. For example, in a 65 nm CMOS technology a PMOS device with $W = 1$ μm suffers 50% reduction of its saturation current at 4 MGy while the ELT version suffers a smaller reduction of 33% [31]. As effective as ELT devices can be to mitigate the TID induced degradation, their use in very deep sub-micron technologies (e.g. 28 nm) is not allowed by the foundries (and cannot be waived) and is no longer a technique the engineer can rely on.

Very high data rate circuits tend to use dynamic logic [36] for high speed and low power operation. Dynamic logic is however very sensitive to leakage currents that corrupt the charge stored in the flip-flops storage nodes. With the increase of the sub-threshold leakage currents in advanced technologies, even in the absence of radiation damage, dynamic logic has to resort to the addition of "retention" devices that effectively act as "weak" latches containing the storage nodes [37]. This technique can be also used to address the increase of leakage currents due to TID in modern technologies where, for example, the leakage current of a NMOS device in a 28 nm (L=30 nm) can increase by 4 orders of magnitude at 10 MGy [38].

Current Mode Logic (CML) logic circuits are built using resistive loads and NMOS transistors only. They therefore present the ultimate robustness against TID since they avoid altogether the use of PMOS devices and use polysilicon resistors that are not affected by radiation. The main disadvantage of CML is the presence of high static power consumption. When compared with CMOS logic (either static or dynamic), CML is power hungry and should be thus reserved for the very last stages of serializers, high-frequency prescalers and high data rate line and laser drivers. CML logic has been used successfully in HEP to build 5 and 10 Gbps transceivers and laser drivers that proved to be radiation hard [21,39–41].

3.2. NIEL robustness

Although most ASICs for LHC have been designed using CMOS technologies a few have used BiCMOS technologies where, besides TID [42], damage induced by Non-Ionizing Energy Loss (NIEL) needs also to be taken into account for bipolar transistors [43]. Both TID and NIEL radiation degrade the bipolar transistor current gain (β), defined as the ratio of the collector and base currents (I_c/I_b). The TID increases the surface component of the base current while displacement damage induced by NIEL increases the bulk component of the base current due to the increased recombination of minority carriers in the base. Both effects are more important when the devices are operated at low injection levels (low currents). The device sensitive to NIEL depends on the semiconductor technology used and device geometry with, for example, narrower base thickness yielding better radiation tolerance and lateral devices being less robust than vertical devices [43]. For a given technology the engineer is thus faced with the choice of device type (if multiple types are available) and he has to bias the devices at high collector currents to minimize the impact of β degradation. The latter action can only minimize the effects of radiation and is penalizing from the point of view of power consumption.

3.3. SEE robustness

A very important consideration for HEP links, and thus communication ASICs, is their robustness against Single Event Effects (SEE). In their mildest form SEEs might reveal themselves as a single bit error during transmission and, at worse, as a link de-synchronization that might last for several milliseconds seriously corrupting data transmission. The first type of events is typically the consequence of an upset on the data path circuitry, logic gates or flip-flops, while the latter tend to be the result of upsets on the transceiver PLL/CDR, on the ASIC configuration registers or on the ASIC Control State Machine (CSM). De-synchronization events have a high impact if they happen on CDR circuits driven by the downlinks since the downlink receivers tend to be the clock sources for the on-detector sub systems and thus an integral part of the detector synchronization.

3.3.1. Configuration registers and control state machines

To prevent functional interrupts, it is important to protect the configuration registers and the ASIC control state machines since any lasting Single Event Upset (SEU) can lead to a long link downtime. Triple Modular Redundancy (TMR) is one of the most robust techniques available to the designers and has been used since the 1950s [44]. This technique is generic and can be applied at various design levels: from protecting a single bit of information to full complex blocks.

While providing ultimate protection against SEE in digital designs, circuit triplication comes with associated costs. Typically, the circuit area and power consumption are increased by more than a factor of three (additional resources are required for the majority voters and buffers). Moreover, the addition of majority voter cells limits the maximum frequency of operation of digital circuits which is especially important in case of circuits operating at highest frequencies (e.g. frequency dividers in a PLL).

TMR is a common choice for configuration registers and the ASIC control state machines (e.g.: power-up calibration, frame acquisition) as these are essential for operation free of functional interrupts and as such require maximum protection and prompt correction of SEUs. The power consumption overhead from TMR for configuration registers is typically negligible (on the chip level) due to the quasi static operation of these blocks and is typically further reduced by utilization of clock gating techniques. The HEP community has developed dedicated tools that automatize the process of converting the Register-Transfer Level (RTL) code into its triplicated version [45].

3.3.2. Clock generation

High up in the list is the design of SEE robust PLLs and CDR circuits. Traditionally these circuits have been designed in the HEP community as analogue PLLs and thus no standard recipes for hardening have been developed.

The PLL/CDR loop utilizes a Phase Detector (PD) and/or a Phase Frequency Detector (PFD) to close the loop. The typical implementation of a PFD contains flip-flops and therefore it is sensitive to SEU. An SEU in the PFD could result in enabling the charge pump up to a period of the reference clock (far exceeding the normal time for which it is enabled when in lock) leading to a significant change in the Voltage Controlled Oscillator (VCO) frequency [46,47].

For non-linear phase detectors (bang–bang, Alexander) [48], which are also typically implemented with flip-flops, SEU are not of concern as they are virtually undetectable in the random bit sequence caused by random jitter.

The next critical component in the analogue PLL is the charge pump driving the loop filter. As charge pumps have no memory elements, they are sensitive to SET only. Here, the typical problem is the long recovery time (required to evacuate the charge deposited by radiation) due to the limited current. As a solution, the charge pump sensitivity can be minimized by employing a tri-state voltage charge pump which reduces the number of vulnerable nodes present and increases the rate of charge sourcing and sinking [49].

Both classes of events discussed above alter the control voltage of the VCO and therefore create a frequency error at the PLL output. As the PLL/CDR circuits operate in a phase domain, the frequency error has to be converted to a phase error before it can be corrected by the control loop. Therefore, a higher loop bandwidth generally reduces the magnitude of the maximum phase error caused by the SEE.

At the heart of each clock generator block there is a radiation hardened VCO. Two architectures are common: CMOS ring oscillators and LC oscillators, each of them exhibiting different SEE sensitivities. Among others, ring oscillators can suffer from missing pulses [50], phase jumps [51,52], or harmonic oscillations [53]. Mitigation techniques proposed by authors include sizing of the active devices, using relatively large bias currents and replication of bias circuit or parts of the oscillator. Similarly, LC oscillators suffer from a temporary reduction of oscillation amplitude and frequency change [54]. This sensitivity can be reduced adding a discharge path and a decoupling resistor to the bias circuit. Another sensitivity, not present in the ring oscillators is related to the MOS varactor typically used for frequency tuning of LC oscillators [55] for which a modified tuning topology was proposed in [56]. Recently, it was reported that passive components forming an LC tank oscillator exhibit sensitivity to radiation [57,58] which will pose challenges for future generations of extremely low-jitter oscillators.

Strong SEU protection is crucial for frequency dividers in PLLs or CDR circuits where SEUs in the state register results in an abrupt phase jump of the clocks. These phase jumps are likely to unlock the PLL and thus to introduce a large downtime in the links. Typically, the phase error is automatically corrected by the feedback loop. TMR is frequently used for those circuits [47,56]. It does however, introduce speed limitations since the frequency dividers operate at the bit clock frequency (or half that frequency for double data rate architectures). In less critical applications, other radiation-hardened-by-design (RHBD) techniques (e.g. double interlocked cell) could alternatively be used to minimize the SEU sensitivity of the memory elements [59].

3.3.3. Data path

Single or small bursts of bit errors (e.g. contained within the boundaries of one or two transmission frames) might be tolerable by the system and thus when designing for a specific detector system one needs to judge if protection against these errors is justified. At the limit, one can discard altogether protecting the data path and accept the occasional burst of errors. However, when designing a general purpose data transmission ASIC, that cannot be assumed to be case. The “brute force” approach would be to build the data path and serializer as a TMR circuit. However, this is not the best approach. This limits the speed of the serializer (due to the additional gate delays from TMR) and, most importantly, neglects the fact that SEEs can inject errors further down the chain in the laser-driver, laser, pin-diode and pin-receiver. Laser driver and pin-receivers are “analogue” type devices that cannot be designed foolproof against SEE. A better option is to add to the transmitted data a Forward Error Correction (FEC) code [60,61]. These allow, within limits, to correct bursts of errors and thus make low bit error rates achievable in HEP environments.

Fig. 3 shows the impact of using FEC encoding for an experiment made with GBTIA [63] PIN-receiver in the VTRx module [64]. In the experiment, data was transmitted either with no encoding or using the FEC encoding implemented in the GBTX [19]. The flux of 70 MeV protons during the experiment was $1\times10^{8}\,\mathrm{p/cm^2/s}$. The measured code gain is 2 dBm at a Bit Error Rate (BER) of 10^{-6}. The figure also clearly shows that simply increasing the optical power cannot overcome the effects of SEE while the FEC code basically restores the thermal noise limited signature of the receiver sensitivity.

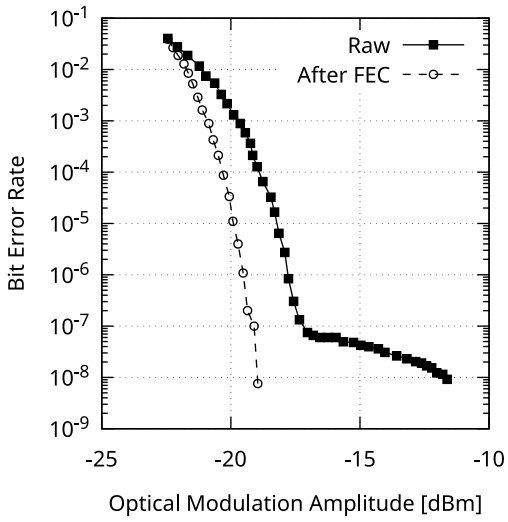

Fig. 3. Data transmission errors with and without FEC in a SEE experiment [62].

3.3.4. Verification

Designing for SEE robustness is perhaps one of the most difficult tasks facing the engineer designing ASICs for HEP applications, including the communications ASICs. As careful and thorough the engineer is in predicting failure mechanisms, it is not uncommon that SEE testing will reveal an unforeseen failure mode or a badly protected or unprotected node that makes the circuit to fail under radiation. Verification methodologies are thus mandatory to increase the chances of success upon SEU testing and real operation conditions. Nowadays commercial tools exist that can inject SEEs as current pulses on analogue circuits [65] and simulate random bit flips in digital circuits [66]. As not all of the verification needs of ASICs for HEP applications are served by commercial offerings, dedicated tools and methodologies have been developed in the community [67,68]. These allow extensive verification of the SEE immunity of the circuit prior to fabrication thus maximizing the chances of a successful ASIC design.

4. Communications ASICs for LHC

This section reviews the ASICs and design techniques that have been used by the HEP community to build optical link components for the LHC detectors and upgrades. The techniques used depend on the integrated circuit technologies available at the time and fall within the broad categories defined above. The most important aspects for each ASIC will be briefly discussed.

4.1. Early ASICs, building the LHC detectors

With approval of the LHC and the complexity of detector systems planned, it was clear to the community of physicists and engineers developing the experimental systems that ASICs had a fundamental role to play in the construction of the detectors. An early candidate for the development of a dedicated communications ASIC was the LHC Timing, Trigger and Control (TTC) distribution system. Specifications for the system matured in the early 1990s [69]. The system envisaged the distribution of the LHC bunch clock (40.079 MHz) to all the

detectors plus beam-synchronous messages specific to each detector or sub-detector. The TTC signals were broadcast over passive optical networks to several thousand destinations providing two time-division multiplexed channels (L1 trigger and commands) at 80 Mbps encoded in biphase mark for optimal DC balance and thus low jitter [70].

4.1.1. TTCrx

The receiver ASIC developed for the TTC system [70] was the TTCrx [14]. The TTCrx delivers the 40.079 MHz LHC clock signal, the first level trigger decision signal and its associated bunch and event numbers. In addition, it provides for the transmission of synchronized broadcast commands and individually addressed commands and data. It is programmable to compensate for particle flight times and for propagation delays associated with the detectors and their electronics. To implement these functions, the TTCrx includes a limiting amplifier, a PLL and two phase shifters based on Delays-Locked-Loops (DLLs) with a 104.2 ps resolution. Its operation is controlled by data transmitted by the TTC source and by an I^2C interface.

At the time of the development, the path to build radiation robust ASICs had not yet been established by the community. Consequently, the design went through several implementations in different CMOS technologies culminating with the production version [71] being made in the BiCMOS DMILL technology that was designed for radiation hardness [8].

The DMILL technology offered a choice of vertical bipolar and MOS transistors in a Silicon On Insulator (SOI) substrate. The TTCrx took advantage of both types of devices with the limiting amplifier using bipolar transistors and the remaining circuitry using the CMOS devices. Bipolar transistors presented the advantage of lower noise for the design of the limiting amplifier but were also known to be affected by displacement damage [8]. This damage translates into a base current leakage that degrades the transistor current gain (β) since it does not contribute to the collector current and thus the signal gain. This effect can be easily mitigated by operating the bipolar at relatively high collector currents.

To mitigate SEE effects, both the data reception and the configuration registers are protected by a Hamming check sum [72], allowing the correction of single bit errors and the detection of dual bit errors. Single bit data errors are corrected at reception while an SEU correction state machine checks the configuration registers in a cyclic way visiting all the registers with a periodicity of 1 ms. Additionally, a watchdog monitors the PLL for losses of lock lasting more than 50 ms, automatically resetting the chip if those occur. The ASIC was tested for TID effects by neutron and gamma irradiation and for SEUs by proton and heavy ions irradiation [71].

The TTC system, being built as a broadcast passive optical network (unidirectional), had the main disadvantage of being a "blind system" in the sense that the delivery of timing, synchronized commands and chip control could not be handshake or verified by the trigger system source. Although not strictly necessary for operation, the inclusion of the I^2C interface in the TTCrx was thus a way to circumvent this difficulty in what concerns the chip control itself. It relied however on the availability of an independent control link.

4.1.2. DORIC

The ATLAS SemiConductor Tracker (SCT) and Pixel detectors have adopted an alternative approach to the distribution of the TTC signals to the front-end modules via optical fibres [73]. The system relies on a single channel transmitting TTC data at 40 Mbps from which the clock is extracted and the TTC data retimed.

The Digital Optical Receiver Integrated Circuit (DORIC) was developed for that purpose [74]. It receives and amplifies the photocurrent from a PIN-diode. The amplified signal, which is biphase mark encoded, is then processed by a sequential circuit to present at the chip outputs (two redundant pairs) the recovered clock signal and the serial retimed data converted to Non-Return-to-Zero (NRZ). The data retiming and clock extraction circuit, being sequential and driven by the data signal itself, depends on setting delays for correct operation. This is achieved by a DLL that adjusts automatically the duty-cycle of the recovered clock to 50%.

Several versions of the chip were developed in three technologies (including DMILL [75,76]) but the production version for the ATLAS SCT detector was fabricated in 0.8 μm BiCMOS AMS [77]. This technology is not radiation hard but careful design choices and radiation testing qualified the device for the SCT radiation environment, namely, 100 kGy (Si) and $3{\cdot}10^{14}$ n cm^{-2} (1 MeV equivalent), by exposing the ASIC to neutron and gamma irradiation [74,77].

The use of bipolar transistors was restricted to NPN and the logic is implemented as current mode logic. Additionally, the NPN transistors are biased at relatively large currents to avoid β degradation and preference was given to circuit topologies that are β "insensitive" [77].

Although a successful ASIC, the SCT DORIC exceeded the power budget required by the ATLAS pixel detector systems and its radiation hardness was also below the required 10^{15} n cm^{-2} (1 MeV equivalent). Given the potential for radiation hardness of standard sub-μm CMOS technologies, when used in conjunction with radiation hardening layout techniques [30], the design was ported to 0.25 μm CMOS. This allowed both lower power consumption and higher radiation hardness.

The circuit functionality and architecture remained unchanged with the most notable differences being the use of a single ended preamplifier in a pseudo-differential configuration to improve the power-supply rejection, a feedback loop to cancel the offset of the differential post-amplifier and the adoption of LVDS signals for the data and clock outputs. Additionally, the ASIC was designed as a four channel device.

The chip was successfully qualified for the ATLAS pixel detector radiation environment [76,78].

4.1.3. RX40

The CMS tracker adopted a token-Ring like Network (RN) for the on-detector control system with the Control and Communication Unit (CCU) ASIC managing the ring communications and interfacing with the front-end modules [79,80]. This network carries all the traffic related to the distribution of the slow control commands to the front-end integrated circuits. It implements a fault tolerant redundant network architecture capable of functioning even upon failures of a number of non-consecutive modules in the ring. The control data is sent from the Front-End Controller (FEC) to the RN over an optical fibre at 80 Mbps. The first level trigger decisions (L1) and the bunch-crossing clock (40.079 MHz) are combined and sent to the RN via a second fibre. The combined clock-L1 signal behaves as a normal clock signal in absence of a positive L1 decision but upon a positive decision the positive cycle of the clock is "suppressed" (the clock is maintained at the low level for a full clock period). A PLL is used on-detector to recover the clock and the L1 signals [81]. Both the control data and the combined clock-L1 signal are received by a custom-designed PIN-receiver, the RX40 [82]. This receiver is built as a four channel device to handle both channels plus the redundancy built into the RN [79]. For radiation tolerance the ASIC was built in a commercial 0.25 μm CMOS technology using ELT geometries [83].

Among the most interesting features of this chip are the techniques adopted to cope with the degradation of the PIN diodes due to radiation. With non-ionizing radiation, the Responsivity (R) of PIN-diodes decreases and their dark (leakage) current (I_d) increases [84]. The expected degradation of the PIN-diode responsivity in the tracker system means that the signal current can be of the order of 500 μA at beginning of life and be reduced to 10 μA at the end of life. Moreover, the dark current can increase from a few pA to a few 100 μA.

Low signal currents (∼ 10 μA) expected at end of life will lead to low Signal-to-Noise Ratio (SNR) resulting in prohibitively high BER. The receiver needs thus to be designed as low noise and high gain. However if the gain is high, operating with high currents (∼ 500 μA) of the beginning of life conditions can saturate the preamplifier stage

and again lead to a high BER. The adopted solution was to design the transimpedance preamplifier stage with automatic gain control thus ensuring low noise and high gain for small signals and low gain for large signals, avoiding saturation.

In the RX40, the PIN-diode is reverse-biased between the supply rails and the preamplifier input. The preamplifier acts thus as the negative terminal of the bias network and should be able to absorb the diode dark current. For the tracker system the end of life dark current ($\sim 100\,\mu A$) has the potential to saturate the preamplifier. It is necessary to deviate this current from the preamplifier input, a job that is done by a current sink that drains any excess DC current. As is the case for the DORIC chip discussed above [76], this ASIC uses a pseudo-differential topology to improve the power supply rejection ratio. It is the average of the difference between the outputs of the preamplifier stage and the dummy stage (a replica of the preamplifier stage) that is used to control the current sink that absorbs the PIN-diode dark current.

A point to keep in mind when designing optical receivers for HEP systems is the presence of bit errors that are induced by particle hits on the PIN-diodes themselves. These have been observed in the receivers discussed so far (TTCrx, DORIC and RX40) [71,73,85]. At the expense of having to triplicate the PIN-receiver, there is not much that can be done to mitigate SEE on PIN-diodes at the circuit level since they are virtually indistinguishable from the signal. Increasing the optical power can improve the situation (see e.g. [73]) but the bit error rate will saturate at a level that is determined by the flux of the particles causing the SEEs. A solution is only possible at the system level by the use of error correction codes as discussed before.

4.1.4. VDC

Acquiring data from the detectors through optical links requires radiation hard serializers and EEL/VCSEL drivers. An early example of an HEP VCSEL driver is the VDC. The VDC was developed for the data acquisition uplinks of the ATLAS Semiconductor Tracker and Pixel detectors. It was developed in parallel with DORIC chip and its development path mirrors very closely that of the DORIC ASIC with the production implementations in 0.8 μm BiCMOS AMS [77] for the ATLAS SCT detector and a four channel version produced in 0.25 μm CMOS for the ATLAS pixel detector [78].

The BiCMOS version is a two channel, for redundancy, cathode VCSEL driver that operates at 40 Mbps. It accepts the LVDS signals provided by the ATLAS SCT front-end ASIC [77]. It is capable of modulating the VCSEL with currents up to 20 mA to which a 1 mA current is added to bias the VCSEL above threshold. The modulation current magnitude is programmed through an external voltage supplied to the chip. Because the data stream fed to the driver is NRZ with no encoding to guarantee the DC balance, the circuit was designed to draw constant current from the supply (independent of the logic state) so that no switching noise is introduced in the power supply [77].

The 0.25 μm CMOS version is a four channel device operating at 80 Mbps and designed as an anode driver to be able to drive a common cathode VCSEL array [76].

4.1.5. GOL

The design of radiation hard ASICs in 0.25 μm CMOS [7] opened the horizon to Gpbs rad-hard serializers [86]. An early example is the GOL serializer [23,87] initially developed for the CMS ECAL and which found widespread use in the four LHC experiments.

Underlining the development was the concept of compatibility with transceivers for serial links developed by the industry. This would avoid the development of ad-hoc off-detector systems (where radiation is not a concern) and would require minimum effort to develop test systems for the ASICs and data transmission systems being developed. Under that token the GOL was designed to be compatible with two families of chips, the TLK1501 & TLK2501 from Texas Instruments and the HPMD-1024 from Hewlett-Packard. These chips used, respectively, the 8B10B [88] and CMIT [89] line coding that the GOL ASIC supports. For flexibility, it can operate at either 800 Mbps or 1.6 Gbps interfacing with the front-end electronics through a 16-bit or 32-bit parallel bus, respectively.

The ASIC is capable of driving 100 Ω differential transmission line (or cable) and integrates a laser driver being able to directly drive an EEL.

COTS laser drivers tend to integrate a feedback loop to set the laser mean optical output power. This is done by a regulation loop that automatically adjusts the laser bias and modulation currents. Such a control loop requires sensing the laser light output using a PIN diode. However the degradation of the PIN-diodes responsivity in HEP environments [84] prevents the use of such architectures. A solution is to make the laser-bias and modulation currents "remotely" programmable. This solution, adopted in analogue form for the VDC [76] and in the digital form for the GOL [23], has been the norm for the laser drivers built for HEP. Its drawbacks include the need for the output optical power to be monitored off-detector (either directly or by estimating the bit error rate) and that the chip should start with a reasonable configuration that takes into account laser aging, radiation damage and ambient temperature fluctuations. Setting the bias and modulation currents in the GOL is done either through an I^2C or a JTAG interface.

The ASIC was proved to be radiation tolerant to 100 kGy TID. Its sensitivity to SEEs was assessed with its impact on data transmission estimated for a few LHC detector environments [87]. It displayed error free operation during 60 MeV proton irradiation but revealed PLL unlocks during heavy ion irradiation testing. As discussed above, PLL unlocks, when present, tend to dominate the SEE response of communication ASICs and it is thus important to design SEE robust circuits and architectures (a point we will return to later in the paper).

4.1.6. LLD

A singular approach, that deviates from digital transmission, was adopted for the CMS Tracker for the readout optical links. Data from the 128 channel analogue pipeline of the APV25 ASIC [90] are transmitted over the optical link together with a digital header and trailer. The pipeline data is transmitted as 7-bit (128-levels) 40 MS/s analogue signal. The outputs from two APV25 are further multiplex enabling each fibre to carry data from 256 silicon microstrips. Besides the radiation hardness constraints and the need to control the mean optical power to stabilize the laser, as discussed above, three additional factors are important for the performance of such a system: linearity of the laser (proportionality between the modulation current and the output optical power), linearity of the laser driver and low noise performance of the laser transmitter (driver plus laser). Although for digital transmitters noise can almost be ignored, for amplitude sampled systems the SNR of the transmitter is reduced by the number of analogue levels (128 in this case) and noise optimization becomes an important consideration [91]. For the tracker a 4-channel EEL Linear Laser Driver was initially developed in 800 nm BiCMOS process [91] with the production version, later developed, being a 3-channel device in 250 nm CMOS [92]. The chip is I^2C programmable allowing adjustment of the EEL-bias current and the transconductance gain (four settings). For linear operation the input stage is a trans-conductor with resistive source degeneration and an active bulk driving technique [92]. The ASIC achieved a 8-bit equivalent dynamic range with an analogue bandwidth of 250 MHz and the specified radiation hardness.

Since November 2009, the LHC and its LHC experiments have been in regular operation. The success of the physics experiments, and in particular the Higgs boson confirmation in 2012 [93], is a testimonial to the importance microelectronics has played and will continue to play in the HEP field. Moreover, the fact that the first generation ASICs have survived now for more than 10 years in operation under stressful radiation conditions, displaying no discernible TID degradation or functional interrupts, validates the principles and methods adopted to design and qualify ASICs for TID and SEE tolerance.

4.2. Second generation ASICs

With the LHC detector systems installed, the start of LHC operation and the beginning of data taking, new systems were being planned for the HL-LHC phase I upgrades that would take place during the LHC long shutdown (LS2) between 2019–2021. The high luminosity of the upgrades called for high bandwidth links (~ 5 Gbps) and up to 1 MGy TID radiation tolerance. With the experience the HEP community acquired designing, building and commissioning detector systems for the LHC, it was clear that future systems would become more complex, harder to test and debug, more expensive but also that the engineering resource in the community were unlikely to grow in proportion. It was thus necessary, wherever possible, to adopt common solutions of the type one "one fits all". Ideal candidates for such an approach are optical links and their components: optoelectronics and ASICs. This led to the specification and development of the Versatile Link optical modules VTTx and VTRx [64] and of the GBT chipset [41]. Both projects were developed by collaborations across several HEP institutes.

4.2.1. The GBT chipset

The GBT chipset consists of four ASICs: the GigaBit Transceiver (GBTX), the GigaBit Trans-Impedance Amplifier (GBTIA), the GigaBit Laser Driver (GBLD) and the GigaBit Slow Control Adapter (GBT-SCA). The GBT-SCA [94], not being strictly a communications ASIC, will not be discussed in this paper.

The chipset development was the embodiment of the idea, discussed before, that links providing different services (e.g., TTC, DAQ and control) do not need to be physically distinct entities, they can share the same physical resources and, as a consequence, development costs and engineering resources. Another very central consideration that guided the development of the chipset was the compatibility with COTS systems. In particular FPGAs were not only ubiquitous in HEP systems (off-detector) but provided the high bandwidths needed for the HEP systems. Although implementing an ad-hoc line coding the GBTX was designed to be compatible and to communicate with, at the time, state-of-the-art FPGAs [24].

The chipset was designed in a commercial 130 nm bulk CMOS technology. It operates at 4.8 Gbps and implements a complete solution for data transmission between the detectors and the counting room. The target for radiation tolerance was 1 MGy.

Being a general purpose device, and as such having to carry trigger information, the GBTX [19] was designed as a fixed and deterministic latency device (for both the up and downlink directions). Flexibility is built-in in the ASIC by providing a highly configurable interface to the front-end devices. The concept of parallel bus (present in the GOL chip) is abandoned in favour of multiple electrical serial links (e-links) that can interconnect to multiple front-end devices. Each e-link data rate is independently configurable to match, as well as possible, the bandwidth requirements of the front-ends, enabling various levels of data aggregation. To ensure proper operation the e-links implement a phase alignment mechanism that allows data to be received correctly from devices transmitting to the GBTX with random phases [95].

In the GBTX, SEE robustness is achieved by TMR protection of the configuration registers in the relatively low speed digital logic. As discussed, TMR imposes however limitations on the operation speed of circuits. In PLLs the frequency divider operates at the highest frequency and needs to be protected for SEE since upsets can lead from single bit period phase jumps to full frame cycle slips. This can easily unlock the PLL and thus lead to long link down times. The conflicting requirements between operating at high speeds and the need for TMR protection was resolved in the GBTX by the use of dynamic "true single phase" flip-flops in which voting is done on one of the internal storage nodes of the flip-flop [96].

The GBTX ASIC protects the data being transmitted and received through the optical fibres for bursts of errors using a Reed–Solomon FEC code [61]. The code is built by interleaving two Reed–Solomon RS(15,11) [60] encoded words. Each of the interleaved code words, built from 4-bit wide symbols, is capable of double error correction. In practice this means that a sequence of up to 16 consecutive erroneous bits can be received error free.

The use of FEC codes comes at the cost of reduced payload (user bandwidth). In the GBTX, 32 FEC bits are added to the 88 payload bits thus resulting in a code efficiency of 70% (if the frame header bits are accounted for). Given the high level of protection achieved, this was considered acceptable mainly when taking into consideration that the standard 8B/10B line coding [88] has an efficiency of 80% but provides no error correction ability. In the GBTX data DC balance (guaranteed by the 8B/10B code) is achieved through scrambling thus having no further impact on the user bandwidth [61].

The GBTX was qualified for the LHC upgrades environment trough X-ray and heavy-ion irradiation. For SEEs the error rates were estimated for some of the CMS detector environments [97]. During SEE testing it was observed, once again, that PLL unlocks tend to dominate the SEE response of transmitters and transceivers.

The GBLD laser driver [98] was designed to be driven by the GBTX and to be integrated in the VTRx and VTTx optical modules [64]. The challenge in designing rad-hard EEL/VCSEL drivers are the low voltage power supply requirements of sub-μm technologies and the large voltages swings needed to bias and drive laser-diodes and VCSELs. Radiation damage on laser-diodes and VCSELs tends to increases the threshold voltage needed to forward bias the lasers [84] making the matters worse. The 130 nm CMOS technology used to build the GBLD does not allow for supply voltages exceeding 1.5 V supply for the thin oxide transistors and up to 2.5 V for the thick oxide devices. High speed operation demands the use of thin-oxide devices while high voltage the use of thick-oxide. For the GBLD it was decided to power the output stage at 2.5 V to be able to efficiently drive the laser. However the thick oxide devices are slow and too sensitive to ionizing radiation (see e.g., [99]). An early version of the GBLD [98] used thin oxide devices in the output stage isolated from the 2.5 V supply by a thick oxide NMOS cascode stage (where their lower speed has a small impact). The strategy proved successful from the point of view of speed and voltage tolerance but the current driving ability of the device degraded by 30% at 1 MGy TID due to the threshold voltage shift of the thick oxide transistors. For the production version of the ASIC it was then decided to build the output stage using thin-oxide transistors only. Compatibility with the 2.5 V supply was still achieved with a cascode topology that ensured that the thin oxide devices would never experience more than 1.5 V voltage drops across their terminals [100].

The transimpedance amplifier designed to be integrated in the VTRx optical module and drive the GBTX high speed serial input is the GBTIA [63].

As for the PIN-receivers previously discussed (DORIC, RX40) major design challenges reside in handling the radiation damage of PIN diodes (decrease of R and increase of I_d) [84]. This requires both high sensitivity and preventing the dark current from saturating the preamplifier. In the GBTIA the strategy adopted was to AC couple the PIN-diode to the transimpedance preamplifier thus deviating the DC dark current from the input of the preamplifier. The PIN-diode and its bias circuit form with the coupling capacitance a high-pass network. This is undesirable since the low-cutoff frequency introduces DC wander in the signal, and thus intersymbol interference, degrading the BER. To avoid this an adaptative bias network was used that automatically adjusts to the dark current maintaining high impedance (compared with the preamplifier input impedance) while at the same time providing a reverse bias voltage that maintains the PIN diode inside its optimal bias zone [101]. The low cutoff frequency obtained was demonstrated not to degrade the BER when used with the GBTX frame encoding (FEC + scrambling). For good Power Supply Rejection Ratio (PSRR) the GBTIA was designed as a full differential circuit.

For SEE testing the GBTIA was integrated with a commercial 60 μm InGaAs photodiode in a Receiver Optical Sub-assembly (ROSA). The

work reported in [102] has shown that, when irradiating the ROSA with 63 MeV proton beam, that the majority of SEE can be attributed to particle hits on the photodiode, with only a small fraction attributed to the preamplifier. The SEEs can produce multiple-bit upsets (bursts) but all errors that occurred during the experiment were corrected by the GBTX FEC encoding. The assembly was shown to operate error free with a particle flux of $1.8 \times 10^8 \mathrm{p/cm^2/s}$.

4.2.2. Laser driver array

An 8 channel VCSEL driver array was designed for the ATLAS insertable B-Layer for the ATLAS Pixel upgrade [103]. The device (fabricated in 130 nm CMOS) was designed to drive a VCSEL array and is capable of operation at 5 Gbps per channel. It addresses concerns of reliability of VCSELs. The priority was to ensure that transmission could be maintained even in the event of multiple VCSEL failures in the VCSEL array. To achieve this objective the device is designed as 12-channel driver with 8 electrical inputs. In the event of one or multiple VCSEL failures, data can be rerouted to one of the spare channels. This is done under the control of a serial interface and given the multiplicity, 8-electrical to 12-optical channels, can cope with up to 4 failing VCSELs.

4.2.3. Gigabit wireline transmitter

The move by the LHCb collaboration to adopt a trigger-less readout pushed further the bandwidth requirements of the serial ports in the front-end ASICs. The VeloPix ASIC [104], developed for the Phase I upgrade of the Vertex Detector, requires a bandwidth of 20.48 Gbps for data readout. This was higher than what it was provided by the serializers previously developed in the community. The solution adopted was to include in the VeloPix four serializers operating at 5.12 Gbps achieving an aggregated bandwidth of 20.48 Gbps [20]. In order to minimize the power consumption, the VeloPix serializers avoid the use of a PLL running at the bit rate (or half rate). Instead, the circuit starts from a low frequency clock (in this case 320 MHz) and uses a DLL locked to this frequency, to generate 16 phase-shifted versions of the clock. These phases are further combined to generate non-overlapping signals that act as the select signal of a combinational logic multiplex. The serialized data is driven out of the ASIC using an 100 Ω line driver that implements capacitive pre-emphasis.

4.2.4. Engineering resources

The availability of the 130 nm technology enabled the design of multi-Gbps communications ASICs and allowed higher complexity to be embedded in the HEP ASICs in general and the communication ASICs in particular. The complexity extends to all the phases of the projects from design, verification, testing to user support. With the development of the second generation ASICs the HEP community became aware that designing ASICs with such advance technologies was no longer a matter for small teams but required a wider effort in the community and extends well beyond the production of wafers. The development of the GBTX is a good example with the involvement of 4 institutes and more than 20 engineers across all the activities (from design to user support). For the first time a user support team was put in place that was in charge of answering users questions, helping integrating the ASIC in the detector system and providing demonstration system hardware [105]. Moreover, the notion of design reuse, long established in industry, also gained strength in the HEP community. This took the form of sharing of digital radiation-tolerant libraries, I/O cells and even more complex functional devices like, e.g., the integration of the GBTX serializer and PLL in a serializer ASIC for the transmission of trigger data in the upgraded ATLAS Forward Muon Spectrometer [106,107].

4.3. Third generation ASICs

The complexity of the designs continued to grow with the next generation of ASICs developed in 65 nm CMOS with the design teams expanding in number of engineers and institutes involved. A well know example in HEP is the RD53 collaboration [108] and, in the domain of communication ASICs, the lpGBT collaboration is another having required the involvement of 6 institutes with an engineering team exceeding 30 collaborators.

The third generation of HEP communications ASICs has now (2022) either reached production or it is in the final phase of the prototyping stage. These devices will be installed in the experiments during the phase II upgrades with the systems commissioning taking place between 2026 and 2028 (LS3). The ASIC developments essentially target the ATLAS and the CMS detector systems with the strongest constraints coming from the Trackers and Pixel detector environments. The main goals were the development of low power devices, capable of working in rad-hard environments (that can reach 10 MGy for the innermost detectors[1]) and with bandwidths of 10 Gbps per optical fibre.

4.3.1. The lpGBT chipset

To address those requirements the VL and GBTX (chipset) concepts evolved into the VL+ and lpGBT chipset [21,26]. Besides the natural evolution to higher bandwidths (10 Gbps) these developments better matched the asymmetry of the bandwidths required for the down and uplinks. These led to the VTRx+ optical module adopting a five channel architecture with 4 channels dedicated to the uplink, with a bandwidth of 10.24 Gbps per fibre, and a single channel dedicated to the downlink, receiving data at 2.56 Gbps. The GBTIA [101] was retained for the PIN-receiver in the VTRX+ and a 4-channel 10.24 Gbps VCSEL driver was developed and radiation qualified up to 3 MGy [109].

To achieve the target data rates (10.24 Gbps), radiation tolerance (2 MGy) and low power consumption, a 65 nm CMOS technology was chosen [31]. This choice allowed, e.g., the lpGBT to achieve a quarter of the power consumption of its predecessor, the GBTX, with the double of the bandwidth and with enhanced functionality (many of the slow control and environment monitoring functions like, clock phase shifting, voltages and temperature measurements, that were implemented in the previous generations by ASICs like the PHOS4 [15], the DCU [110] and the GBT-SCA [94] were also included in the lpGBT).

Hand-in-hand with the potential for high speed goes the ability to provide low phase-noise reference clocks to the detectors. The lpGBT achieves a phase noise < 2 ps RMS [111] making the circuit attractive for timing detectors like the ATLAS MIP Timing Detector (MTD) and the CMS High-Granularity Timing Detector (HGTD). Such low phase-noise was achieved by operating the PLL/CDR circuit at 5.12 GHz and employing an LC VCO [56]. Moreover, the chip uses a modified Varactor biasing topology reducing by two orders of magnitude the SEE cross-section on this circuit element [55,56]. Measurements made with heavy-ion irradiation show that loss-of-lock free operation can be achieved even with the highest LET ions used during the SEE experiment (Ni, LET = 20.4 MeV/mg $\mathrm{cm^2}$) leading to a limit cross section $< 7.4 \cdot 10^{-8}$ $\mathrm{cm^2}$ for the losses-of-lock. With those basically eliminated from the SEE response, it was possible to probe further into SEE phenomena on PLLs and experimentally demonstrate that even the inductor (L) in the LC VCO is susceptible to SEEs [57] leading to small phase jumps of the VCO signal: 400 ps for the highest LET heavy ions used (Ni) and less than 40 ps for 200 MeV protons. These effects are however small and have no impact on data transmission.

[1] Although TID is expected to reach as high as 10 MGy for the innermost detectors, optoelectronics devices cannot be placed in those environments. As a consequence, the TID radiation hardness specification for the companion ASICs was set to 2 MGy.

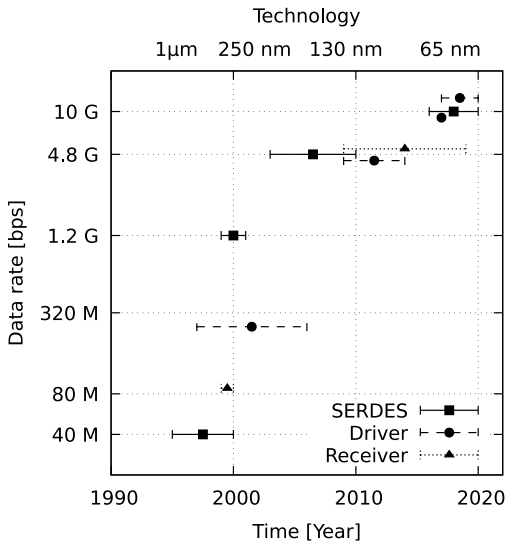

Fig. 4. Data rate evolution.

4.3.2. The GBCR2

In tandem with the bandwidths achieved between on and off-detector systems, the bandwidths between the front-ends and the transceivers have proportionally increased reaching 1.28 Gbps in the case of the lpGBT. To avoid placing the optoelectronics devices in the high-radiation environment of the pixel detectors, the ATLAS and CMS pixel ASICs (RD53) [112] will send data to the lpGBT at 1.28 Gbps over low-mass AWG34 Twinax cables. Low mass cables are needed to conform with the detectors mass budget but at 1.28 Gbps transmission can be impaired by Inter-Symbol-Interference (ISI) due to the low bandwidths of those cables. The problem is particularly acute in the case of ATLAS since the cables can span up to 6 m. The lpGBT provides programmable equalization for its e-links but not sufficient to handle the highly bandwidth limited case of the ATLAS detector. To address this, the GigaBit Cable Receiver (GBCR2) was developed [113]. The GBCR2 will receive data from cables with lengths between 3 and 6 meters and will provide a programmable amount of equalization that matches the bandwidth of the cable. It consists of a programmable Continuous Time Equalizer followed by a re-timer circuit that optimally re-samples the data using the 1.28 GHz clock provided by the lpGBT.

5. Current research

The 2021 ECFA detector research and development roadmap [114] identifies research areas that are particularly relevant for the developments of future HEP data links. Among those are the development of high data rate and low power ASICs (and thus systems), the exploration of emerging technologies like Silicon Photonics (SiPh) and the investigation of the radiation tolerance of advanced CMOS technologies that will enable achieving data rates in excess of 28 Gbps per fibre or lane.

Fig. 4 shows that the adoption of finer feature technologies with time has enabled the development of higher bandwidth HEP ASICs and links. Hidden in this picture is also the fact that the move to more advanced technology nodes has allowed the community to build ASICs which achieved higher degrees of radiation hardness with the most recent generation routinely tolerating several MGy. With its radiation hardness still being actively assessed, the HEP community is currently exploring a 28 nm CMOS technology [33] which should allow the development of ASICs operation at several tens of Gbps.

Among the current challenges to move to higher data rates, are the contradictory requirements between the need for relatively high voltages to bias correctly PIN-diodes, EELs and VCSELs (of the order of a couple of Volts) and the low voltages (less than a volt) required by the modern technologies to achieve both reliability and low power operation. One of the solutions envisaged is the use of a charge-pumps to locally boost the ASIC supply voltages to the voltages needed to bias the PIN-diodes and VCSELs. Using this concept a 10 Gbps quad VCSEL driver [115] and a 10 Gbps quad PIN-receiver [116] were demonstrated in a 65 nm CMOS technology that implement charge pumps to generate the bias voltages needed for the VCSELs and PIN-diodes, respectively.

Although laser drivers operating at 25 Gbps have already been demonstrated in the community [117] it is unlikely that direct modulation of VCSELs will be able to achieve much higher bandwidths. To overcome this limitation the telecommunications industry has been either adopting the use of external modulators, e.g. Mach–Zehnder or ring modulators, or the use of higher order modulation formats. In HEP both solutions are being studied with a Pulse Amplitude Modulation with 4 levels (PAM-4) transmitter demonstrated to work at 20 Gbps (10 GBd) [118]. Such an approach is expected to enable 56 Gbps transmission when implemented in a 28 nm CMOS technology.

To address the challenges present in the analogue components, all-digital PLL/CDR architectures were proposed demonstrating a superior single-event effect (SEE) tolerance [119,120].

SiPh offers the potential of yet higher bandwidths by combining in the same silicon wafer external modulators and wavelength-division multiplexing elements. Research is already ongoing on making these components radiation hard [121–124] and they are expected to play a major role in future HEP links.

6. Conclusions

ASICs have made possible the construction of the LHC detector experiments. A good fraction of those were communications ASICs developed for the rad-hard optical links. They spanned bandwidths from a modest 40 Mbps to 1.6 Gbps in the LHC experiments with radiation tolerances requirements reaching 0.1 MGy. The LHC upgrades (phase I and II) pushed the bandwidths to 5 and 10 Gbps per fibre with radiation specifications up to 2 MGy. All this was in turn made possible by the adoption of carefully selected and radiation-qualified CMOS technologies and, to the largest extent, by the use of sub-µm CMOS commercially available technologies (250 nm, 130 nm and 65 nm). The community learned how to profit from those resources and successfully produced the ASICs described in this paper in the context of the LHC and its upgrades (HL-LHC). New detector systems are now conceived [114] that will certainly push communications ASICs to even higher bandwidths and radiation hardness. In anticipation, CERN and its collaborating institutes are already looking ahead and exploring the radiation hardness of 28 nm CMOS and aiming at the development of > 28 Gbps ASICs.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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