EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE

CERN - PS DIVISION

PS/ RF/ Note 95-07

TUNING LOOP PROGRAMS
(PS/RF-HC 3192)

M. Paoluzzi

Geneva, Switzerland
15 March 1995

1. INTRODUCTION

The 'Tuning Loop Programs' module is a triple 10-bit frequency to voltage converter. One channel provides linear f-v conversion while for the other two channels the conversion functions are stored in EPROM memories.

Four memory pages, corresponding to four frequency ranges, are available for storing different conversion functions and can be selected from the front panel.

The output of the linear f-v converter is used to generate a frequency error signal in case the input frequency or its variation vs. time exceeds the selected limits

A dedicated program (PROG3192.PAS) allowing easy generation of the data required for programming the memories has been developed and can be found in the documentation.

2. CIRCUIT DESCRIPTION

The Tuning Loop Programs block diagram is shown in Figure 1 and the complete circuit diagram is included in annex.

The rf signal present on the RF IN connector is amplified and applied to IC4 which counts the number of cycles occurring in a fixed time so as to generate a 10 bit digital frequency word. The accepted input rf signal amplitude is 0.35 to 1.4 V peak.

The count time window is generated by the 5.068 MHz crystal oscillator and the frequency divider (IC7 , IC8).

The dividing ratio depends on the frequency band and memory page selection code generated by the decoder (IC4) according to the status of SK7, SK8, SK9 and SK10.

Frequency range selection is done by pulling down the required input. In case more than one input is low, the lower range is selected whilst if all inputs are high the 10 MHz range is active.

At the end of the counting time the digital frequency word is latched (IC5, IC25) and transferred to the digital to analog conversion circuits.

For the linear frequency to voltage conversion the digital frequency word is directly converted into its analog value by IC13 and thus scaled, filtered and buffered (IC16, IC19, IC24) before being applied to the output (SK1).

In the other two cases the digital frequency word is used to address two EPROM couples (LSB and MSB - IC9, IC10, IC26, IC27) into which the conversion function is stored. The memory data are then applied to the digital to analog conversion circuitry (IC14, IC15, IC20, IC21, IC22, IC23).

The following table gives the address range of the four memory pages.

Memory Page	Selected Full Scale	Memory Address
1	2.5 MHz	0 - 1023
2	10 MHz	1024 - 2047
3	5 MHz	2048 - 3071
4	20 MHz	3072 - 4095

The full scale output voltage is 10 V for the Gain Program Output (SK6), 5 V for the I Program Output (SK5) while the Frequency Output is scaled so as to obtain 10 V at the rated full scale frequency.

The circuits built around IC17 and IC18 generate an error signal in case the frequency or its rate of change vs. time exceed the limits set by corresponding pots.

The frequency error signal is intended for protection purpose.

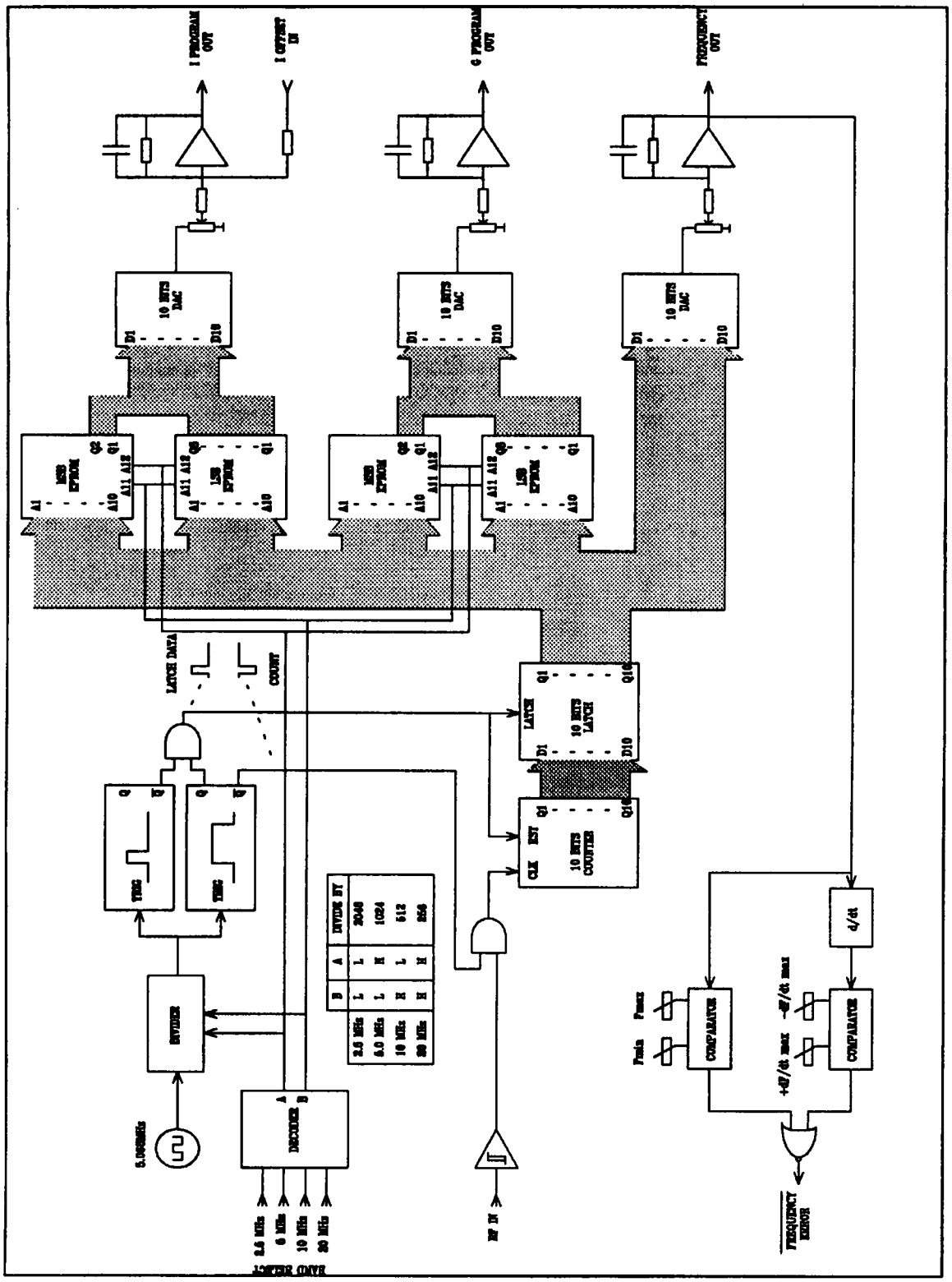

Figure 1. - Tuning Loop Programs Block Diagram.

3. ADJUSTMENT

For the adjustment of the module two EPROM couplets containing the adjustment functions defined in Figure 2 are required.

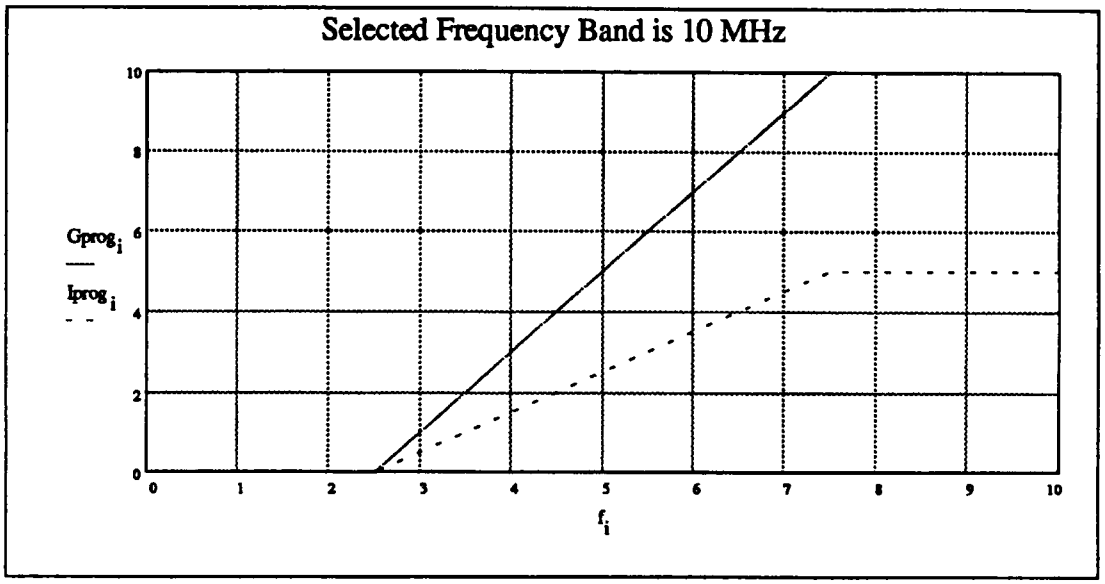

Figure 2. Adjustment Functions.

1	Preliminary Check
1.1	By visual inspection verify that the module does not present evident manufacture errors and verify that it has been properly cleaned.
1.2	Verify that all required supply voltage are present and adjust P1 so as to obtain on IC1 - pin 6 a voltage of 10. V +/- 0.1%
1.3	Install the adjustment EPROMs as IC9, IC10, IC16, IC27

2	Timing Block Test
2.1	Verify that the frequency of the signal at IC28 - pin 3 is 5.0685 MHz +/- 500 Hz. If necessary change C13 to the value required to obtain the correct frequency.
2.2	Verify that the frequency of the signal at IC8 - pin is 3 is : ~19.8 kHz when 20 MHz F.S. Is selected ~9.9 kHz when 10 MHz F.S. Is selected ~4.95 kHz when 5 MHz F.S. Is selected ~2.47 kHz when 2.5 MHz F.S. Is selected

3	Input Amplifier Test
3.1	Apply a 20 MHz rf signal on SK11 and verify that IC2 - pin 3 swings from 0V to >4.5 V when the input signal amplitude is > 0.35 Vp and < 1.4 Vp

4	Output Stages Offset Adjustment
4.1	Set P2, P3 and P4 at minimum (12 turns CW). Load SK4 on 50 Ω . Adjust P10 so as to obtain on SK6 0V +/- 5 mV Adjust P11 so as to obtain on SK5 0V +/- 5 mV Adjust P12 so as to obtain on SK1 0V +/- 5 mV
4.2	Load SK11 and SK4 on 50 Ω . Set P2, P3 and P4 at maximum (12 turns CCW). Adjust P7 so as to obtain on SK6 0V +/- 5 mV Adjust P8 so as to obtain on SK5 0V +/- 5 mV Adjust P9 so as to obtain on SK1 0V +/- 5 mV

5	Scaling Adjustment
5.1	Load SK4 and SK9 on 50 Ω . Apply a 10 MHz , 0.5 Vp rf signal on SK11 and : Adjust P2 so as to obtain on SK6 10 V +/- 10 mV Adjust P3 so as to obtain on SK5 5 V +/- 10 mV Adjust P4 so as to obtain on SK1 10 V +/- 10 mV
5.2	Verify that changing the rf signal frequency to 0.1 MHz the voltage on SK5 and SK6 is 0V +/- 10 mV while on SK1 the voltage is 0.1 V +/- 10 mV. If required readjust P7, P8 and P9 and then restart from point 5.1.
5.3	Load SK4 and SK10 on 50 Ω . Apply a 20 MHz , 0.5 Vp rf signal on SK1 and verify that the voltage on SK1 is 10 V +/- 30 mV Verify that changing the rf signal frequency to 2 MHz the voltage on SK1 is 1V +/- 10 mV.
5.4	Load SK4 and SK8 on 50 Ω . Apply a 5 MHz , 0.5 Vp rf signal on SK1 and verify that the voltage on SK1 is 10 V +/- 50 mV Verify that changing the rf signal frequency to 0.5 MHz the voltage on SK1 is 1 V +/- 10 mV.
5.5	Load SK4 and SK7 on 50 Ω . Apply a 2.5 MHz , 0.5 Vp rf signal on SK1 and verify that the voltage on SK1 is 10 V +/- 50 mV Verify that changing the rf signal frequency to 0.25 MHz the voltage on SK1 is 1 V +/- 10 mV.

6	Frequency Error Block Test
6.1	Set P5, P13 at maximum and P6, P14 at minimum and load SK4 and SK9 on 50 Ω . Apply a 10 MHz , 0.5 Vp rf signal on SK11 . Verify that reducing the reference value set by P5 the error indication goes active.

6.2	Set P5,13 at maximum and P6, P14 at minimum and load SK4 and SK9 on 50 Ω . Apply a 1 MHz , 0.5 Vp rf signal on SK11 . Verify that increasing the reference value set by P6 the error indication goes active.
6.3	Set P5,13 at maximum and P6, P14 at minimum and load SK4 and SK9 on 50 Ω . Apply on SK11 signal with the following characteristics : fmin = 1 MHz fmax = 6 MHz sweep mode : triangular wave sweep time 0.01 s Verify that while the generator sweeps from fmin to fmax a voltage of -5 V +/-10% is present on SK2, while when the generator sweeps from fmax to fmin the voltage is +5 V +/-10% . Verify that increasing the reference value set by P14 the error indication goes active. Verify that reducing the reference value set by P13 the error indication goes active.

7	**Labeling**
13.1	Put a drop of paint on all pots except those on front panel.
13.2	Label the module 'OK+Date'

Distribution :

R. Garoby
PS-RF-HC Section