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PWM(*) RECTIFIER WITH LOW VOLTAGE RIPPLE

FOR MAGNET SUPPLY.

D.Ciscato, L.Malesani, L.Rossetto, P.Tenti, GL.Basile, M.Pasti, F.Voelker

A collaboration has been set up some time ago, thanks to the CERN Industry and Technology Liaison Office, with the firm OCEM/Italy concerning the use of GTO devices in high performance magnet power converters.

Development is based on a 50 kW converter (170 V, 300 A) and concerns the power part as well as the related electronics, which has shown to be quite intricate. External collaborators from the University of Bologna and Padova assist OCEM in this project.

In the course of the first part of the development the attached article, treating the mode of controlling the power flow to the load, has been published in the Proceedings of the IEEE/IAS Annual Meeting, Seattle, Oct.'90.

A more specific paper on the subject, planned to be presented at the next EPE Conference in sept.'91 will report the work results and describe the elaborate pulse modulation and regulation scheme under development.

The subject is of great interest for the design of high power converters which are mains friendly and have excellent performance. Accordingly the present Note should keep the people working in the field informed.
It is expected that the PS/PO group will have the opportunity to specify and order a first power converter based on this modern technology in the near future, in view of a wider application in the frame of the LHC project.

(*) Pulse Width Modulation

F.Voelker

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PWM RECTIFIER WITH LOW DC VOLTAGE RIPPLE FOR MAGNET SUPPLY

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Abstract

PWM bridge rectifiers with GTO switches are considered for application to magnet supplies of particle accelerators, where extremely low DC current ripple is required.

Different control strategies, both with pre-programmed and variable switching patterns, are examined and compared in view of the optimization of the system performance. In particular optimum digital PWM, multi-level delta modulation, and hybrid PWM/delta techniques are analysed.

The validity of the control methods is verified by simulation and by experimental tests on a 60 kW prototype.

Introduction

Power supplies for magnets of particle accelerators are usually required to give extremely smoothed DC currents, the allowed current ripple being in the order of 0.01% of the DC component. On the other hand, typical power ratings being in the order of hundreds or thousands of kVA, thyristor rectifiers are normally used. Accordingly, heavy output filters (passive, active, or both) are needed to fulfill DC current ripple specifications. Moreover, provisions to compensate for input reactive power and current harmonics may also be needed in order to comply with the AC supply requirements.

More modern solutions are based on PWM-controlled GTO rectifiers, which can considerably improve the system performance, both on load and supply side. In fact, neglecting the modulation harmonics, ripple-free DC voltages and sinusoidal in-phase AC currents are theoretically possible *[2]*. In practice, since maximum switching frequency of GTOs is constrained below 1÷2 kHz, the modulation process affects both input and output waveforms, calling again for AC and DC filters. However, size of the filters depends strongly on the modulation strategy implemented in the converter control.

In this paper, suitable PWM techniques are analysed and compared. Theoretical results are then verified on a full-size prototype.

System configuration and basic operation

The basic system configuration is shown in Fig.1. It includes a PWM bridge rectifier, made up of six unidirectional fully-controlled switches, input and output filters, and ohmic-inductive load.

For the application being considered, where the DC current has to be controlled both during rise and fall phases, positive and negative load voltages are required. Thus, taking into account the inductive load, impressed-current schemes like that of Fig.1 offer the only single-stage solution of the problem.

Since the converter is seen from the AC supply as a pulse-width-modulated current generator, capaci-

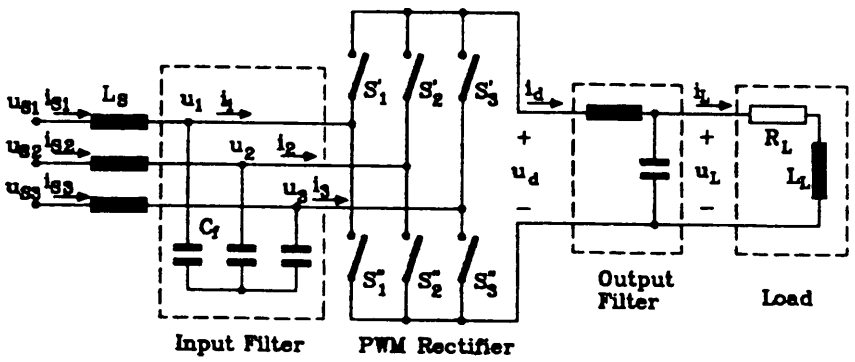

Fig.1 - System configuration

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tive input filters C_f are needed to limit the input voltage ripple due to line inductances L_s.

Moreover, an output filter may be needed to comply with the DC current ripple specifications.

Taking into account that the switches are reverse blocking, for proper converter operation one (and only one) switch in the upper and lower half-bridge must be closed at any time. Thus, let x_i' and x_i'' (i=1÷3) be respectively status signals (1=on, 0=off) of upper switches S_i' and lower switches S_i'', we can write:

$$x_1' + x_2' + x_3' = 1 \qquad (1.a)$$

$$x_1'' + x_2'' + x_3'' = 1 \qquad (1.b)$$

Depending on which switch pair is closed, rectified voltage u_d can coincide with any line-to-line voltage or can be zero (free-wheeling status). The general expression of voltage u_d is:

$$u_d = (x_1' u_1 + x_2' u_2 + x_3' u_3) - (x_1'' u_1 + x_2'' u_2 + x_3'' u_3) \qquad (2)$$

where u_1, u_2, u_3 are converter input voltages.

Define now status signal x_i of the i-th bridge leg as:

$$x_i = x_i' - x_i'' \qquad (3)$$

which equals 1 if upper switch S_i' is on, -1 if lower switch S_i'' is on, 0 if both switches are on or off. Accordingly, Eq.2 can be rewritten as:

$$u_d = x_1 u_1 + x_2 u_2 + x_3 u_3 \qquad (4)$$

Similarly, converter input currents may be expressed in dependence of output current i_d as:

$$i_1 = (x_1' - x_1'') i_d = x_1 i_d \qquad (5.a)$$

$$i_2 = (x_2' - x_2'') i_d = x_2 i_d \qquad (5.b)$$

$$i_3 = (x_3' - x_3'') i_d = x_3 i_d \qquad (5.c)$$

Note that, at a given time, only two converter legs can be modulated independently, the third being constrained by Eqs.1. This, however, does not cause any practical limitation, since controlling the waveforms of two line currents necessarily implies the waveform produced by the third leg, which also acts as a free-wheeling path.

Neglecting the high-frequency modulation harmonics, Eqs.2 and 3 may be rewritten in the form:

$$u_d = \sum_1^3 i \; m_i u_i \qquad (6.a)$$

$$i_i = m_i i_d \qquad \text{for} \quad i = 1 \div 3 \qquad (6.b)$$

where m_i are modulation laws of the converter legs, i.e. time-averaged values of status variables x_i.

Eqs.5 show that, in the ideal case of sinusoidal and symmetric supply voltages and assuming ripple-free DC current (the load time-constant L_L/R_L being always quite high in our applications), the PWM converter can be controlled so as to obtain sinusoidal and in-phase input currents. For the purpose, sinusoidal and symmetric modulation laws must be adopted, which also give ideally smoothed output voltage *[2]*.

In practice, due to supply inductances L_s, actual converter input voltages may become distorted. This affects the DC voltage ripple if sinusoidal modulation laws are maintained. On the contrary, correcting the modulation laws so as to compensate for the AC voltage distortion gives ripple-free DC voltage, but the AC current waveforms are worsened.

In the following, both control strategies which lead to optimum input behaviour (sinusoidal in-phase currents) and optimum output behaviour (ripple-free DC voltage) are examined.

Control strategy for optimum input behaviour
Digital PWM (Minimum harmonic contents)

In our application, due to the quite large time-constant of the load, ideally smoothed DC current can be assumed. Thus, digital PWM techniques based on off-line calculation of optimum switching patterns *[4]* can be adopted in order to optimize the AC system behaviour.

Control scheme

Fig.2. shows a control scheme implementing the digital modulation.

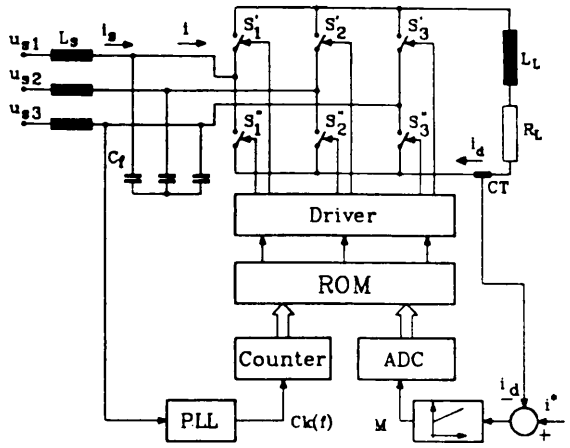

Fig.2 - Digital PWM control

A DC current error amplifier determines modulation index M, which is converted to digital and sets the most significant bits of the address of a memory location where the switching patterns are stored. The less significant bits are generated by a counter, driven by clock signal Ck(f) generated by a PLL. This latter acts as a frequency multiplier producing the desired clock frequency (sampling frequency f_s). Accordingly, the memory contents is cyclically explored and the switch status signals, corresponding to the desired output voltage level, are updated at a frequency f_s and transmitted to the switch drivers.

For a given number of commutations per period this modulation strategy allows, in theory, optimum input and output converter performance. For this kind of application, where DC current is well smoothed, the usual optimization criterion is to minimize the total harmonic contents of the AC currents. If the AC voltages are sinusoidal and symmetric, this criterion also gives low harmonic contents of the DC voltage.

However, since AC voltage distortion and unbalance are generally non negligible *[5]*, this kind of control involves good input behaviour (low reactive power, high power factor), but causes some DC voltage distortion, which generally affects the output filter design.

Moreover, due to the cyclic operation, the DC voltage and AC current spectra can exhibit non-negligible harmonic components at frequencies which

are multiple of the line frequency.

With this technique the phase of the AC currents can be controlled (e.g. to compensate for reactive power absorbed by input filter capacitors) by advancing or delaying the phase signal driving the PLL.

Computation algorithms

Switching patterns minimizing the total harmonic contents of supply currents i_s were computed by taking into account the transfer function of the input filter.

In order to eliminate the even harmonics, switching patterns symmetric with respect to T/4 (T is period of the AC voltages) and antisymmetric with respect to T/2 were chosen.

According to the Fourier analysis, the rms values of the line current harmonics are given by:

$$I_n = \frac{4\sqrt{2}}{T} \int_0^{T/4} i(t) \sin(2\pi n f t)\, dt \qquad (7)$$

where n is harmonic order, i(t) is time behaviour of the generic line current (i_1, i_2, i_3), and f is line frequency.

In our case, i(t) is a sampled variable which can only assume values 0, $+I_d$ or $-I_d$ (I_d is converter DC current) depending on status of the corresponding bridge leg. The equation above can therefore be rewritten as:

$$I_n = \frac{2\sqrt{2}}{\pi n} I_d \sum_{1}^{K} x_k \left[\cos\left(\frac{n\pi}{2} \frac{k-1}{K}\right) - \cos\left(\frac{n\pi}{2} \frac{k}{K}\right)\right] \quad \text{for} \quad \begin{matrix} n = 6j \pm 1 \\ j = 1 \div J \end{matrix} \qquad (7'.a)$$

$$I_n = 0 \qquad \text{otherwise} \qquad (7'.b)$$

where K is number of samples per quarter of period, and x_k (k=1,K) is the switching pattern.

Let F_n be the AC filter gain at a frequency n·f, the supply current harmonics become:

$$I_{sn} = F_n I_n \qquad (8)$$

and the optimization is obtained by selecting the switching patterns so as to minimize the function:

$$\sigma^2 = \sum_{2}^{N} I_{sn}^2 = \sum_{2}^{N} F_n^2 I_n^2 \qquad (9)$$

Of course, the computation must be repeated for all desired levels of the DC voltage.

In practice, in order to ensure symmetry between the phases, the switching pattern can be chosen independently only in the interval $\pi/6 \div \pi/2$. For the same reason, number N_s of samples per period must be divisible by six.

Harmonic spectra

As an example of application, the control technique discussed above was applied to the cases of f_s = 2100 Hz (N_s = 42) and f_s = 3300 Hz (N_s = 66), 50 Hz being the line frequency. The corresponding numbers of independent commutations per sixth of period are respectively 7 and 11, the maximum switching frequencies being 1050 and 1650 Hz.

The optimum switching pattern was obtained, for 256 DC voltage levels, by an exhaustive analysis of all possible solutions (128 per output voltage level in the first case, 2048 in the second). More precisely, reference was made to modulation index M, which is related to DC voltage amplitude, and is defined by:

$$M = \sqrt{2}\, I_1 / I_d \qquad (10)$$

where I_1 is rms value of the fundamental component of line current i(t).

Typical harmonic spectra of supply currents and DC voltage are shown in Fig.3 as obtained by simulation (assuming f_s = 3300 Hz, F_n = 1/n and sinusoidal input voltages).

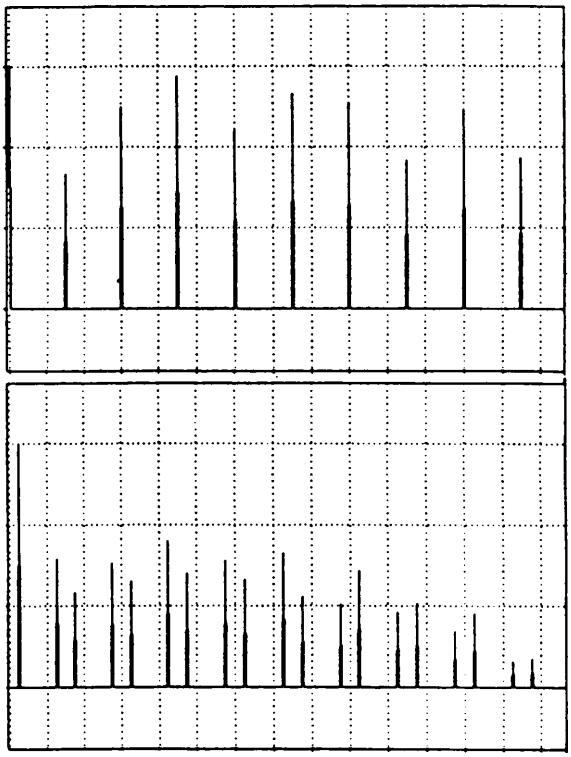

Fig.3 - Simulated results with optimum switching pattern (N_s=66, M=0.25, 200 Hz/div, 20 dB/div)
top: Harmonic spectrum of converter output voltage
bottom: Harmonic spectrum of supply current

It is noticeable that, in spite of the low switching frequency (typical of the GTOs), the total harmonic contents (σ) of the supply currents is very reduced even for small values of the modulation index. The dependence of σ on M is shown in Table I.

Switchings per per period N_s	Modulation Index M	Total Harmonic Contents σ/I_1
42	0.25	20.3
	0.50	13.5
	0.75	6.2
	1.00	6.6
	1.05	27.8
66	0.25	10.4
	0.50	7.2
	0.75	4.6
	1.00	3.0
	1.05	21.6

Table I - Results for optimum PWM
Total harmonic contents of the AC current
(per cent value of the fundamental component)

Control strategy for optimum output behaviour
Delta modulation

Improving the converter output behaviour in presence of high AC voltage distortion, so as to meet the DC current ripple specifications, calls for closed loop control techniques, which perform on-line control of the switching pattern.

In particular the delta modulation technique *[3]*, giving more uniform harmonic distribution with smaller amplitudes of individual harmonics, is suitable for our application.

Control scheme

Operation of the converter controlled by the delta modulator can be described by means of the general scheme of Fig.4.

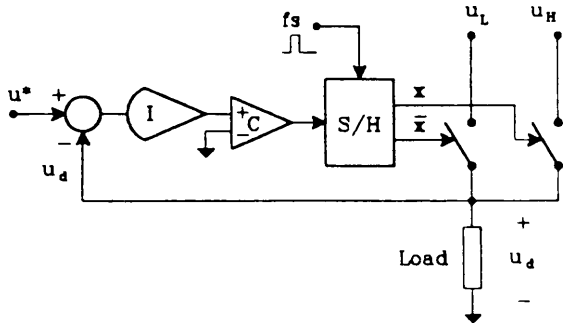

Fig.4 - Basic scheme of delta modulator

Instantaneous voltage u_d is obtained by switching the converter output between suitable line-to-line voltages u_H (higher than DC voltage reference u*) and u_L (lower than u*). For the purpose, voltage error signal u^*-u_d is fed to an integrator whose output is compared to zero. The comparator output is then sampled at a frequency f_s giving status signal x which determines whether voltage u_H or voltage u_L has to be applied to the load.

An external current loop controls u* providing the required current accuracy. The cascade scheme has the advantage of fast voltage control, able to compensate for low-order ripple harmonics due to AC distortion and unbalances.

As compared to the digital PWM, this control technique causes optimum output converter behaviour, since the integral of the output voltage error is minimized irrespective of the AC voltage waveform.

Instead, the AC current spectrum is worsened. In fact, the delta modulator performs the on-line evaluation of the switching pattern so as to compensate for the AC voltage distortion. This means that in Eqs.6 the modulation laws are generally not sinusoidal. Thus the line currents become as more distorted as higher the AC voltage distortion.

Control strategies

Due to the bridge converter configuration, converter output voltage u_d can actually be modulated between seven different values (six line-to-line voltages and zero). Accordingly, different control strategies can be devised, depending on which voltage pair is assumed as u_H-u_L, giving different converter performances.

The complete control scheme is shown in Fig.5.

Given converter input voltages u_1, u_2, u_3 and DC voltage reference u*, the Upper Voltage Selector (UVS) determines which, among the seven possible output voltages, is voltage u_H; more precisely, UVS selects the pair of converter switches which must be closed to give voltage u_H (corresponding status signals are set to 1, the other being zero).

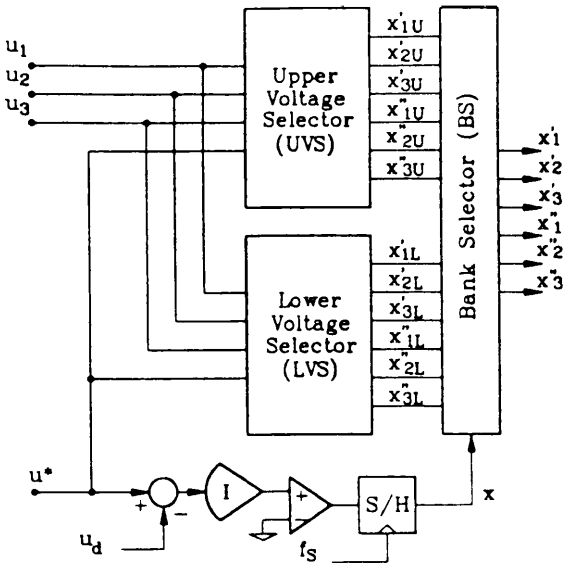

Fig.5 - Multi-level delta modulator

Similarly, the Lower Voltage Selector (LVS) choses voltage u_L.

Then, at any clock signal, voltage u_H or voltage u_L is applied to the converter output depending on status x of the delta modulator. This is done by the Bank Selector (BS), which is easily implemented by logic circuitry.

Minimization of output voltage ripple. Output voltage (and current) ripple is minimized by modulating u_d, at any time, between those line-to-line (or zero) voltages which are the closest (respectively higher and lower) to reference u* (optimum multilevel control, *[1]*).

For the purpose, UVS, LVS and BS are easily implemented by a set of comparators (comparing line-to-line voltages and reference u*) and a read-only memory, addressed by status signals of the comparators and by status x of the delta modulator. The memory output, which is sampled at each clock pulse, controls directly status of the converter switches.

This technique has the drawback that the modulation laws, which are determined - at a given time - by the relative amplitudes of DC voltage reference and line-to-line voltages, are generally non sinusoidal. They can also become unsymmetric in presence of AC voltage distortion or unbalance. Thus, the line current spectrum is worse as compared with the case of digital PWM.

However, since the conduction intervals of each converter leg are symmetric with respect to the corresponding line voltage, the converter input currents remain in-phase in all operating conditions. Thus, the reactive power absorbed by the filter capacitors cannot be compensated.

Simplified implementation. An alternative solution, which gives similar results with simpler control circuitry, is to modulate voltage u_d between zero and maximum instantaneous line-to-line voltage (positive or negative, depending on polarity of reference u*).

In this case, assuming that the AC voltages are moderately distorted, blocks UVS, LVS and BS can be implemented by a single memory adressed by a counter driven by a PLL (similarly to the scheme of Fig.2). In fact, only a phase signal is needed to establish which line-to-line voltage is maximum at a given time.

As an additional advantage, reactive power control can be achieved by adding to the PLL phase signal an offset generated by a power factor control loop.

Typical simulated DC voltage and AC current spectra are shown in Fig.6.

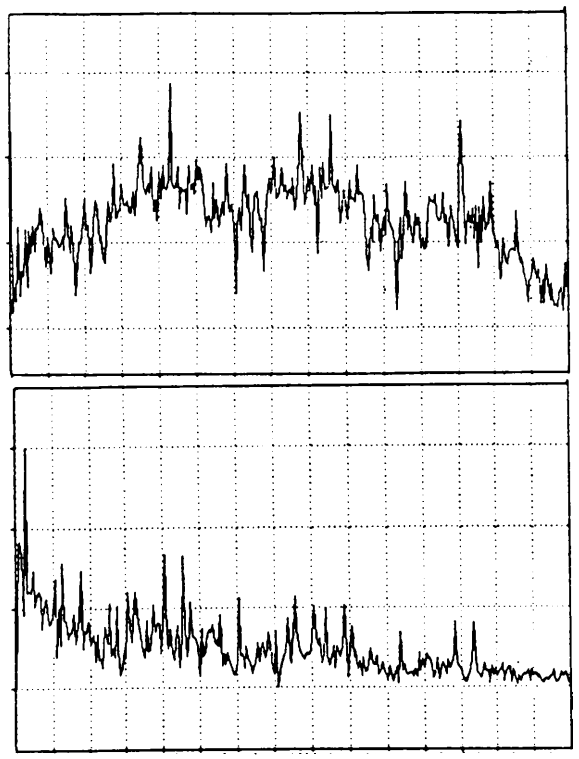

Fig.6 - Simulated results with delta modulation (simplified implementation, f_s=1650 Hz, M=0.25,200 Hz/div,20 dB/div)
top: Harmonic spectrum of converter output voltage
bottom: Harmonic spectrum of supply current

Multi-sampled delta modulation

Delta modulation techniques allow good response and small harmonics of the controlled variable and are easy to implement by digital techniques. However the switch-on and switch-off times are necessarily multiple of the sampling period. Thus, low-frequency voltage and/or current harmonics may appear when the duty-cycle approaches 0 or 1.

In order to overcome this problem, a multi-sampled technique was investigated, in which each sampling period T_s is further subdivided into N_i sub-intervals of duration T_i.

With this technique the comparator status is sampled at the beginning of each interval T_s, giving control signal x which selects the initial converter output voltage (u_H or u_L). The comparator status is then sampled again at the beginning of each sub-interval T_i and the converter output is switched (from u_H to u_L or vice-versa) as soon as x changes. After changing status, signal x is kept constant until sampling period T_s ends.

As a result, the converter changes status only once per sampling period, but the duty-cycle accuracy is increased by N_i times as compared to the usual delta modulation.

Of course, increasing N_i makes the converter operation more and more similar to that of ramp-comparison PWM controls.

This approach, which can be adopted irrespective of the control strategy, fits very well with the capabilities of GTOs. In fact, T_s can be chosen to comply with maximum switching frequency limitations, while T_i can be selected so as to ensure the specified minimum on and off times.

With this technique, the low-order harmonics of the output voltage remain small even for very low DC voltage levels.

Experimental results

Converter specifications

A three-phase bridge converter with unidirectional GTO switches has been developed with following specifications:

AC input voltage (line-to-line)	150 V ± 10%
DC voltage (resistive drop)	170 V
DC current	300 A
DC current accuracy (including ripple)	≤ 0.01 %
Load time constant	≈ 15 ms
AC power factor	≥ 0.9
Efficiency	≥ 90 %

These requirements are typical of converter modules which are currently studied within a joint research carried out by CERN and OCEM.

Due to the very stringent specification on the DC current ripple, delta and multi-sampled delta modulation techniques have been preferred. Both control strategies (minimum ripple and simplified implementation) were tested to compare their actual performance.

Basic design criteria

AC voltage. Given rated DC voltage U_{dn} and current I_{dn}, the AC voltage amplitude is easily obtained by balancing the input and output power. In the assumption of sinusoidal symmetric AC voltages we have:

$$U_d = 3/\sqrt{2}\ M\ U \qquad (11)$$

where U is rms value of the line voltage and M is modulation index, defined by Eq.10.

Modulation index. In the case of delta modulation the maximum value of modulation index M can rise up to the value corresponding to uncontrolled bridge operation:

$$M_{max} = 2\sqrt{3}/\pi \approx 1.1 \qquad (12)$$

In practice M should not exceed 1.05, in order to avoid input and output filter overrating. In fact, as the converter operation approaches that of the uncontrolled bridge rectifier, DC voltage and AC currents become considerably distorted.

AC current. The fundamental component of the AC current derives immediately from Eq.10, given M and I_{dn}, the harmonic contents being dependent on the modulation strategy. In any case, rms value I of the AC current is less than (but not far from) the value corresponding to uncontrolled converter operation. Thus:

0

$$I \leq \sqrt{6}/\pi\ I_{dn} \qquad (13)$$

Output filter design: As mentioned before, the converter behaviour is strongly affected by control strategy, AC voltage distortion and value of the modulation index (i.e. by DC voltage reference).

It results that, in the case of simplified delta modulation, the peak of the output voltage spectrum can be approximately evaluated by:

$$f_d = \frac{U_d}{U_{dmax}} f_s = \frac{M}{M_{max}} f_s$$

$$\text{for } M \leq \frac{M_{max}}{2} \qquad (14.a)$$

and:

$$f_d = \frac{U_{dmax}-U_d}{U_{dmax}} f_s = \frac{M_{max}-M}{M_{max}} f_s$$

$$\text{for } M \geq \frac{M_{max}}{2} \qquad (14.b)$$

Eqs.14 confirm that the output voltage spectrum exhibits as more low-frequency components as closer M is to 0 or M_{max}.

The corresponding value of the voltage ripple integral can be evaluated as:

$$\Phi_U = U_d(M_{max})\ T_s \qquad (15)$$

As AC voltage distortion and unbalances producing low-order harmonics in the DC output are compensated by the delta control, the passive output filter can be designed only for high-order harmonics according to Eqs.14 and 15.

Input filter design. The AC current waveform depends strongly on actual circuit parameters and controller operation. Thus input filter design has been performed by the help of simulated results.

Prototype parameters. The actual converter configuration includes input transformer (60 kVA, 10 % short circuit voltage), capacitor filters (C_f = 100 μF), GTO switches with series diode (to ensure reverse voltage blocking capability), output filter and load (R_L = 0.5 Ω, L_L = 10 mH).

GTOs type MEDL-DGT304SE10 (RCD snubber: 2.2 μF, 5 Ω-50 W), which are capable of 1 kV blocking voltage and 390 A rms current, and fast series diodes type MEDL-DSF4012ST10 (RC snubber: 0.1 μF, 10 Ω-25 W) have been used.

In order to allow broad-range experimentation, a third-order adjustable output filter was adopted, made up of a series inductance (2.5 mH) and two parallel paths (purely capacitive path: 1250 μF; ohmic-capacitive path: 1.2 Ω-5000 μF connected in series).

The maximum switching frequency (equal to $f_s/2$) has been chosen at 1.65 kHz.

Experimental results. The measured efficiency at the rated power resulted about 92 % and the AC power factor above 0.9 even in absence of provisions to compensate for the reactive power absorbed by the input capacitors.

Typical converter input and output waveforms obtained by the delta modulation technique (with simplified implementation) are shown in Fig.7, the corresponding spectra being shown in Fig.8. The correspondence with the theoretical results of Fig.6 can be appreciated.

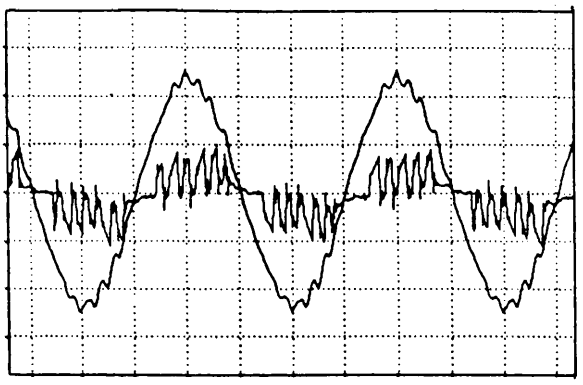

Fig.7 - Measured converter input waveforms for delta modulation with simplified implementation (f_s=1650 Hz, M=0.3, 5 ms/div, 100 V/div, 100 A/div)

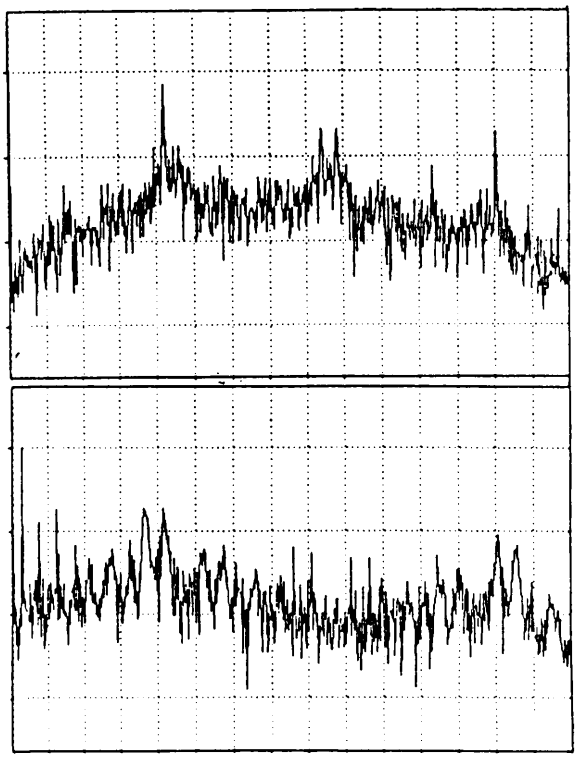

Fig.8 - Measured DC voltage and AC current spectra (200 Hz/div, 20 dB/div, same conditions as in Fig.7)

Conclusions

Control techniques aimed to optimize the behaviour of PWM rectifiers for magnet supplies were examined.

In particular, optimum digital PWM and multilevel delta modulation techniques (this latter with three kinds of control strategy: minimum output voltage ripple, simplified implementation, multi-sampled) were considered.

In theory, both solutions allow AC currents and DC voltages free of low-frequency harmonics. Control of the AC current phase is also possible (except for the minimum output voltage ripple strategy), allowing maximization of the AC power factor.

In practice, digital PWM techniques are better suitable for optimizing the AC converter performance, while delta modulation techniques give better results in terms of DC current and voltage distortion.

The theoretical results were experimented on a 60 kW prototype, demonstrating the feasibility of PWM converters with GTO switches for magnet supplies in substitution of traditional phase-controlled thyristor rectifiers.

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