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MOMENTUM STOCHASTIC COOLING WITH DIGITAL NOTCHES

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ABSTRACT

For momentum stochastic cooling at low energies (2 MeV, 5.9 MeV) in LEAR, a 200 MHz sampling rate digitizer is used to make a recurrent notch filter. Using this technology, long delay lines are obtained with good phase and amplitude characteristics. This paper describes the system and the results on stochastic cooling at a relativistic velocity factor of 0.065.

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Abstract

For momentum stochastic cooling at low energies (2 MeV,5.9 MeV) in LEAR, a 200 MHz sampling rate digitizer is used to make a recurrent notch filter. Using this technology, long delay lines are obtained with good phase and amplitude characteristics. This paper describes the system and the results on stochastic cooling at a relativistic velocity factor of 0.065.

Introduction

The CERN Low Energy Antiproton Ring (LEAR) decelerates antiprotons down to a momentum of 105 MeV/c and eventually to 61.2 MeV/c (2 MeV kinetic energy). To maintain the beam (about 10^9 particles) within acceptable dimensions and to counteract intrabeam scattering , we have developed a stochastic cooling system for these momenta. It includes several new features such as digital filters for the longitudinal cooling system.

The pick-ups

The pick-ups are of travelling wave type (TWPU). They are composed of a number of loop couplers connected in series outside the vacuum. The length of the connecting cable is such that it corresponds to the beam travelling time between the centre of two consecutive loop couplers. Coaxial relays are inserted to commute between a short delay (105 MeV/c) and a longer one (61.2 MeV/c). There are two circuits, one for the inner(top) and one for the outer(bottom) electrodes. This gives the possibility to obtain sum and difference signals. The upstream end of the TWPU is terminated with a 50 ohm resistor cooled at 20 K. The head amplifier which is connected to the downstream end, is cooled to 80 K. This leads to a noise figure of 0.8 dB (fig.1). The characteristic of this "home made" amplifier are shown in fig 2. The momentum cooling system uses the sum signal and is based on the filter method [1,2]. The horizontal and vertical systems use the corresponding difference signals (see e.g.[2]).

Results on cooling at 105 and 61.2 MeV/c

With the three systems working (fig. 3 for the horizontal plane , fig. 4 for the vertical plane), the life time of the beam at 105 MeV/c was increased from 0.3 to 3 hours (1.2 10^9 particles), fig. 5. At 61.2 MeV/c the life time increased from 7 to 25 minutes. The momentum spread at 61.2 MeV/c is maintained within 2‰ (5 10^8 particles), fig. 6.

Design of the notch filter

The most common way to build a recurrent notch filter for longitudinal cooling is by using adapted cables or delay lines as shown in fig. 7a,7b. The frequency response of these filters is shown in fig. 8a,8b, where the frequency difference between notches is defined by the length or the half length of the delay line. The phase depends on the sign of the reflected wave for the

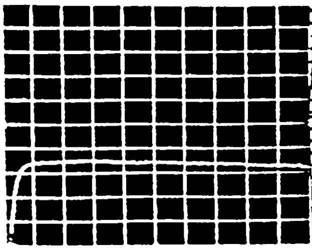


Fig.1
Noise figure of the MGF1412 GaAs Amplifier cooled to 80 K. 0.2 dB/div, Sweep 0-200 MHz

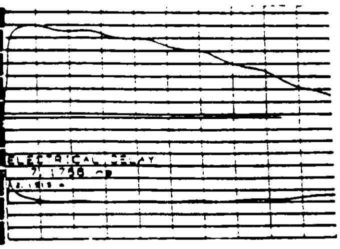


Fig.2
Amplitude and phase versus frequency response of the MGF 1412 Amplifier.
5 dB/div. ; 90°/div.
Sweep 0.3-200 MHz.

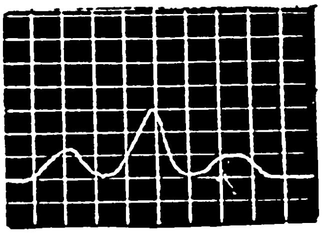


Fig.3
Example of a horizontal Schottky scan in LEAR at 105 MeV/c.
Frequency span 450 KHz.
Centre frequency 42.45 MHz.

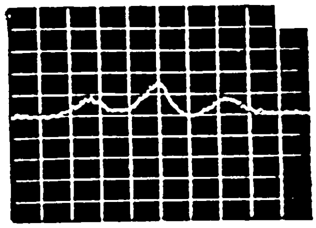


Fig.4
Example of a vertical Schottky scan in LEAR at 105 MeV/c.
Frequency span 450 KHz.
Centre frequency 42.45 MHz.

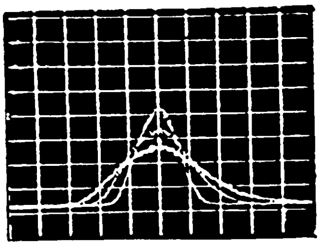


Fig. 5
Example of momentum cooling effect on a beam at 105 MeV/c. after 40 s. and after 200 s.
Frequency span 220 KHz.
Centre frequency 31.25 MHz.

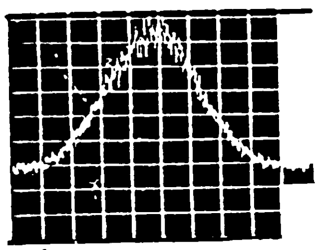


Fig. 6
The momentum spread at 61.2 MeV/c. is maintained within 2 ‰ .
Frequency span 200 KHz.
Centre frequency 33.053 MHz.

circuit of fig.7a, and for fig.7b, on the input phase combiner (0 or 180 degrees). Cables or artificial delay lines can be used in principle. With artificial delay lines it is difficult to obtain good phase linearity as well as constant magnitude over a large bandwidth. Therefore this solution should be reserved for low frequency and modest bandwidth (50 MHz) applications. The second way, using coaxial cables as delay lines is better and easier if the notch frequency interval does not require cables longer than 500 m. (corresponding to a notch spacing of about 0.4 MHz for the circuit of fig.7a). Longer cables become heavy and expensive because in order to provide sharp notches, low losses and good phase linearity are required. This means large mechanical dimensions and high unit price.

At LEAR we have this problem at very low momentum, especially at 61 MeV/c, where a 1.5 Km. cable would be necessary to have the notch interval of 242 KHz. On the other hand the useful bandwidth is limited by band overlap which starts somewhere in the 50 to 100 MHz region depending on beam momentum and momentum spread. We have therefore developed a digital delay line with 100 MHz (fig. 10) bandwidth for the prototype and up to 200 MHz for the final version. The phase linearity is better than 2 degree in the useful region.

The principle is simple, but the realization is a technological challenge. The basic idea is to sample the input signal as fast as possible and store it for the time needed to provide the desired notch spacing. (at LEAR this interval must be adjustable because we want to use the system from 60. to 200 MeV/c).

Next the signal is recovered and combined with the original one to obtain the notch effect.

In 1988 we have investigated the possibility to store the input signal in one analog CCD delay line. Unfortunately this solution permits only fast storing, but due to high output impedance the restitution of the signal cannot be done faster than 20 MHz.

The solution we have chosen is based on analog to digital conversion followed by word memorization, shift, conversion to analog form and recombination with the original signal.

Description of the circuit

The input signal (fig.9) is digitized (8 bit definition) with a fast ADC at 200 megasamples rate, one 8 bit latch keeps data stable between samples. Due to the memory access time of 15 ns, the sampled data are latched alternatively on 4 latches working at 1/4 of the main clock ratio, this enables us to meet the read/write time requirement of the four following 256x8 memory-cells. These memories act as FIFO devices with variable length. In fact the time between a defined input data sample and the output of the same one depends on the value present in the address counter driving the memory cells.

The result is that we obtain from the memory output a word which is delayed from input by Nx4 times the main clock ratio (where N is the preset value of address counter). Subsequently we recover data from each memory bank in the same way as we have store them. The data are then fed to a fast DAC (500 MHz) in the same manner and at the same speed as the direct signal. The two reconstructed signals are recombined either with 0 or 180 degrees relative phase depending on the frequencies where we want start the notch effect.

The magnitude of the two reconstructed signals is minutely adjusted to obtain the best result.(fig. 11). Finally to fully cover the minimum time step corresponding to the least significant bit in the address counter (50ns. at 200 Mhz main clock), the main clock generator can be finely adjusted without a considerable change of the system bandwidth.

To avoid the aliasing phenomena a low pass filter less than 1/2 of the sampling rate must be added at the input side and another

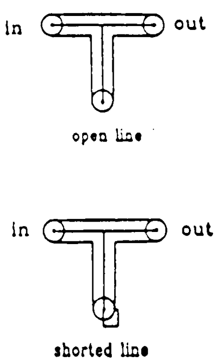


Fig. 7a
Simple periodic notch filter using low loss transmission line as a stub resonator.

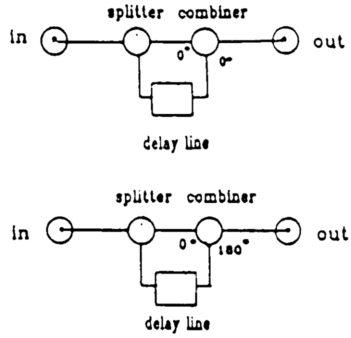
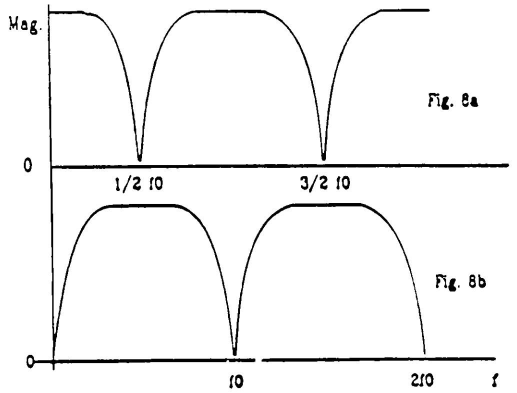


Fig. 7b
Periodic notch filter using a delay line and combiner.



Amplitude versus frequency response of the notch filter. The period is defined by the length of the delay line (fig. 7b) or by 2 times the length of the cable (fig. 7a).

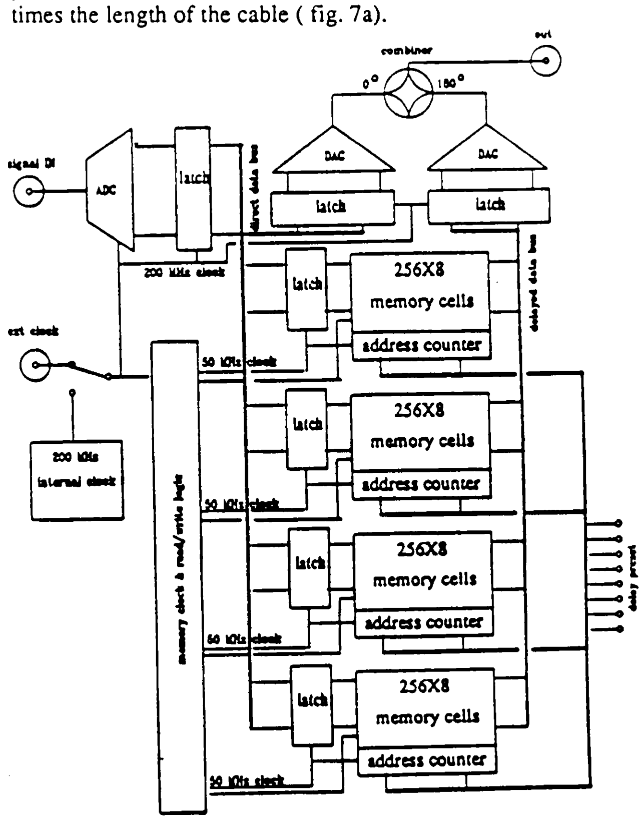


Fig. 9 Block diagram of the digital notch filter.

one rejecting the sampling frequency at the output side.
The problems encountered in the realization of this circuit were essentially due to the interconnection length and adaptation of wires carrying signals. At this frequency care must be taken at each connection and all lines must be properly terminated. The wiring is done with strip lines techniques on an epoxy substratum. The logic circuitry is of ECL type. The conversion devices are manufactured by 'Analog Devices'. The internal main clock generator is fixed at 200 MHz and controlled by one 50 MHz crystal.

Circuit characteristics
(200MHz clock)

Zin	50 ohm.
Zout	50 ohm.
Bandwidth	100 MHz.
Input range	+- 2 V.
Gain	0 dB.
Phase linearity	+- 1 °
Notches depth	40 dB.
Delay line adjustment range	50 ns. to 1280 ns.

Improvements

The actual bottleneck in digitizing speed is given by the ADC conversion time; the input capture time is very short ~340 ps. Coupling two ADCs working with a sampling clock in phase opposition will increase the bandwidth up to 200 MHz. The news ECL SRAMs devices with 2 ns. access time will permit to simplify the design, one fast digital adder can be used to sum or subtract the two signals and finally a fine tunable clock generator can be included on board.

Conclusion

The stochastic cooling system described above is of great importance for operation of LEAR at low momenta The resulting increase of the beam life time permits slow extraction spills of 1 hour at 105 MeV/c and 15 minutes at 61.2 MeV/c. Digital notch filters have been successfully used for momentum cooling.

Acknowledgements

We would like to thank D.Allen, J. Chevallier, C.Vasseur and H.Picard for their excellent contributions to the work described above.

References

[1] L.Thorndahl and G.Carron, "Stochastic cooling of momentum spread with filter techniques," CERN/ISR/RF/78-12, 1978.

[2] D. Möhl, "Stochastic cooling for beginners," in Proceedings of the CERN Accelerator School, " Antiprotons for colliding beam facilities," CERN Report 84-15, 1984, pp. 97-153

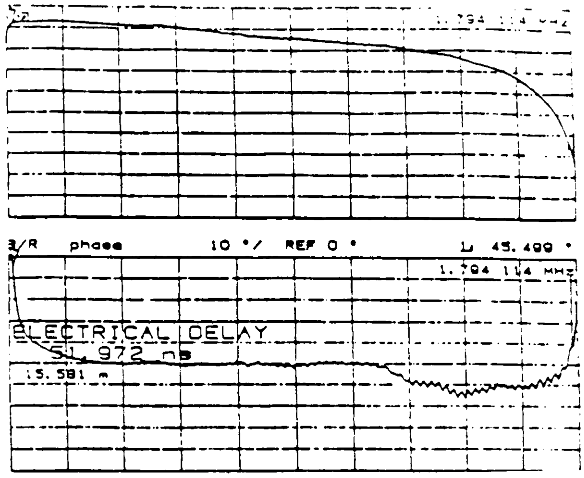


Fig. 10
Amplitude and phase versus frequency response of the digital delay line. 5 dB/div, 10°/div, sweep 0.3-200 MHz.

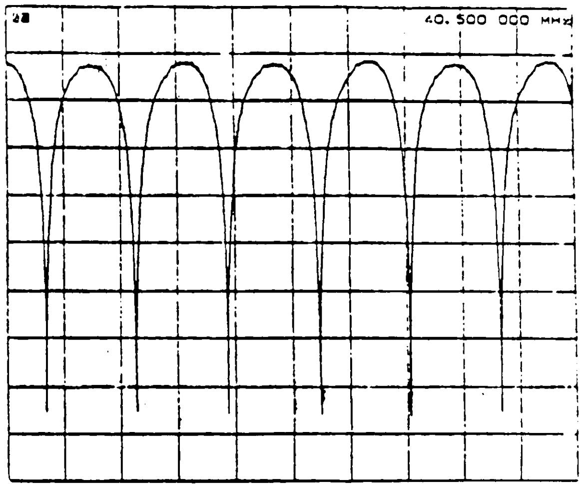


Fig. 11
Periodic effect of the digital notch. 5dB/div.
Frequency span 1MHz.
Centre frequency 40 MHz.

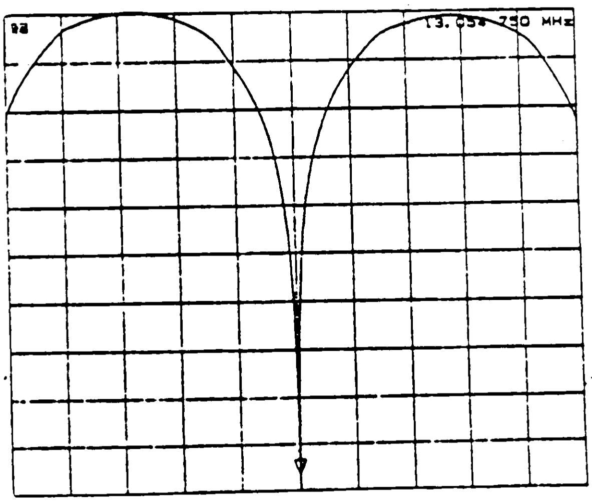


Fig. 12
Behavior of the digital notch. 5dB/div, frequency span 400 KHz.
Centre frequency 13.054 MHz.