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OPTIMUM CONTROL OF PWM RECTIFIERS FOR MAGNET SUPPLY

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ABSTRACT

The paper presents a very low current ripple PWM rectifier for supply of particle accelerator magnets. The modulation technique is based on the feed-forward optimum control theory and is implemented by means of a high-performance micro-controller, which also generates the PWM control of the converter switches.

The proposed solution consists in a single-stage step-down totally-controlled GTO converter, and uses the Intel 80C196KC micro-controller. The optimum control strategy ensures minimum low frequency output voltage ripple and maximum input power factor irrespective of the line voltage distortion.

Design criteria and control implementation are described. Experimental results are given for a 15 kW prototype.

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Abstract

The paper presents a very low current ripple PWM rectifier for supply of particle accelerator magnets. The modulation technique is based on the feed-forward optimum control theory [1,2], and is implemented by means of a high-performance micro-controller, which also generates the PWM control of the converter switches.

The proposed solution consists in a single-stage step-down totally-controlled GTO converter, and uses the Intel 80C196KC micro-controller.

The optimum control strategy ensures minimum low frequency output voltage ripple and maximum input power factor irrespective of the line voltage distortion.

Design criteria and control implementation are described.

Experimental results are given for a 15 kW prototype.

Keywords: PWM rectifiers, optimum control, micro-controller.

INTRODUCTION

Power supplies for magnets of particle accelerators are primarily required to supply almost ripple-free DC currents (better than 0.01%). Moreover, because of the high power levels involved, the behaviour on the supply side must also be optimized, both in terms of reactive power absorption and harmonic content of the line currents.

The classic solution of 12 pulses, fully controlled thyristor rectifiers is well suited for the regulation of such a high power, while keeping the harmonic content within reasonable limits. In order to meet the demanding specifications, however, heavy input and output passive filters are also needed.

A better solution can be obtained by means of PWM rectifiers using GTO switches, which are able to handle power in the MW range while allowing high modulation frequency and fast regulation of input and output variables [3]. Provided suitable control tecniques are employed, the low ripple and high power factor requirements may be fulfilled even with input and output filter of reduced size [4].

In the paper a single-stage, step-down GTO converter structure is presented, which is modulated according to the feed-forward optimum control strategy presented in [1,2]. The calculation of the modulation laws is directly performed, from the instantaneous input voltages, by a 80C196KC Intel micro-controller. This solution ensures minimum output ripple and maximum input power factor irrespective of the line voltage distortion, thus allowing an optimal utilization of the converter capability and a minimization of the filtering needs together with the reliability of the digital control.

SYSTEM CONFIGURATION AND BASIC OPERATION

The basic system configuration is shown in Fig. 1. It includes a PWM bridge rectifier made up of six unidirectional fully-controlled switches, input and output filters and ohmic-inductive load.

For the application being considered, both positive and negative output voltages are needed. In fact, in order to obtain an accurate control of the DC current, a system response faster than the load time constant is required. Thus, as the load is higly inductive, impressed current schemes like that of Fig. 1 offer the only single stage solution.

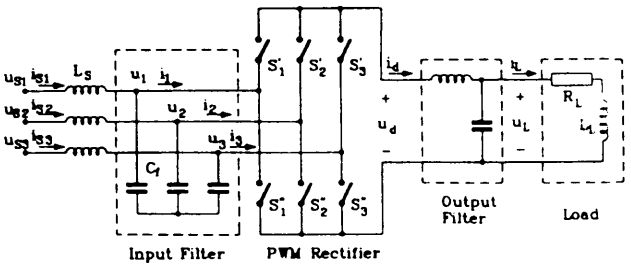

Fig. 1 - Basic System Configuration.

Since the converter is seen by the AC supply as a PWM current generator, capacitive input filters C_f must be employed. Moreover additional series inductors L_s may be required to enhance the line current filtering.

Also an output filter is normally needed to comply with the DC current ripple specifications, although of reduced size in comparison to those used in thyristor solutions.

For given input and output ripple, the size of filter components are strongly dependent on the modulation frequency f_m adopted. This latter, in turn, depends on the kind of switching components used. With GTO's, f_m typically ranges from some hundreds to a few thousands of Hz.

Taking into account the inductive load, for safe converter operation at least one switch in the upper and one in the lower half-bridge must be closed at any time. Closing more than one switch in one half bridge does not cause converter fault as the switches are unidirectional. However, as an uncertainity in the current path can arise, this situation cannot be allowed, except during commutations.

Thus, calling x_i' and x_i'' (i=1..3) respectively the status signals (0=off, 1=on) of upper switches S_i' and of lower switches S_i'', it results:

$$x_1' + x_2' + x_3' = 1 \quad (1.a)$$
$$x_1'' + x_2'' + x_3'' = 1 \quad (1.b)$$

Depending on the switch pair closed, rectified voltage u_d can coincide with one of line-to-line voltage or can be zero (free-wheeling state). The general expression of the instantaneous voltage u_d is:

$$u_d = (x_1' u_1 + x_2' u_2 + x_3' u_3) - (x_1'' u_1 + x_2'' u_2 + x_3'' u_3) \quad (2)$$

where u_1, u_2, u_3 are the converter input voltages.

From Eqs. 1 and 2 it derives that free-wheeling state is obtained when both the switches of one leg are on.

Defining now status signal x_i of the i-th bridge leg as:

$$x_i = x_i' - x_i'' \quad (3)$$

which equals 1 if upper switch S_i' is on, -1 if the lower switch S_i'' is on and 0 if both switches are on or off, Eq. 2 becomes:

$$u_d = x_1 u_1 + x_2 u_2 + x_3 u_3 \quad (4)$$

In the same way, converter input currents may be expressed in dependence of output current i_d:

$$i_1 = (x_1' - x_1'') i_d = x_1 i_d \quad (5.a)$$
$$i_2 = (x_2' - x_2'') i_d = x_2 i_d \quad (5.b)$$
$$i_3 = (x_3' - x_3'') i_d = x_3 i_d \quad (5.c)$$

Note that, at any time, only two converter legs can be modulated independently, the third being constrained by Eqs. 1. This condition, however, does not cause any practical limitation, since controlling the waveforms of two line currents necessarily implies the waveform produced by the third leg.

Considering the time-average value of status signals x_i, modulation laws m_i of the converter legs are obtained. Accordingly, from Eqs. 4 and 5 the following relationships among the low frequency content of converter variables (indicated by underline) are derived:

$$\underline{u}_d = m_1 \underline{u}_1 + m_2 \underline{u}_2 + m_3 \underline{u}_3 \quad (6)$$

$$\underline{i}_1 = m_1 \underline{i}_d \quad (7.a)$$
$$\underline{i}_2 = m_2 \underline{i}_d \quad (7.b)$$
$$\underline{i}_3 = m_3 \underline{i}_d \quad (7.c)$$

where modulation laws m_i can vary between -1 and +1.

As the input currents have zero sum, by adding Eqs. 7 it derives immediatly that at any instant:

$$m_1 + m_2 + m_3 = 0 \quad (8)$$

thus two degrees of freedom in the choice of modulation laws are allowed.

Eq. 6 shows that, for given input voltages, by adopting suitable modulation laws m_i, the $\underline{u}_d$ amplitude can be varied continuously from a maximum down to zero both in positive and negative polarity. In particular, $\underline{u}_d$ can be kept constant for any waveform of input voltages.

One degree of freedom remains, which can be used for some optimization of the input current behaviour, according to Eqs. 7.

This approach is a particular case of the general optimization technique [1,2], when the smoothing of the DC output voltage is of primary concern. Moreover, owing to the high load inductance value, $\underline{i}_d$ can be considered fairly constant.

CONTROL STRATEGY

The optimum control theory gives the modulation laws which allow the output voltage $\underline{u}_d$ to follow a given reference u^*, while minimizing the total harmonic content of the input currents.

With these assumptions the modulation laws turn out to depend only on the actual values of input voltages $\underline{u}_i$:

$$m_i = \frac{u^* \underline{u}_i}{\underline{u}_1^2 + \underline{u}_2^2 + \underline{u}_3^2} \quad (9)$$

Eqs. 9 show that only if input voltages $\underline{u}_i$ are sinusoidal and symmetrical, also sinusoidal modulation laws are obtained. Thus, from Eqs. 7, sinusoidal, symmetrical and in phase input currents result too.

In the case of non sinusoidal and/or non symmetrical input voltages, the denominator of Eq. 9 is in general a non constant term. Thus the waveform of modulation law m_i differs from that of the corresponding voltage $\underline{u}_i$ and the input current $\underline{i}_i$ becomes distorted.

Consider, for example, the case of sinusoidal but unbalanced input voltages. In this instance it is possible to refer to the unbalance degree, expressed as the percentage of reverse component related to the direct component of the voltage sequence. If symmetrical and sinusoidal modulation laws were adopted, sinusoidal input currents would be obtained but the DC voltage would present a second harmonic component (at twice the line frequency) fairly proportional to the unbalance degree, as indicated in Fig. 2. This shows that it is not possible to maintain sinusoidal modulation laws and meet the low output ripple specification at the same time. On the contrary, if modulation laws obtained by Eqs. 9 are used, according to the optimum control technique, zero DC voltage ripple results but the input currents become distorted, as reported in Fig. 2 again.

It should be pointed out that, in the input current harmonic content, also a non negligible third harmonic is present. Indeed, with unsymmetric input voltages, unsymmetric input currents result, as shown in Fig. 3 for the case of 20% voltage unbalance degree.

CONTROL IMPLEMENTATION

The feed-forward optimum control strategy can be

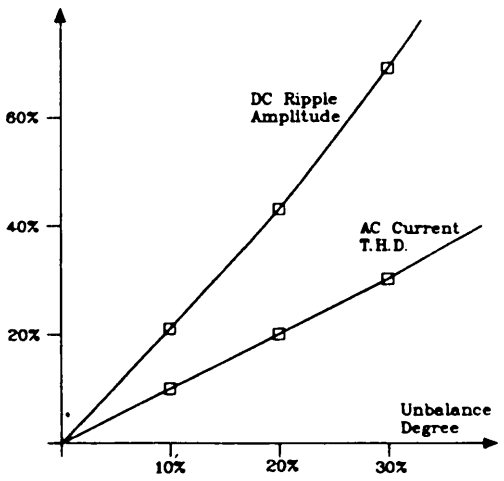

Fig. 2 - Input Voltage Unbalance Effects
top: DC voltage ripple for synusoidal modulation laws.
bottom: Total AC current harmonic distortion for optimum modulation laws.

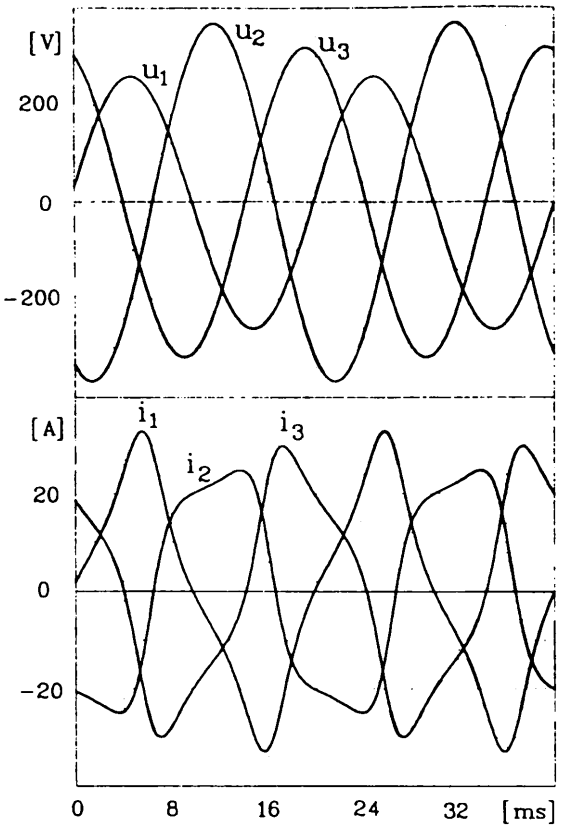

Fig. 3 - Operation with Optimum Control
and 20% Input Voltage Unbalance
top: Simulated AC voltages
bottom: Simulated AC currents

easily implemented by means of a micro-controller (μC), which is well suited to perform all A/D conversions, calculations and other control tasks. Here the μC Intel 80C196KC was chosen.

Fig. 4 shows the control scheme. The converter input voltages u_i are sensed and reduced to proper limits (by Voltage Conditioning Block) for the ADC included in the μC, and are converted, together with the output voltage reference u^*, at the beginning of each half modulation period.

The μC calculates the three modulation laws, according to Eqs. 9. From these relations, the switch status sequences are calculated, according to a strategy described later, and stored, together with their duration of validity, in a circular buffer. This latter is controlled by an internal timer and, when the actual status duration is expired, the new switch status is transferred to the output buffer. Accordingly, the GTO gating signals are generated by the Driver circuits.

When the timer reaches the number of microseconds corresponding to the duration of half modulation period, it is reset and all acquisitions and computations are started again for the next half-period.

The flow chart of the program is shown in Fig. 5. The total computation time is about 250 μs thus allowing modulation frequency f_m up to 2 kHz.

A PLL circuit is also used to synchronize the modulating frequency of the bridge with the line frequency. For this purpose, the μC produces a synchronizing signal (sync), by dividing the modulation frequency by the number of periods which should be included in the line period. This signal is fed to an external phase comparator, together with a signal synchronized to a line voltage. The comparator output is filtered and converted by the μC so as to correct the duration of the half modulation period.

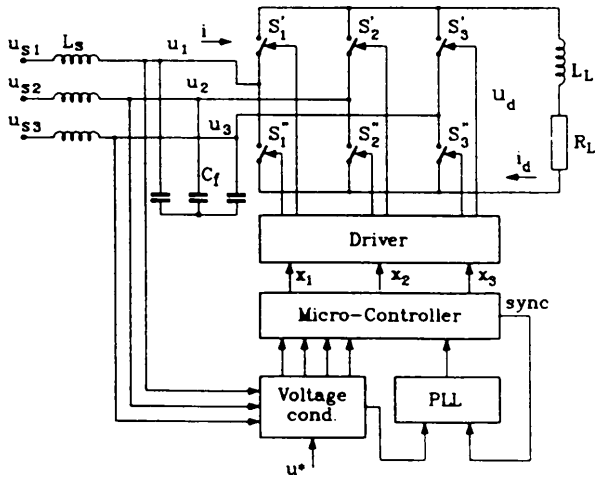

Fig. 4 - Control Scheme

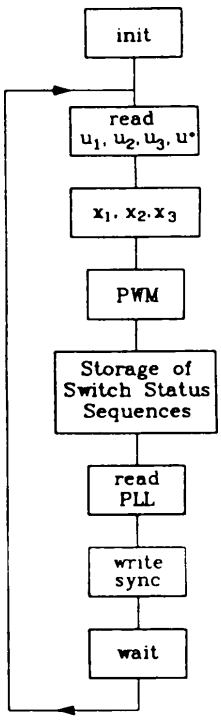

Fig. 5 - Simplified Flow Chart
of Micro-Controller Program

Although the above solution was chosen to limit the calculation time of the μC, a fully digital implementation of the PLL is also possible and is well within the capability of the μC itself.

As a result of the syncronization, very low subharmonic content in the output voltage was obtained.

MODULATION TECHNIQUE

For given modulation laws, different switching patterns can be adopted within the modulation period.

In fact, for each leg, the same value of the modulation law m_i can be obtained by different timings of status signal x_i of the leg switches, according to Eqs. 3. More precisely, as shown by Eqs. 5 and 7, m_i depends on the difference between the on times of the upper and lower switch of the same leg i within the period.

In this application the following switch timing criterion has been adopted [5]. At the beginning of the first modulation half-period, the calculated modulation laws m_i are compared each other, and the two phases corresponding to the maximum positive m_{max} and minimum negative m_{min} values are selected (Fig. 6).

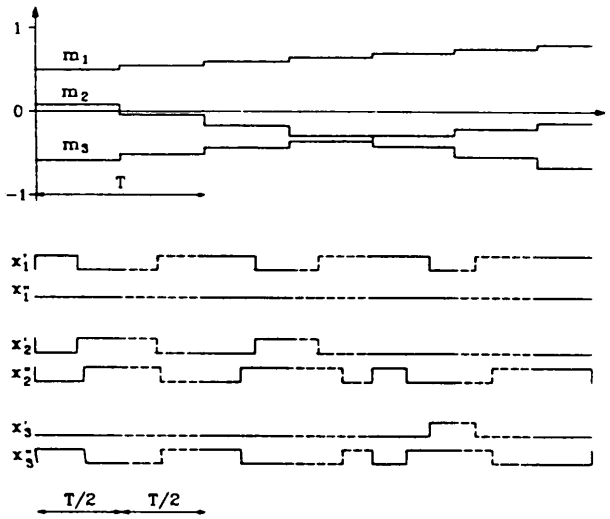

Fig. 6 - Calculated Modulation Laws and Switch Status

In the leg corresponding to m_{max} (phase 1 in the example of Fig. 6) the upper switch is turned on and kept closed for a fraction of half-period equal to m_{max}. The lower switch of the same leg is kept open for the whole half-period.

Similarly, in the leg corresponding to m_{min} (phase 3 on the left and phase 2 on the right of Fig. 6), the upper switch is kept open, while the lower one is closed so as to give a duty cycle equal to m_{min}.

In the third leg, the upper switch is turned on at the opening of the upper switch of the first leg. Similarly the lower switch of the third leg is closed when the lower switch of the second leg is turned off. Thus the constraints of Eqs. 1 are satisfied. When both switches of the third leg are closed, a free-wheeling state is established. Thus, output current is shorted by the two closed switches, and no input current flows in the third phase nor in the others.

At the beginning of the the second half-period a new computation of the modulation laws is done. The strategy adopted is the same as in the first half period, but reversed in time, beginning with both switches of the third leg on. Thus quasi symmetric waveforms in the whole period are obtained.

With this strategy, only four switches are operated in the modulation period. This results in an average switching frequency of each switch equal to 2/3 of the modulation frequency. Moreover, the instantaneous current in each input phase does not reverse within the period. This ensures minimum rms value of the current itself. The criterion of using two samples of the modulation laws in the modulation period corresponds to the so called regular sampling technique [6], which produces an additional improvement of input and output waveforms.

DESIGN CRITERIA

At the input side the converter presents a current generator characteristic. Thus input filter capacitors C_f (Fig. 1) are required to keep the voltage ripple of the converter input within reasonable limits and to reduce modulation frequency current harmonics in the line. According to the figure reported in [5], the maximum voltage ripple can be evaluated from the current ripple integral taking into account the total capacitance interested by this current. Assuming that the ripple voltage waveform can be approximated by a triangular shape, it results:

$$v_{rpp} = I_d/(6\ f_m\ C_f) \qquad (10)$$

where v_{rpp} is the peak-to-peak ripple value, I_d is the actual DC current, f_m is the modulation frequency and C_f is the capacitance the of line to line filter capacitors.

The line current harmonics may be reduced further by means of additional series inductors L_s which increase the line inductances. The corresponding line induced current component i_r (rms) at frequency f_m is given by:

$$i_r = 0.09\ v_{rpp}\ /(f_m\ L_{ss}) \qquad (11)$$

where L_{ss} is the total series inductance, including that of the supply.

As regards the line harmonics, comparable reductions are obtained either by increasing capacitance C_f or inductance L_{ss}. However, if large capacitive values are chosen, the reactive power absortion becomes worse. On the contrary, larger series inductances result in higher voltage drops. Thus a suitable trade off has to be found.

From the above relations, if the system input configuration is that of Fig. 1, the values of C_f and of L_s can be determined.

At the ouput side, the filter design strongly depends on the switching pattern adopted. With the solution described above the peak-to-peak current ripple i_{dr} may be evaluated [5] according to:

$$i_{dr} = (\sqrt{6}/4)\ U\ /(L\ f_m\ ) \qquad (12)$$

where U is the rms line voltage and L is the load series equivalent inductance at the modulation frequency f_m.

For a given ripple limit, and with the modulation frequency which can be used with the GTOs, the required value of L turns out to be appreciably lower than the value usually adopted for SCR rectifiers.

As regard the frequency modulation, it may be taken into account that the average commutation frequency of each switch is about $(2/3)f_m$. Thus f_m can be chosen up to 50% higher than the maximum switching rate of GTO's used in the converter.

EXPERIMENTAL RESULTS

The proposed control method was applied to a rectifier prototype, of reduced power. It included a three-phase bridge converter with unidirectional GTO switches (Fig. 7).

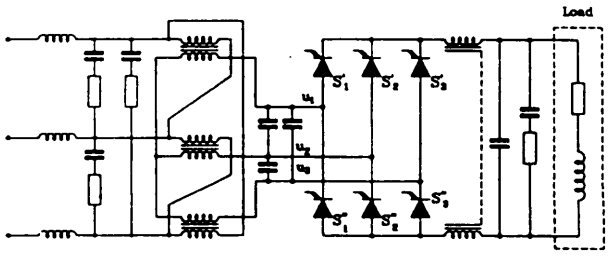

Fig. 7 - Experimental Prototype Configuration.

System specifications are:

AC input voltage (line to line)	380 V
DC voltage (resistive drop)	170 V
DC current	85 A
DC current accuracy (including ripple)	≤ 0.01 %
Load inductance	5 mH
Load time constant	≈ 2.5 ms
Modulation frequncy f_m	1.5 kHz
AC Power factor	≥ 0.9
Efficiency	≥ 90 %

As shown in Fig. 7, the input circuit configuration was complicated, with respect to the scheme of Fig. 1, by the presence of an input step-down transformer with its equivalent series inductance. Thus the optimal C_f and L_s values are found by simulation, which also allows a proper choice of the damping resistors R_{da}. The following values are adopted:

E_1/E_2 turn ratio	380/90 Delta/Wye
V_{sc} short-circuit voltage	10%
L_s input filter inductance	0.1 mH
C'_f + R_{da} (primary side)	10 μF + 2 Ohm
C''_f (secondary side)	280 μF

In the output circuit a damping branch R_{dd}, C_{dd} is added. The filter inductor L_{fd} is split into two mutually coupled windings. The adopted values are:

L_{fd}	Output filter total inductance	2.5 mH
C_{fd}	Output filter capacitance	50 μF
C_{dd}	DC side damping branch capacitor	164 μF
R_{dd}	DC side damping branch resistor	1.33 Ohm

A clamping circuit, not indicated in Fig. 7, is connected in parallel with the load, for protection against accidental opening of the load current path.

Feed-forward control and Pulse Width Modulation ensure very fast responce of the converter output voltage, typically within a half of modulation period corresponding to a bandwidth of 500 Hz.

Snubbers of conventional design are used in parallel to the converter GTOs. Owing to the low modulation frequency, the accuracy of the open loop control of the commutation times is not appreciably affected by GTO switching times and by the snubber action.

The system operation was tested for the entire range of operating conditions, demonstrating reliable performance and excellent accuracy, both at the input and at the output, in accordance with the theoretical expectations.

As an example, in Fig. 8 are shown an input line voltage u, the corresponding input current i and its spectrum, obtained at a DC output of 150 V, 75 A. The low ripple voltage amplitude and small current harmonic content can be appreciated. The presence of a third-harmonic component can be justified by the presence of some unbalance in the input voltages.

The DC voltage spectrum, in the same conditions, is shown in Fig. 9, while in Fig. 10 the load current spectrum is reported.

The small amplitude of the voltage spectrum components, (less than -50 dB up to 900 Hz with respect to the DC component) confirms the effectiveness of the optimum control technique in actual operating conditions. In particular the low-order harmonics, multiples of the line frequency (which are of significant amplitude in thyristor rectifiers), result of negligible value.

The very low harmonic content of the load current corresponds to a total ripple well within the specified limits.

CONCLUSIONS

A PWM GTO rectifier for magnet supply was presented, digitally controlled according to an optimal feed-forward technique.

The Pulse Width Modulation according to the optimal control strategy results in outstanding performance both on the line and load side.

Very low DC current ripple was obtained, even with an output filter of reduced size, in comparison to that needed for usual thyristor rectifiers.

High power factor and small input current harmonic contents have been ensured also in presence of appreciable line voltage distortions and unbalances.

The system performance was verified on a prototype of significant size, demonstrating to be fast, accurate and reliable.

Acknowledgement

The authors would like to thank M. Farioli for his effective support to the development and implementation of the experimental work.

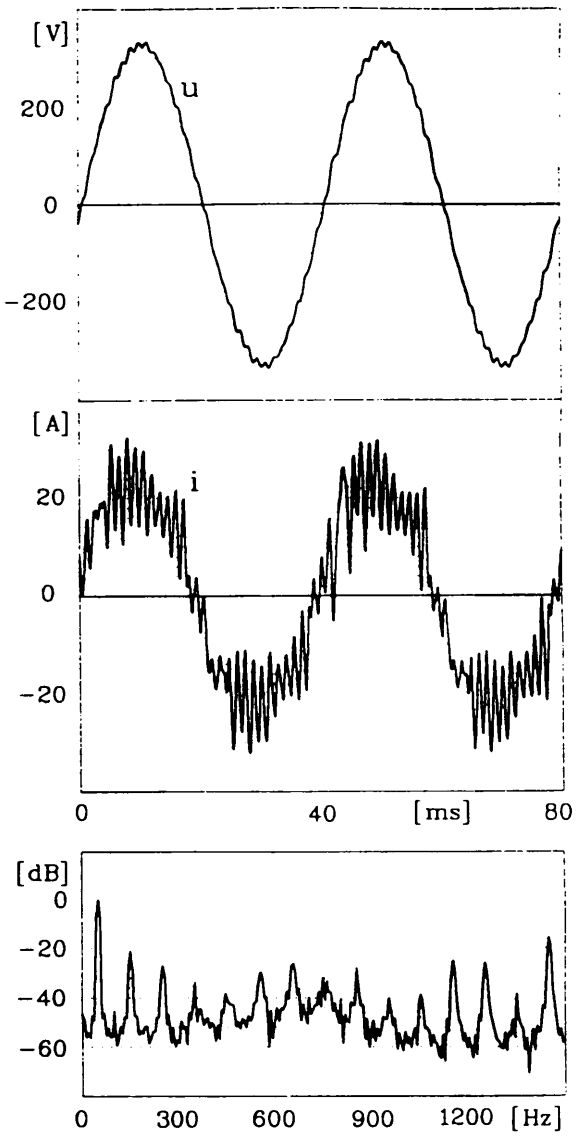

Fig. 8 - Experimental results (u_d=150V)
top to bottom:
AC voltage (4 ms/div, 100 V/div)
AC current (4 ms/div, 10 A/div)
AC Current sprectrum (150 Hz/div, 20 dB/div)

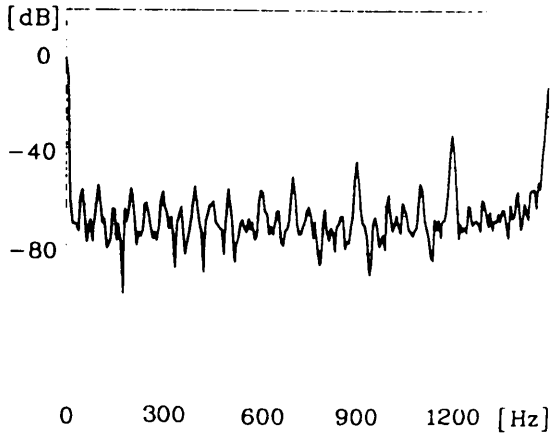

Fig. 9 - DC Output Voltage Spectrum
(u_d=150V, 150 Hz/div, 20 dB/div)

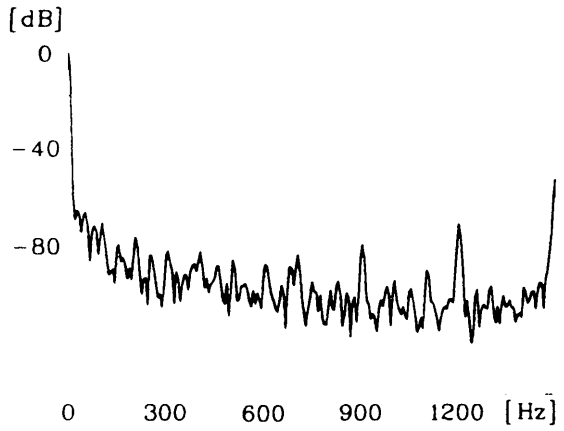

Fig. 10 - DC Load Current Spectrum
(u_d=150V, 150 Hz/div, 20 dB/div)

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