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### CLOSED-ORBIT SIGNAL SUPPRESSOR FOR THE TRANSVERSE FEEDBACK OF THE PSB

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#### 1. SUMMARY AND INTRODUCTION

In the PSB (along with most circular particle accelerators and storage rings) transverse instabilities can develop, giving rise to fast oscillations of the beam around its equilibrium position (closed orbit).

These oscillations can be damped by feeding back to the beam (through an electromagnetic deflector) a signal that is proportional to them, and with the proper phase<sup>1)</sup> (Fig. 1).

As the power requirements of the deflector-driving amplifier depend on the amplitude of the signals it has to handle, there is a practical interest in keeping these signals no larger than is required for damping.

The instability signal can be obtained from an electrostatic pick-up similar to those normally used for orbit observation. Such a pick-up produces two signals, consisting of two bunch-shaped carriers modulated in opposite phase by the beam position. The difference between these two signals no longer contains the carrier, but only two sidebands with the spectrum of the beam position.

The beam position is the sum of the closed orbit plus the instabilities. The closed orbit can be, and normally is, predominant; therefore it largely determines the power in the spectrum and hence the power requirements of the deflectordriving amplifier.

It might therefore be interesting to remove the closed-orbit component of the pick-up difference signal and leave only the component due to the instabilities, which we need in order to operate the feedback system. This is what the circuit described in the following sections is designed to do, taking advantage of the fact that the closed orbit and the instabilities occupy different portions of the composite signal spectrum.

#### 2. CIRCUIT DESCRIPTION

#### 2.1 Functional description

The circuit is realized as a self-balancing bridge<sup>2)</sup>, reaching its equilibrium point when the closed-orbit component of the difference signal is zero. The bridge is shown in the block diagram (Fig. 2) as two FET-controlled attenuators driven by the phase opposing signals coming from amplifiers  $A_1$  and  $A_2$ . These closed-orbit signals are obtained by phase detection through an analog multiplier, making the product of the sum and difference signals, followed by a low-pass filter.

The transverse displacements of the beam appear as an amplitude modulation of the bunch signals. Whilst the amplitude of the modulating wave is the same on each of the pick-up plates, the phase is in opposition. As there is no overlap between the frequency spectra of the instability and the closed-orbit modulating signals, the latter can be separated after synchronous demodulation by a low-pass filter; this is done in order to obtain the control voltage for the variableresistance FETs.

It will now be shown that it is possible to eliminate the closed-orbit component from the difference signal, provided that the modulating envelope exists as a separate signal.

Let the signals at the plates of the pick-up be represented by a carrier f(t) amplitude modulated by two time functions h(t) and g(t), representing the closed orbit signal and the instabilities, respectively, i.e.

$$e_1(t) = [1 + h(t) + g(t)]f(t)$$
 (1)

$$e_{2}(t) = [1 - h(t) - g(t)]f(t)$$
 (2)

The difference signal, without closed-orbit suppression, will simply be a suppressed carrier waveform. Multiplying Eq. (1) by 1 - h(t) and Eq. (2) by 1 + h(t) and then making the difference, we obtain

$$e_{s}(t) = 2 g(t)f(t)$$
 (3)

In this last equation it can be seen that the closed-orbit component has been completely removed from the difference signal.

The above arguments are recapitulated graphically in Fig. 3. The left-hand side of the figure, working from top to bottom, shows: a) the spectrum of h(t); b) the spectrum of g(t); c) the low-pass filter amplitude response. The righthand side of the figure, again from top to bottom, shows the spectra of: d) the modulated plate signal; e) the difference signal without closed-orbit suppression; and f) the difference signal after closed-orbit suppression.

#### 2.2 The suppression factor

In order to get a quantitative description of the circuit performance, a suppression factor can be defined as the ratio of power contents of the differential output signal in open- and closed-loop conditions, i.e.

# $F = \frac{Power \text{ content without suppression}}{Power \text{ content with suppression}}$

In both cases the differential signal considered is that due to the carrier modulated by h(t) alone. Considering the Fourier development of the signals, it can be proved<sup>2)</sup> that the power content (PC) of the differential voltage after suppression becomes

PC = 
$$kf^2t^2 \sum n^2c_n^2$$
, n = 1, 2, 3, ...,

where t is the FET time constant, f is the fundamental frequency of the carrier, and  $c_n$  its Fourier coefficients.

The suppression factor can now be written as

$$F = \frac{\sum_{n=1}^{\infty} c_n^2}{kf^2 t^2 \sum_{n=1}^{\infty} n^2 c_n^2}, \quad n = 1, 2, 3, \dots$$

Using an RF FET such as the 2N 4416, a time constant as low as t = 0.4 ns can be achieved.

For a bunch-formed carrier the form factor

$$\frac{\sum c_n^2}{\sum n^2 c_n^2} \approx 0.6 ,$$

and for the PS Booster the highest carrier repetition frequency is f = 8 MHz. Under these conditions the suppression factor becomes

$$F = 10^3$$
 .

This figure reduces the output power, at the present highest intensity of the PSB beam and with a gain of 2000 from pick-up to deflector, to less than 10 W.

#### 2.3 Circuit details

The self-balancing bridge is made up of two attenuators with 2N 4416 FETs as controllable resistors. The lengths of the paths on the printed circuit from the inputs through the attenuators up to the differential amplifier inputs are carefully equalized, in order to avoid phase differences between the signals. A phase difference of 0.8 degrees at the fundamental frequency of the carrier reduces the suppression factor by a factor of two. This corresponds to a delay of 0.3 ns, so the lengths of the cables from the pick-up to the closed-orbit suppressor have to be equalized accordingly in order not to degrade the circuit performance. An adjustable coaxial delay line has been introduced in the signal path after the head amplifiers in order to adjust this length in the actual operating conditions.

The trimmers  $C_3$  and  $C_7$  provide the means for adjusting the reactive component of the bridge at balance.

In order to extend the linearity range of the FETs, a feedback arrangement (as indicated in Fig. 4) has been provided.

It has been proved<sup>3,4)</sup> that the distortion of a variable FET attenuator can be considerably reduced by feeding a fraction of the drain voltage back to the gate. The linearity of the characteristics around the origin, particularly in the third quadrant, are greatly improved, allowing operation of the attenuator at the necessary levels of input signal.

The sum and difference signals are obtained from IC 1 and IC 3 (see circuit diagram, Fig. 5). An MC 1495 analog multiplier is used as the synchronous detector because of its good transconductance versus frequency response; 200  $\Omega$  resistors have been placed at the inputs of the multiplier to avoid high-frequency oscillations due to negative input impedance. The sum signal input is operated at a saturated level in order to make the product independent of beam intensity.

Before making the product, the difference signal is amplified by a two-stage Avantek broad-band integrated amplifier. A third Avantek stage is used to produce a suitable voltage gain and a 50  $\Omega$  output from the closed-orbit signal suppressor.

The active filter following the multiplier, as well as the phase-splitting and driving stages for the FETs, are made with a conventional operational amplifier.

The reference voltage determining the operating point of the FET attenuators is obtained from the voltage divider R26,R41, the potentiometer Pl being an offset control for the multiplier and d.c. amplifying stages.

#### 3. CHARACTERISTICS

- Two a.c. coupled inputs.
- 3 dB low-frequency corner: 5 kHz.
- Input impedance at balance: 50  $\Omega$ .
- Maximum input signal level: 1000 mV \_\_\_\_\_\_.
- Carrier fundamental frequency: 3 to 8 MHz.
- Suppression bandwidth: determined by  $C_9$  and  $R_{40}$ .
- Voltage gain at output (1) for non-suppressed differential input signals<sup>\*</sup>):
  35 dB min. for three-stage version,
  22 dB min. for two-stage version.

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<sup>\*)</sup> Note: For experimental purposes two versions have been made. A low-gain version with a two-stage GPD Avantek amplifier for output (1); and a high-gain version with a three-stage GPD Avantek amplifier for the same output. It should be taken into account that a phase inversion exists between the output signals of the two versions. When interchanged, the input cables to the unit must be inverted.

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- Suppression factor for sinusoidal input signals at 8 MHz carrier frequency, with 1.25 amplitude ratio: 34 dB min. at 500 mV nn common-mode input signal.
- Output impedance: 50  $\Omega$ .
- Output (1): Suppressed signal output, to be used for transverse feedback loop.
- Output (2): Observation output, with lower suppression factor.

#### 4. CALIBRATION PROCEDURE

#### 4.1 Internal switch in open-loop position

- a) Apply a 5 MHz, 20 mV signal to one of the inputs, terminating the other one with 50  $\Omega$ . Gradually increase the input level, observing the output signal.
- b) Verify that there is a 3  $V_{pp}$  min. saturation level of the GPD amplifier.
- c) Check the gain value of  $35 \pm 3$  dB.
- d) Repeat the above measurements, interchanging the inputs.

#### 4.2 Internal switch in closed-loop position

- a) With both inputs 50  $\Omega$  terminated, adjust the offset potentiometer Pl until "zero" is reached on a 3 V voltmeter range at test point TP.
- b) With a phase splitter (50  $\Omega$ ), apply a 8 MHz 500 mV signal to both inputs and observe the output with a 50  $\Omega$  input scope.
- c) Set trimmers  $C_3$  and  $C_7$  to their minimum capacitance value. Identify the one that reduces the output signal and use it to adjust a minimum on that signal. A strong second harmonic component should be observed (see Fig. 6b).
- d) Verify that when reducing the input level by 10 dB steps, the output reduces smoothly. If not, retouch potentiometer P1 in order to get the minimum output signal at minimum input level.
- e) Connect the splitter, with 2 dB difference in its output levels (specially made for this purpose), to the inputs. Care must be taken that the length of the cables used is matched within 0.15 ns (0.5 degrees at 8 MHz).
- f) Adjust a 1100 mV signal at the input of the splitter.
- g) Connect the spectrum analyser to the output. Verify that when inverting the inputs, the first harmonic of the output signal remains at approximately the same level. If not, retouch the trimmers used in step (c) (see Fig. 7).
- h) Short-circuit switch B with a wire in order to assure closed-loop operation of the module.

- 4.3 Label the module to show that it has been checked and adjusted.
- 4.4 Pairing of FETs in case of replacement

The FETs in the self-balancing bridge have been matched within  $\pm 5\%$  of their resistance values at the quiescent point ( $V_{GS} \approx 650$  mV). In spite of the self-adjusting property of the bridge, it is worth making this matching in order to get a symmetrical operation of the circuit around the equilibrium point. The measurement should be done at 100 kHz and with a signal not exceeding 200 mV<sub>DD</sub>.

#### 5. MEASUREMENTS

- Fig. 6) Output (1) waveforms, when the inputs are fed respectively with 500 mV pp and 625 mV (a ratio of 1.25) 8 MHz signals.
  - a) Open-loop operation. Voltage scale: 500 mV/div.
  - b) Closed-loop operation. Voltage scale: 20 mV/div.
- Fig. 7) Output (1) frequency spectra. (Same inputs as in Fig. 6.) a) Open-loop operation. (A second harmonic of the input signal can be observed.)
  - b) Closed-loop operation. A suppression factor of 42 dB on the fundamental is attained.

#### Acknowledgements

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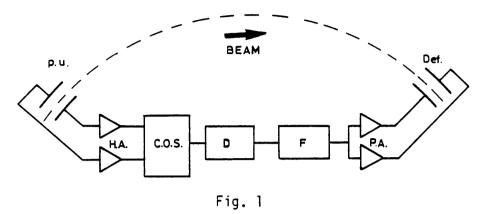
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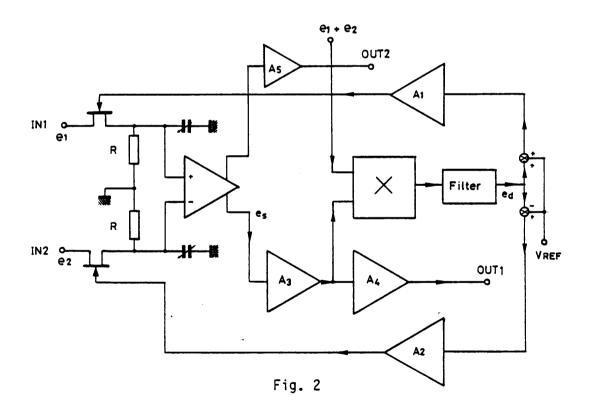
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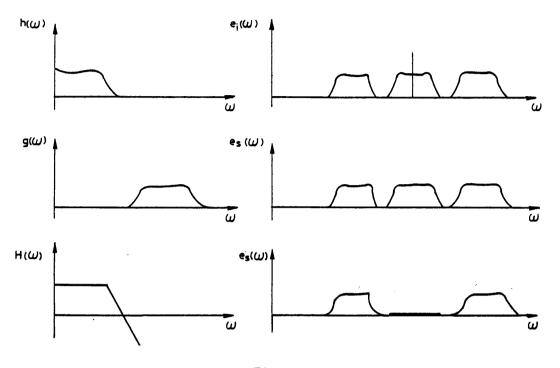
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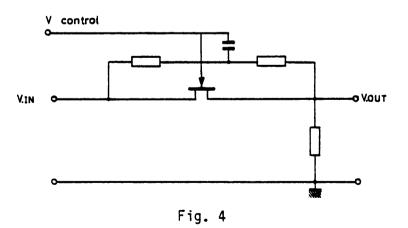


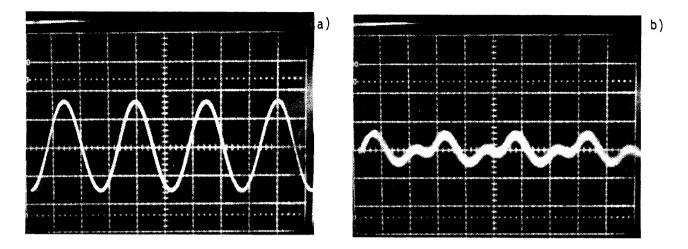
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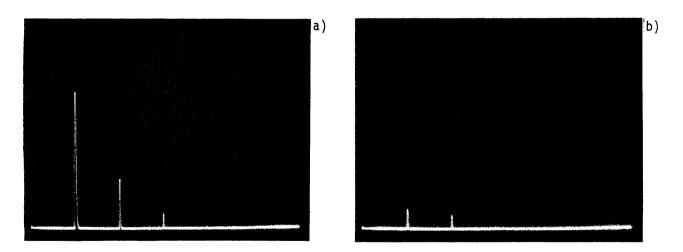














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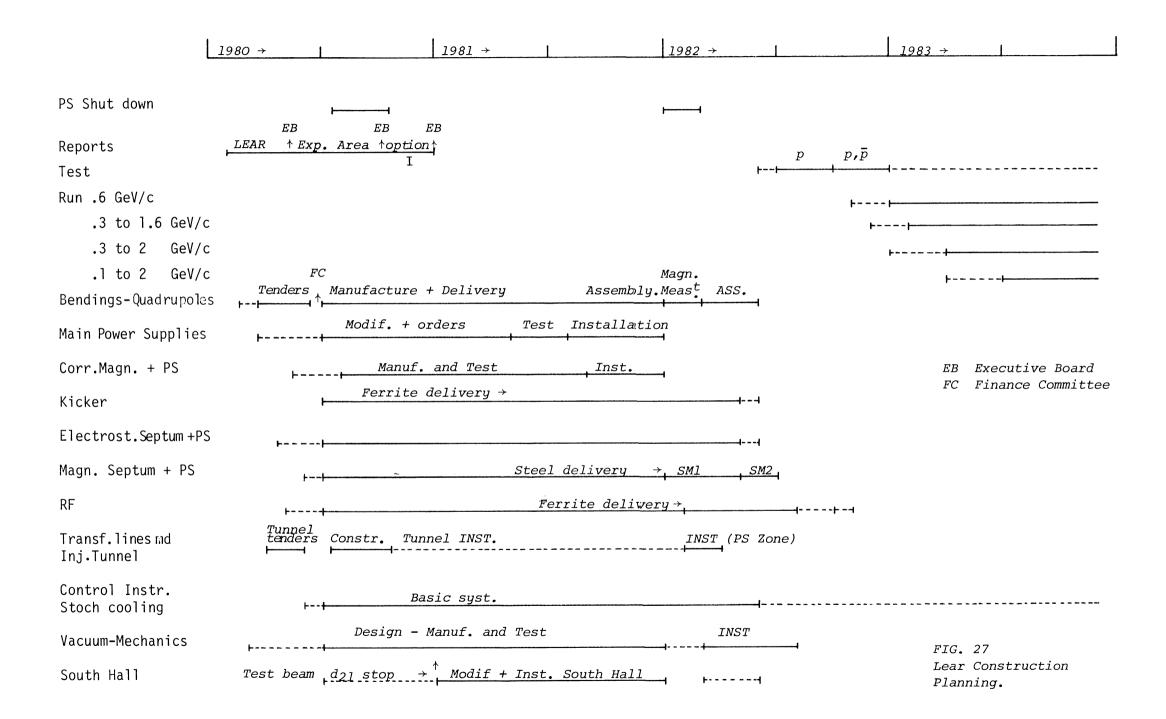


Fig. 6

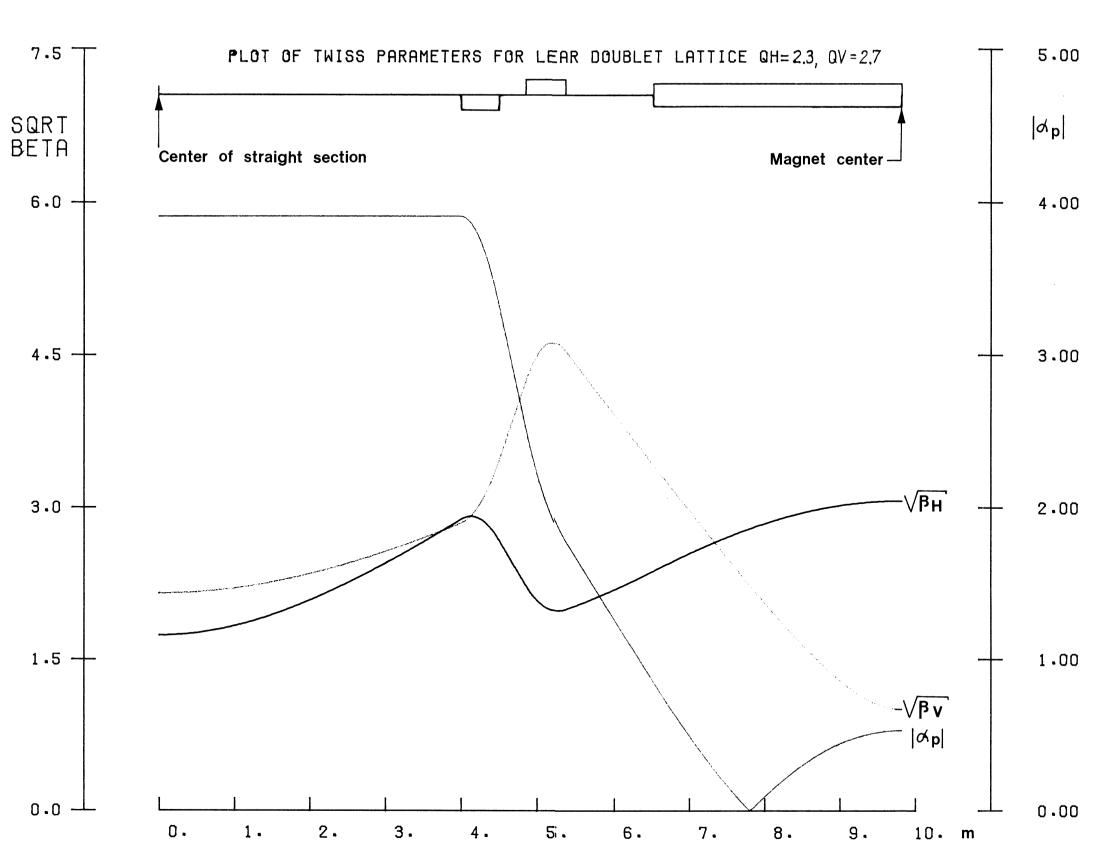


Fig. 8

