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# ASIC survival in the radiation environment of the LHC experiments: 30 years of struggle and still tantalizing

Federico Faccio

*CERN, EP department, Esplanade des Particules 1, Meyrin, 1211, Switzerland*

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ABSTRACT

The radiation environment at the CERN Large Hadron Collider (LHC) poses an unprecedented challenge to the reliable functionality of the electronics components composing the detector systems. Starting from the beginning of the 90s, a large effort has been dedicated at CERN and in the collaborating institutes to develop, produce and deploy Application-Specific Integrated Circuits (ASICs) tolerant to all types of radiation effects: Total Ionizing Dose (TID), Single Event Effects (SEE) and Displacement Damage (DD). This article briefly describes the approaches and methodologies that the High Energy Physics community developed or adopted for that purpose over the last 30 years.

## 1. Introduction

With the construction of the LHC accelerator, a new chapter in the book on the electronics for High Energy Physics has been opened. This high luminosity hadron collider produces an unprecedented radiation background in the detector systems built around the points where the accelerated protons collide head-on, particularly hostile to the reliable functionality of electronics devices. As an example, the radiation background in one of the two general-purpose detector systems (ATLAS) at the LHC is described in Table 1, while a transverse view of the other (CMS) is shown in Fig. 1. to illustrate the position of the different dedicated detector layers. At the beginning of the 90s it was already clear that the electronics of the trackers needed to be radiation tolerant to unprecedented levels, and that the HEP community had to acquire new competences on radiation effects in electronics devices and circuits. Things only got more challenging with the approval of the High-Luminosity LHC upgrade, with the consequent 10× increase in the radiation background.

This article tries to provide a short historical perspective of this long period of time, with a focus on the difficulties and successes in the effort of developing and producing Application-Specific Integrated Circuits (ASICs) for the physics experiments at the LHC and HL-LHC. Following a chronological flow, chapter 2 illustrates the efforts that the HEP community deployed to develop and qualify ASICs satisfying the radiation requirements of the LHC detector systems. It shows how, after an initial effort on the radiation-hard CMOS and biCMOS processes of the time, most of the developments took place in a commercial-grade quarter-micron CMOS technology where systematic design techniques to improve the radiation tolerance were used. This chapter also covers the establishment of a practical test procedure to qualify circuits against the risk of Single Event Effects. The procedure lies its foundations in a simulation methodology developed to estimate the error rates in the mixed-field and high-energy particle field of the LHC radiation environment. With the electronics for the first generation of LHC experiments ready, Section 3 guides the reader through the long development cycle of ASICs for the detector upgrades, with emphasis on the High-Luminosity LHC program that foresees an increased luminosity of the accelerator determining an even more severe radiation background. Here the 130 and 65 nm CMOS nodes were adopted, with the discovery of complex radiation effects manifesting at ultra-high TID levels and eventually traced to basic mechanisms taking place in the parasitic oxides used in transistors' manufacturing. Finally, in chapter 4 the very specific case of ASICs designed for power distribution devices such as DCDC converters is treated. This chapter eloquently shows how high-voltage rating and radiation tolerance are difficult to obtain at the same time.

The author is aware that the events are reported from his viewpoint and that the story is thus incomplete, but it should be a coherent and readable one from which hopefully the young members of our HEP community could learn.

## 2. Towards the first generation of LHC experiments

### 2.1. Radiation hard CMOS processes

Even before the convergence of the LHC experimental program to the ATLAS and CMS experiments we know today, it was clear that the

*E-mail address:* federico.faccio@cern.ch.

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inner detector layers at these general purpose apparatuses required equipment capable of surviving to unprecedented levels of radiation[1] (10 Mrad and $1-3\times10^{14}$ n/cm$^2$). Already in September 1991, before the birth of the ATLAS collaboration in 1992, projects aimed at evaluating some of the available radiation-hard CMOS processes for ASIC design were on-going. These CMOS technologies had been developed for military and Space applications during the cold war period, and were only used to produce a handful of wafers yearly. The most notable efforts, to which one has to add less documented studies that included also JFET, bipolar or even technologies on Silicon-on-Sapphire substrates, concentrated on processes developed in the US or in France. The typical read-out ASIC of an early 1990 HEP experiment embedded mainly analog functions, and was a direct descendant of the fully analog circuits of the 80s, thus most of these evaluations were mainly targeting the analog performance of the transistors in the technologies, and in particular the radiation-induced noise degradation. Experimental test benches to measure noise in the 1 kHz–1MHz frequency range blossomed in several Institutes around the globe. Technologies that were studied in some details in the beginning of the 90s included three CMOS on SOI substrates: the Honeywell RICMOS_IV 0.8 μm [1], the Thomson TCS HSOI3-HD 1.2 μm [2], and the DMILL 0.8 μm [3] – the latter offering a combination of CMOS, bipolar and JFET transistors. The popularity of the SOI substrates in this generation of radiation-tolerant CMOS was justified by the strong bias, driven by space and military applications, to improve the resilience of the circuits to radiation effects potentially triggered by the energy deposition by a single particle (Single Event Effects, SEE). Additionally, the Harris AVLSIRA 1.2 μm on bulk substrate was studied [4]. Although the workhorse was the measurement of individual transistors before and after irradiation, some of these works went as far as developing advanced prototype readout circuits for the ATLAS or CMS trackers, for which the use of the Harris or DMILL technologies were the baseline solution until the late 90s. Viewed from 2021, progress was very slow: these studies spanned over more than 5 years and eventually only the DMILL technology was used—and for a minority of the LHC phase 1 ASICs. To justify this apparent slowness, the modern reader has to consider that in the early 90s virtually no researcher had a personal computer for individual use, and there was no Google browsing—there was no WWW to build that on, actually. The way to get state-of-the-art knowledge was the pedestrian path to the local scientific library, scan through volumes of IEEE TNS, and queue up at the local Xerox machine for a copy to bring back home and underline. Transistors measurements were performed with instruments requiring floppy disks for data storage, and extraction of their electrical parameters demanded a curve tracer (the 6-color model at CERN took about 5 min to put an Id/Vg curve on paper) and the patience to extrapolate the curves manually with the help of pencil and ruler. Irradiation for TID studies was only performed at dedicated facilities, requiring the transport of the equipment to keep transistors under bias. From CERN, we organized 4 days-long travels to the premises of CEA in Saclay (close to Paris, France) to expose test structures to $^{60}$Co gamma rays at the "Pagure" facility of a commercial service provider, and only once we dared transport the expensive semiconductor parameter analyzer HP4145B and take measurements locally. Irradiation to 10 Mrad required normally 3 days at the facility. Switching the connections to each transistor without a switching matrix was done manually. This all looks like Jurassic Park today, where with automatized test systems and in-house X-ray machines we can complete the full characterization of a test structure with some 20 individual transistors irradiated with different bias at 100 Mrad at any temperature (−30 to 100° C) in the first 24 h after having received the bare die from the Foundry. But this was life back in the early 90s. These years were scattered with a few successes and many setbacks. These low-volume technologies basing their radiation hardness on processing details were ill-equipped to produce hundreds of wafers with good parametric and radiation response reproducibility. Yield was often an issue, and large variation in lot-to-lot radiation tolerance was sometimes reported. Cost was also a big problem for the HEP community: the fixed development and radiation qualification cost had to be amortized on a low-volume production. On top of that, the vastly different mindset of HEP researchers and commercial representatives of companies heavily sponsored by military funding was prone to create misunderstandings and wrong expectations, making long-term trustful relationships difficult. As a result, and with the additional simultaneous decrease in military funding due to the end of the cold war, many radiation-tolerant technologies disappeared and most designers of HEP ASICs were very happy to change course as soon as an alternative appeared (subject of the next chapter). Only the radiation-hard DMILL technology was eventually used to produce ASICs installed in the LHC, and in particular for different ATLAS detector systems. Some examples are the ABCD FE chip for the strips [5], the ASDBLR FE chip for the TRT [6] and the TTCrx communication chip (optical receiver) for the distribution of timing, trigger and control in the LHC [7].

### 2.2. Hardness-By-Design (HBD)

In this situation, it is not surprising that in the mid 90s the HEP community was looking for alternative approaches to develop the LHC ASICs. The progress of commercial-grade CMOS technologies, helped by the physics of the radiation-induced damage in oxide layers and a pinch of ingenuity, fully changed the game.

#### 2.2.1. Previous work in the radiation effects community

The extensive study of TID effects on CMOS transistors carried within the radiation effects community in the 70s and 80s resulted in a good understanding of the physical mechanisms affecting the electrical performance. Damage could result from ionization in the gate oxide itself, or in the thicker isolation oxide surrounding the active transistor (LOCOS or STI) and was traceable to charge trapping in defects in the insulator or at its interface with the silicon. Research carried by N.Saks and co-workers at Naval Research Lab (NRL) demonstrated unambiguously that both mechanisms strongly depended on the oxide thickness [9,10]. While for large $t_{ox}$ the radiation sensitivity decreased with the thickness (damage proportional to $t_{ox}^n$, with n close to 2), an even steeper decline was found for $t_{ox}$ below about 12 nm as illustrated in Fig. 2. This work on thermally grown laboratory-grade oxides strongly suggested that also commercial-grade gate oxides, thermally grown as well, would become less prone to radiation-induced damage for each CMOS generation, since Dennard's scaling required the gate oxide thickness to decrease.

However, both the LOCOS isolation oxide and the STI that replaced it from the 250 nm node and surrounding the transistors were not deemed to scale down, and appeared to remain a limiting factor to the radiation tolerance: positive charge trapping in these oxides opens leakage current paths between source and drain of n-channel transistor, or between adjacent n-doped regions at different potential. But maybe this leakage could be prevented by a modification of the transistors' design, as suggested by the work performed at RCA Corporation and published in 1977 by Dingwall and co-workers [11,12]. RCA introduced what they called C$^2$L, or Closed COS/MOS Logic, devices where the drain was fully enclosed by the gate as shown in Fig. 3. This produced transistors with superior performance and, in their words, "circumvented the need to guardband individual MOS transistors, thus achieving low parasitic leakage over a 3–15V operation range".

[1] The definition of survival here strongly depends on the functions integrated in the circuit, and on the system surrounding it. As an example, a TID-induced leakage current increase is acceptable as long as the circuit remains functional and the power distribution system is capable of providing the excess current. The degradation of analog parameters can also be tolerated to an extent that strongly depends on the system before the performance of the detector is affected.

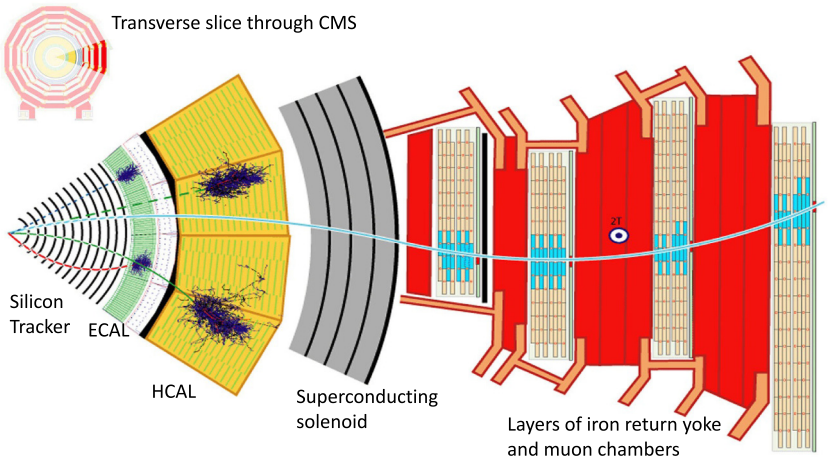


**Fig. 1.** Transverse cut through the CMS detector system, illustrating its composition of several dedicated detector layers. The silicon tracker closer to the interaction point is itself split into a pixel and a strip detector, each composed of several layers intended to enable the reconstruction of the particles' track. ECAL is the electromagnetic calorimeter, while HCAL is the hadronic calorimeter. Muon chambers are dedicated to the detection of these lightly interacting particles that manage to travel from the interaction point beyond the calorimeters, that instead stop electrons and photons (ECAL) as well as hadrons (HCAL). The whole system is in a strong magnetic field bending the trajectory of charged particles to help their identification. In the case of CMS, the field is created by a superconducting solenoid. The track of different particles is shown in the image.

**Table 1**
Radiation environment expected from simulation in the different detector layers composing the ATLAS experiment at the LHC accelerator over an operation period of 10 years [8]. The distance of the detector from the interaction point where the proton beams collide increases from top (pixel and Silicon Central Tracker, SCT, are parts of the silicon tracker) to bottom (muon detector). For each detector, the numbers refer to the layer or location where the radiation field is the most intense. The neutron fluence is expressed in 1-MeV equivalent neutrons, while the charged hadron fluence only counts particles above 20 MeV of energy.

| Detector zone | Total dose [rad] | Neutron fluence [$cm^{-2}$] | Charged hadron fluence [$cm^{-2}$] |
|---|---|---|---|
| Pixel barrel | $113 \times 10^6$ | $1.62 \times 10^{15}$ | $2.3 \times 10^{15}$ |
| SCT barrel | $7.8 \times 10^6$ | $1.6 \times 10^{14}$ | $1.2 \times 10^{14}$ |
| ECAL barrel | $4.8 \times 10^3$ | $1.8 \times 10^{12}$ | $3.8 \times 10^{11}$ |
| HCAL | 380 | $2.7 \times 10^{11}$ | $6.7 \times 10^{10}$ |
| Muon detector | $23 \times 10^3$ | $6.4 \times 10^{12}$ | $1.3 \times 10^{12}$ |

These ideas, and the consequent possibility to use a commercial process with modified design techniques to achieve radiation tolerance, reached the ears of E.Heijne of the CERN Microelectronics group in the period 1981–87, when during his travels to conferences and visits to research laboratories he had the opportunity to discuss with N.Saks (NRL) and R.Smeltzer (formerly at RCA). Only in the following decade, however, gate oxides of commercial-grade CMOS processes became sufficiently thin to envisage multi-Mrad tolerance. In 1996 times were mature for that, and these ideas sown in the CERN Microelectronics group by E.Heijne grew to an exploratory work using the 0.7 μm Mietec technology of the time. Different layout techniques previously proposed to eliminate the source–drain leakage current were considered, like those published by Hatano and Takatsuka (Toshiba) and based on the separation of the source/drain diffusion from the thick field oxide via a thin field oxide [13,14]. The test structures hurriedly designed by a master degree student (G.Anelli) and the author of this paper over a week-end also included the first circular transistor laid out at CERN. The advantage of this layout, later called Enclosed Layout Transistor (ELT), resided on the easy portability to different technologies and the lack of violation of the Foundry's design rules. Measurements confirmed that the source–drain leakage was completely eliminated in this transistor, and this research was extended to other and more advanced technologies in the following 2 years. An example of the effectiveness of the ELTs to eliminate source–drain leakage in 0.5 μm technology is shown in Fig. 4. CERN was not alone to follow this thread: in 1996 Dr. Alexander from Mission Research Corporation presented a full chapter of the NSREC short course on this topic, producing a document that served as a precious reference to us [15]. Active research was also carried by the Aerospace Corporation in California, as witnessed by the numerous papers published on the subject by R.Lacoe and co-workers, with whom we had regular exchanges [16–23]. Hardness By Design (HBD, sometimes also called RHBD where R stands for Radiation) is the acronym that was use in the community to denote circuits having attained radiation hardness without any intervention on the commercial-grade technology, but only via the systematic use of dedicated design techniques.

### 2.2.2. *From first measurements to Foundry Service*

Recognizing the need to establish stronger contacts with the radiation effects community, and of more resources to pursue the very promising research on the use of ELT transistors in an advanced CMOS technology, the CERN microelectronics group promoted a 3-years R&D program that was approved by the CERN DRDC (Detector Research and Development Committee) as RD49 – "RADTOL" [24]. Participants included numerous institutes in HEP but had also, as associated specialized institutes, collaborators with long-standing expertise in radiation effects like ESA, CNES, Montpellier University and CEA. Spokespersons were E. Heijne, P. Jarron (CERN) and A. Paccagnella (DEI, Padova University). The periodic collaboration meetings registered the participation of experts from these and other Institutes, favoring knowledge transfer to our community that was hitherto marginally confronted to the electronics reliability in a radiation environment. Within the collaboration, it was possible to continue the research on ELT transistors and deeper submicron technologies. Test structures were implemented in 0.5, 0.35 and 0.25 μm technologies confirming that the gate oxide tolerance increased in the thinner-gate more advanced processes [25]. Measurements confirmed also that CMOS transistors were not sensitive to displacement damage effects, even up to the fluence of neutrons

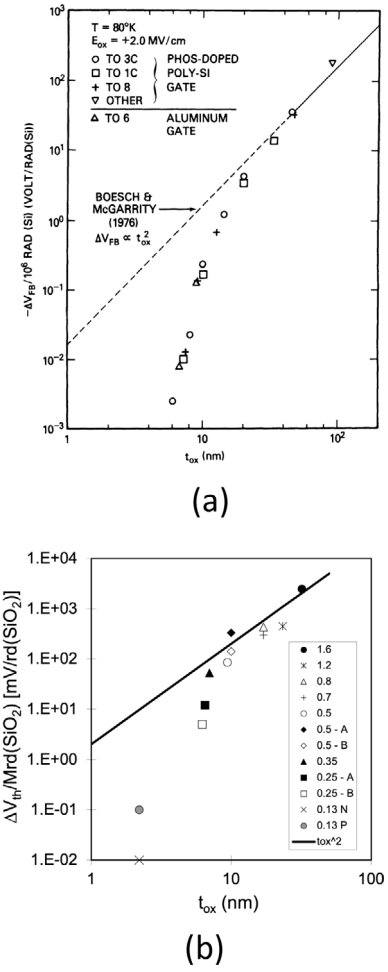


**Fig. 2.** (a) The shift of the flat-band voltage due to positive charge trapped in the gate oxide decreases with the gate oxide thickness in laboratory-grade oxides at 80 °C in [9]. (b) The same trend is verified for the threshold voltage shift of transistors in commercially available CMOS technologies. The nodes in μm are indicated in the inset: with every smaller node, the gate oxide thickness is decreased. In both cases, the straight line is a quadratic dependence guide for the eye.

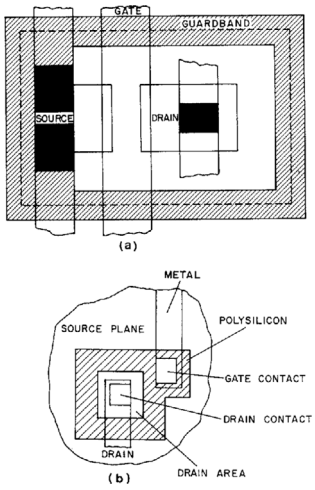


**Fig. 3.** Standard and Ringed (Enclosed) transistors developed by RCA already in 1977. *Source:* From [11].

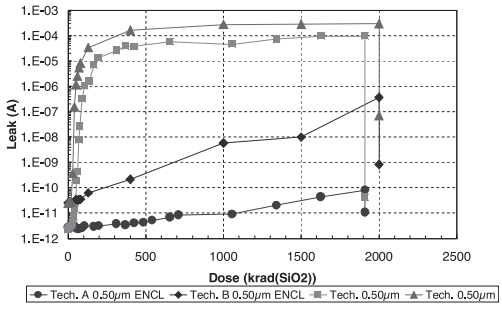


**Fig. 4.** Difference in the drain–source leakage current between standard and ELTs in two different 0.5 μm technologies. The residual leakage increase of ELTs is due to a net decrease of the threshold voltage of the transistors with TID, and not to the parasitic lateral transistor. The last point of each curve shows the effect of post-irradiation high-T annealing.
*Source:* From [25].

of the LHC pixel detectors. This has since been observed in all CMOS processes and even for the more demanding HL-LHC environment—and for this reason displacement damage studies are not mentioned in this article for low-voltage CMOS technologies. The quarter micron technology with a gate oxide thickness of about 5 nm outperformed all others, and was just being commercially introduced at the time. Early access to the IBM foundry was promoted by A.Marchioro, who was instrumental in the establishment of a collaboration and then commercial relationship with this manufacturer. ELT transistors designed in this process demonstrated negligible parametric or noise shifts after the 10 Mrad target TID [26]. Moreover, the systematic use of p+ guardrings to separate n-doped diffusions was very efficient to prevent inter-device leakage currents. All this eloquently showed the way forward: we had our breakthrough. From the design of an individual ELT transistor to the development of a multi-million transistors ASIC mass-produced (hundreds of wafers) with high yield and reliably working the travel is long. This required a team effort where many members of the RD49 collaboration contributed in a significant way, the main work being done in the CERN microelectronics group. A design kit was developed with ELT p-cells (see examples layouts in Fig. 5) where the size of the transistors was compliant with a model for the effective W/L of this specific enclosed geometry experimentally verified [27,28]. The principle of the model is shown in Fig. 6. A small but sufficiently rich digital library was created, documented and distributed [29]. A first ASIC, to be used as a demonstrator, was successfully designed using this approach [30]. Relevant publications for this work are [31–35]. Having also defined a legal and commercial framework allowing CERN to produce and distribute wafers in the IBM fabs, also on behalf of collaborating HEP institutes, times were mature to start what gradually became the largest production of Hardness By Design (HBD) circuits ever.

CERN started to propose Multi-Project-Wafer (MPW) runs in the technology where circuit designers from the HEP community could prototype at low cost their circuits. With the formidable results from the first ASICs produced with this approach becoming available, a snowball effect started and the majority of the LHC ASICs were swiftly moved to the IBM technology. The CERN Foundry Service, the interface between the HEP ASIC community and a wafer supplier, was born—and it is still alive and kicking more than 20 years later! This was a vast success, and it is not exaggerated to state that this was the key instrument enabling the LHC experiments to affordably produce their ASICs. Cost, density, electrical performance and yield were all largely better than for the (very few) radiation-hard technologies still surviving at the time. During the 5 years or so when most of the LHC wafer volume was produced some occasional problem occurred, the most notable being a considerable decrease in yield in some lots of some designs, or in the whole production of other designs. This was traced down by the manufacturer itself after the investment of considerable

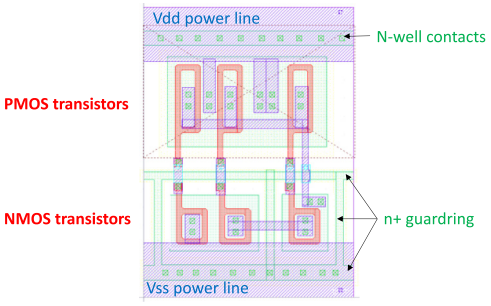


**Fig. 5.** Example cell, a NAND with 3 inputs, from the radiation-tolerant digital library developed at CERN in the quarter micron technology. NMOS need to be enclosed, while PMOS are laid out that way to match the horizontal pitch of the NMOS. An n+ guardring surrounds all n+ sources/drain at different potential, as well as the whole p+ region containing the NMOS transistors.

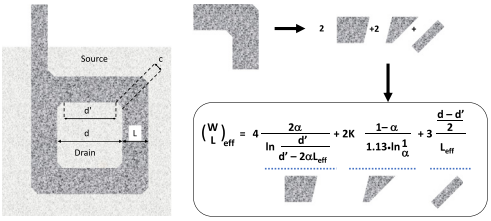


**Fig. 6.** Model to estimate the effective W/L of ELT transistors, valid only for the specific shape with corners cut at 45 degrees as in the image. Each corner is split in 3 components, for which an equivalent W/L is calculated.
*Source:* From [31].

**Table 2**
Summary of the activity of the CERN Foundry Service in the period 2000–2008. Successive prototypes of the same ASIC are re-counted in the total number of ASICs in MPWs. Some of the dedicated Mask Sets were shared amongst different ASICs. Adjusted for inflation the total expenditure would be close to 14 MChF of 2022, but it is important to consider that orders were issued in USD, and 1 USD was quoted up to 1.8 ChF at that time while is close to parity now; moreover inflation was considerably higher in USD than in ChF.

| Number of MPW runs | 16 |
|---|---|
| Total number of ASICs in MPWs | 244 |
| Number of Institutes participating in MPWs | 20 |
| Number of dedicated Mask Sets | 24 |
| Number of wafers produced | 3100 |
| Total expenditure for all the above | 13.3 MChF |

resources for investigation, and some processing steps were modified as a consequence bringing the yield back where one would expect. It is important to mention this episode as a demonstration of how important a good relationship with the supplier might be in case problems arise—and IBM was remarkably supportive. To conclude this section, and to illustrate the relevance of this Foundry Service activity, it is instructive to report some relevant numbers for the period 2000–2008 where the vast majority of the designs using the quarter micron technology were developed and produced. This is done in Table 2 and Fig. 7. The total expenditure for engineering and production wafers, for more than 24 ASICs, is less than three times the cost of the ABCD wafers in the radiation-hard DMILL technology alone.

### 2.3. Single event effects in an accelerator environment

SEEs are radiation effects initiated by the energy deposition from a single particle traversing the integrated circuit, and are thus of a stochastic nature. Their consequences vary from the introduction of a temporary current/voltage transient to the permanent destruction of the full circuit. If the threat posed by SEEs to the reliable functionality

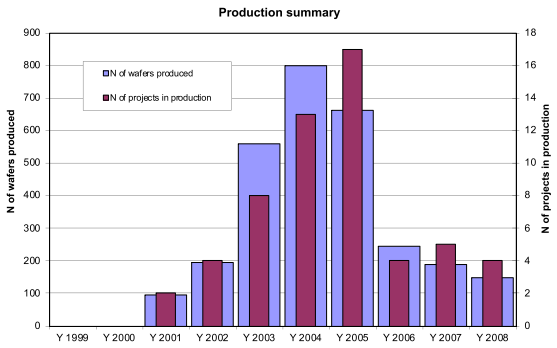


**Fig. 7.** Summary of the production of LHC ASICs in the quarter micron process, via the CERN Foundry Service, for the period 2000–2008. Some of the "projects" included different ASICs.

of electronics was recognized since the beginning for the LHC trackers, it was instead initially ignored – with some exceptions – for other regions of the experiments and for the LHC accelerator electronics. This situation can easily be explained by the lack of instruments enabling an estimate of the rate of SEEs in the LHC hadron-dominated particle environment, leaving space to the belief (or wishful thinking) that occasional data errors could be easily compensated by the inherent redundancy of the detector systems. At the same time, the evidence of proton- or neutron-induced destructive events like Single Event Latchup (SEL) or Burn-out (SEB) was insufficiently known by our community to compel a systematic radiation qualification procedure covering also SEEs for all the LHC electronics. While to the engineers participating in conferences like NSREC and RADECs and exposed to ideas in the Military, Avionics and Space fields the need to qualify LHC electronics for SEEs appeared an evidence, it was impossible to support this need and mobilize the large resources for the task without an indisputable quantitative argument. Luckily, some previous study on the impact of atmospheric or impurity-emitted neutrons in commercial electronics components existed and was inspirational for the development of a tool that changed the picture entirely.

#### 2.3.1. Previous work in the radiation effects community

The semiconductor industry was confronted in the late 70s with soft errors from alpha particles eventually traced to the presence of radioactive impurities in the materials used to produce or package memory chips. After Intel reported operational errors in 16 kbit DRAMs and traced it to contamination from radioactive elements in the water used by a ceramic packaging factory in Colorado [36], IBM setup a task force to study soft fails in 1978 [37]. In the following years, this team of scientists in IBM acquired a unique expertise and developed for the first time tools to simulate the physical phenomena and calculate error rates. Only several years after these facts, and with an already diminished team, IBM documented them in a formidable reference issue of their "Journal of Research and Development" in 1996. This collection of review papers described, amongst other very relevant details, the physics mechanisms behind the charge deposition in the circuits leading to single events [38] as well as a modeling tool called the Soft-Error Monte Carlo Model (SEMM) specifically created to estimate the probability of charge deposition events to occur [39,40]. This tool included Monte Carlo modeling of both the nuclear interaction of the incoming particles with the IC material and the consequent charge transport and collection to produce charge collection probability curves. This information was then combined with circuit characteristics, such as the critical charge and the connection between different nodes, to compute the Soft-Error-Rate in any environment. This was a unique tool that, if available, would have surely and rapidly confirmed the SEE threat posed by the LHC radiation environment to the safe operation of ICs.

To the same purpose of confirming the SEE risk, another very relevant work was being conducted by the group of Dr. E. Normand

at Boeing Defense and Space in Seattle. Their effort was targeted at collecting data and developing predictive models for single event effects in commercial electronics in avionics or in ground applications. They demonstrated that atmospheric neutrons played a key role in the observed soft errors in avionics [41] and terrestrial applications [42]. Dr. Normand himself visited CERN in a couple of occasions and presented his findings in front of a large audience, which contributed enormously to diffuse the idea that atmospheric neutrons, whose flux is orders of magnitude lower than the flux of high-energy neutrons in even the experimental LHC cavers, can pose serious reliability problems to integrated circuits.

### 2.3.2. How to estimate error rates in the LHC environment

The above described SEMM-based method developed at IBM seemed the ideal path in view of quantifying the risk of SEEs in the LHC environment, but required expertise beyond the field of electronics engineering. As was the case for the IBM work, contribution was required from particle physicists mastering the rare software packages that at the time could reliably simulate the nuclear interaction of hadrons in semiconductor materials, as well as calculate the energy deposition from the produced fragments. Such a knowledgeable person existed at CERN: M.Huhtinen was at the time using the Fluka simulation package to compute the radiation background in CMS, and had a strong background in radiation effects in silicon detectors. Merging our diverse competences and with the initial additional help of C. Detcheverry, a student from Montpellier University specialized in SEU effects in CMOS technology at CERN for a 6-months internship, we started in 1997 the work that eventually converged to the development of a powerful simulation method. The final tool was built on the Fluka and TRIM codes, where the first was used to simulate the interaction of the particles present in the LHC radiation environment with the materials composing the ICs (essentially Silicon) and the second to transport the produced fragments in the circuit and calculate the energy deposited via ionization mechanisms. The method required an hypothesis on the volume surrounding any potentially sensitive node of the circuit, all charge deposited inside the volume being able to contribute to the radiation-induced perturbation (SEE). As already done by IBM, we also used an RPP (Rectangular ParallelePiped) approximation that, although strongly far from the physical reality, yielded and continues to yield today in a number of similar simulation-based approaches very reasonable results. This approximation is valid for Single Event Upsets (SEU) only, where the digital nature of the disrupted circuit allows for such crude model of reality. For this reason, the method was not intended to estimate rates for SEL (Latch-up), SEB (Burnout) or SET (Transients in analog ICs) and should not be used for that purpose. The methodology and an example result are illustrated in Fig. 8.

Once the simulation toolset was assembled, it helped clarifying considerably the role of every particle species (protons, neutrons, pions) as well as the influence of their initial energy on the SEU rate any IC could experience. It also provided the means to estimate the error rate in a hadron-dominated environment from data taken at Heavy Ion irradiation facilities, that are typically used to characterize the sensitivity of electronics to be used in Space missions. This was particularly useful in providing a benchmark for the method, thus proving its reliability in yielding reasonable estimates. Data was gathered in the literature for electronics components for which both Heavy Ion and mono-energetic proton irradiation runs were performed. Starting from the SEU cross-section measured with Heavy Ions, our method was used to estimate the expected result during a proton irradiation. The comparison with the experimentally available data indicated a match to within a factor 2 when a SV size of 1 × 1x1 $\mu m^3$ was used. This provided the necessary confidence to document the method as a CMS note first [43] and as a full paper eventually published in NIM A in 2000 [44]. Several very relevant conclusions were highlighted, the most important concerning the large similarity in SEU rates that sensitive ICs would have in a mono-energetic proton environment and

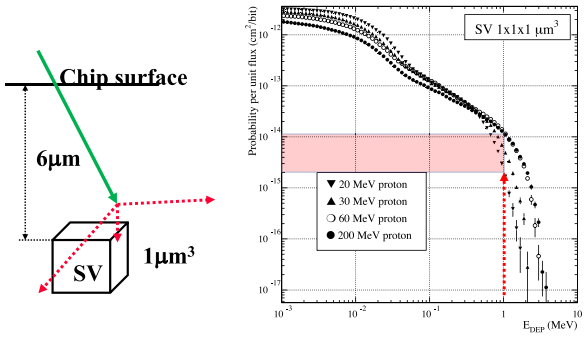


**Fig. 8.** The simulation methodology to estimate the SEU rate in LHC is based on a MonteCarlo approach. The geometry to the left is used, where a Sensitive Volume (SV) cube of 1 μm side situated 6 μm below the chip surface represents the only region where the charge deposited by the incoming particles contributes to the SEU. Incoming particles (green arrow) interact in the SV or in its surroundings, producing secondaries (red dotted arrows) that are transported in the material. The energy deposited by secondaries along their track in the SV is calculated, and probability curves as the one shown to the right produced. Knowing the energy deposition threshold for the SEU to occur it is possible to read in the chart the probability for an energy deposition event equal or above the threshold. The example shows that, for a threshold energy of 1 MeV, probabilities in the range of $2x10^{-15} - 10^{-14}$ are calculated in mono-energetic proton environments of 20 to 200 MeV.

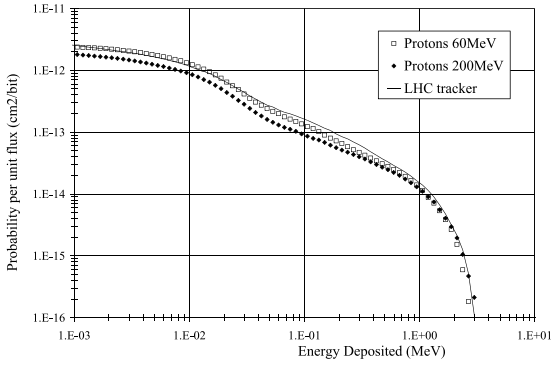


**Fig. 9.** Probability curves for energy depositions in the same Sensitive Volume (a cube of 1 μm side), in mono-energetic 60 and 200 MeV beams as well as in the LHC trackers. Above a few hundred keV of threshold, the probability is very similar in the three environments.

in an LHC-like environment—which includes many particles with a wide energy distribution.

This similarity, shown in Fig. 9, clearly indicated a straightforward strategy to qualify components to be used for the LHC experiments against the risk of SEU-induced disturbances: the cross-section measured during a test with protons with energy equal or larger than 60 MeV could be directly assumed to be valid to estimate the error rate in the LHC.

### 2.3.3. Testing the LHC electronics for SEEs

The conclusions from the simulation-based work described above have to be put into the context of their time to understand their impact. In the last years of the 90s the electronics systems for the LHC experiments were generally well defined, their components selected and often assembled in advanced prototypes. The selection process included radiation tests for Total Ionizing Dose and (if needed) Displacement Damage, but ignored the threat posed by SEEs—simply put because nobody knew how to qualify components for a radiation environment as complex as the LHC one. The simulation work provided the much needed knowledge, and the qualification procedures for the electronics for the LHC experiments were quickly modified to include SEU tests with mono-energetic proton beams. From the SEU cross-section $\sigma_{protons}$ measured in the beam, and calculated as the ratio between the number

of errors and the integrated proton flux, the estimated error rate in the LHC could be directly computed with the multiplication by the instantaneous flux of all hadrons ($h$) above 20 MeV:

$$ErrorRate_{LHC}(errors/s) = \sigma_{protons} \times Flux((h > 20\ \text{MeV})/\text{s})$$

A new column was thus added to the tables quantifying the radiation environments in the different sub-detectors of the LHC experiments: other than the TID (in rad) and the integrated 1-MeV neutron equivalent flux for Displacement Damage, the flux of all hadrons above 20 MeV appeared. While ATLAS added this requirement in the document formally describing their radiation qualification procedure [45], in CMS such document was not pre-existent and a more pragmatic approach was followed, in particular aimed at providing a set of guidelines for a quick qualification of components and systems that were about to be proclaimed production-ready. M.Huhtinen and the author of this paper were summoned in the last months of 1999 by the CMS electronics coordinator, G.Stefanini, to elaborate these guidelines and present them at a dedicated workshop for the electronics in HGCAL, in the muon chambers and in the experimental hall. We came up proposing a single test for all radiation effects based on an irradiation with $\geq$ 60 MeV protons. This concept presented a number of advantages:

- Mono-energetic proton facilities were relatively abundant;
- Protons of that energy are efficient in probing all radiation effects: TID, DD and SEEs. They thus enable a single qualification test;
- Proton beams can be enlarged to cover relatively large areas, making board-level qualification an option. This was a hard requirement given the advanced status of many developments, where a go/no-go test was needed;
- Other than SEUs, protons can also screen for other SEEs (albeit their efficiency in this task depends on their energy and is limited by statistics).

The approach was endorsed by CMS and, because of the addition of proton testing to the qualification procedures of all the experiments, a sudden need for proton beam time emerged. Here once more the contacts that the CERN Microelectronics group had established over time with the international radiation effects community turned out to be precious. We knew the colleagues responsible for the irradiation facilities at the Cyclotron Resources Centre (CRC, Louvain-la-Neuve, Belgium) and Paul Scherrer Institute (PSI, Villigen, Switzerland) from NSREC and RADECS conferences, and for having already performed tests at their facilities. On the basis of this long-standing relationship, and of the participation of both CRC and PSI to the CERN LHC program, we could organize together a facilitated access to the proton beam time at both facilities at preferential rates. Regular irradiation campaigns open to all colleagues from any Institute collaborating to the LHC experiments' construction and from the CERN accelerator groups took place under the coordination of the author of this paper (for the experiments) and T.Wijnands (for the LHC machine sector). Over a period of 5 years, 2000 to 2005, a total of 25 irradiation campaigns took place for about 750 h of beam time, with more than 30 European collaborating Institutes as beneficiaries. This provided an invaluable acceleration to the qualification program, that contributed to keep under control the schedule of the LHC systems.

#### 2.3.4. Protecting ASICs against SEEs

While the SEE tolerance of commercial-grade electronics components can be measured with the appropriate qualification procedure but cannot be modified by the user, ASICs functionality can be protected by a number of design techniques. As detailed in Section 2.2, HBD techniques have been used to upgrade the TID tolerance and meet the LHC requirements. These same techniques might also contribute to increase the resilience to some classes of SEEs, such as SEL (Single Event Latch-up). The systematic use of guard-rings, for instance, other than preventing TID-induced leakage paths is also beneficial against SEL. Radiation-induced latch-up might be provoked in any circuit location by the charge deposition from a single heavily ionizing particle. The current generated by this event is in fact injected in a thyristor structure inherent to the CMOS technology construction, turning it on to produce an almost short-circuit current between the supply voltage and ground. A guard-ring built as a continuous heavily doped band at the frontier between n- and p-wells (or substrate) ties the local potential firmly at the supply or ground voltage, turning off one of the two parasitic bipolar transistors of the thyristor. On the contrary, the use of the same HBD techniques might influence only marginally the sensitivity of the circuit to SEUs (ELT transistors have an increased minimum size with respect to standard layout FETs, and the corresponding increase of load capacitance of each digital gate contributes to lower the SEU sensitivity—at the expenses of larger power consumption). Other design techniques have therefore to be used to achieve the level of immunity required for LHC ASICs, and in particular for usage in the tracker detector systems. A wide variety of approaches has been used by our community of designers, based on either a modification of the memory/register cell, or on redundancy of the information (triplication, encoding). The modification of the cell ranged from simple increase of the size or load capacitance, as studied in [46], to the adoption of a specifically modified schematic for the memory/register cell, such as the Dual Interlock storage CEll (DICE) [47]. Triplication was often the favorite path: the limited density of designs in the quarter micron technology with ELTs and guard-rings made double hits, where the energy deposition from a single particle strike simultaneously alters the state of two cells of the triplet, very unlikely. Triplication was therefore a safe and relatively easy solution, since its addition was compatible with the design flow. For high-speed optical communication, data were often protected by encoding [48].

### 2.4. Conclusion with some hindsight

Looking back at the efforts deployed by our community to produce electronics systems – and most notably ASICs – capable of reliable functionality in the radiation environment of the first generation of LHC experiments, and with the benefit of 2 data-taking physics runs, what can we conclude? Overall, the physics program has been so far very successful and has not been hampered by evident problems traceable to radiation effects in the electronics composing the detector systems. Several issues that required modifications in the foreseen operational routine happened, such as the introduction of frequent resets to clear wrong registers or the modification of the operation temperature, but nothing ever escalated to the point where the problem was widely acknowledge to threaten regular data taking. With local patches at the system level, many problems likely remained confined within the sub-detector system where they occurred. ASICs in both the DMILL and IBM technology, as well as in other much more marginally used CMOS, BiCMOS or bipolar technologies, all contributed to the satisfactory functionality of the detectors, making them a marvelous instrument of discovery.

## 3. The LHC upgrade programs

No sooner had the LHC detectors started Run1 data taking that preparatory activities in view of detector upgrades were launched. Building on the success of the Foundry Service in the IBM 250 nm technology, the CERN microelectronics unit – now a section within the larger ESE group – started already in 2001 an exploratory study of the 130 nm CMOS technology node to evaluate its suitability for future ASIC designs. However, the upgrade target was a machine that eventually converged to what is today known as HL-LHC (High Luminosity LHC). In any configuration, this upgrade required radiation tolerance to a much higher level (10×) than what was painfully achieved for the Run1 experiments. While the 250 nm process was typically tested up to 10 Mrad, sometimes to 50 Mrad, the new generation of ASICs needed to resist to the unprecedented level of 100 Mrad, and even up to 1 Grad for

the inner pixel layers—in that case coupled to $10^{16}$ n/cm$^2$ (1 MeV equivalent). The following sub-sections will detail the work accomplished by the community in qualifying and supporting the CMOS technologies in the 130 and 65 nm nodes used today for HL-LHC ASICs—whose production is either on-going or about to be launched.

### 3.1. The 130 nm node

The 130 nm technology saw the introduction of the full copper metal stack for signal routing, and appeared as a strong node that would remain available for many years—promise that indeed was kept, since it is still easily accessible for prototyping and production 20 years after its introduction. In view of ensuring Foundry Services access to the HEP community, samples from 3 different suppliers were studied for TID effects [49]. The study took place on dedicated test structures including single transistors of different size, either custom designed or kindly provided by the manufacturer. This study clearly evidenced how the TID tolerance is determined, in standard non-ELT transistors, by processing details beyond the control – and understanding – of the user. As expected, the gate oxide thickness of about 2 nm proved for all samples to be subject to very limited radiation-induced defect build-up even to the ultra-high TID levels targeted for the application. The radiation tolerance appeared to be thus limited by the radiation response of the parasitic MOS structures: the edges of the transistors or their lateral isolation, both constructed via the deposition of $SiO_2$ layers – a fast process yielding an insulator rich in defects and hydrogen impurities. Contrary to the well-controlled process commonly used for the thermally grown gate oxide, which is necessarily very similar for all manufacturers, the details of the STI construction can widely vary across fabs, producing a wide variety of radiation responses. This appeared clearly in the evolution of the TID-induced source–drain leakage current in samples from the 3 different manufacturers shown in Fig. 10 [49]. Not only the increase of the leakage current during irradiation is very different, but also its evolution during post-irradiation annealing, that is determined by the properties (energy) of the holes-trapping defect centers in the STI.

From the data published in [49], two of the tested technologies appeared adequate for use in LHC upgrades and even gave reason to hope that the systematic use of ELTs could be avoided. The final choice was eventually driven by many criteria including ease of access, available design kits and libraries, and of course cost. A series of reports and papers were published in the following years to document the study of radiation effects on the electric characteristics of the transistors [50], on their noise [51,52] as well as reliability [53–56].

#### 3.1.1. HBD or standard design?

The detailed study of the TID effects in the chosen technology revealed very interesting features. Significant inter-transistors leakage currents were not detected in FOXFETs of different size and gate material, thus removing the need to guard-ring all the n-type diffusions [50]. Only for extremely sensitive low-current circuits the local use of p+ guards was recommended. Source–drain leakage currents in core n-channel transistors were instead observed to peak, at the dose rate and temperature used as standard in this type of studies, at an accumulated TID of 2–3 Mrad, before sharply decreasing when further dose was deposited in the devices [57]. This response is shown in Fig. 10 and has since been observed in many CMOS technologies. A detailed study of the trap properties using the isochronal annealing technique [58] led to the extraction of their characteristic activation energy that was used to forecast the evolution of the current in a low-dose rate environment [57,59]. This indicated that, at room temperature and at the dose rate foreseen for the experiments, no significant increase of the leakage current could be expected. On the basis of these results, rather than developing a dedicated digital library with ELT transistors similar to the one used years before in the quarter micron process, we took the decision to use the standard cell library already available in

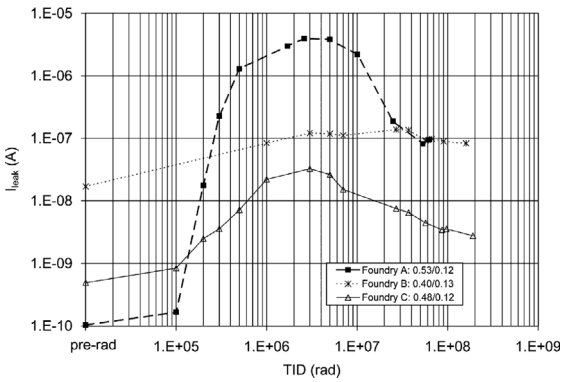


**Fig. 10.** TID-induced source–drain leakage current in NMOS transistors of three 130 nm CMOS technologies.
*Source:* From [49].

the technology. An already started effort to produce an HBD library was abandoned, and commercial-grade libraries procured and used for high-level digital design—while for full-custom analog and small and specialized digital blocks each design group chose its favorite approach. Unfortunately, the measuring equipment of the time prevented exploration at sub-zero °C temperatures, at which the de-trapping of holes is considerably slowed down. The attention devoted to this negative temperature range and to the very high dose rates in the innermost detectors was probably insufficient to warn the groups working on upgraded pixel detector systems of possible leakage current problems, which determined dire consequences years later (as described further on).

While in older technologies the effect of radiation-induced trapping in the STI (or birds' beak LOCOS) isolation was limited to the turn-on of leakage currents, the study of the 130 nm technology revealed for the first time that also the characteristics of the MOSFETs could be affected. The current flowing in narrow-channel transistors was indeed strongly influenced by the accumulation of radiation-induced charges in the STI surrounding the transistor's channel region. This effect, shown in Fig. 11 as a threshold voltage shift in NMOS transistors, was called Radiation-Induced Narrow Channel Effect (RINCE) [59] and it has since been regularly reported in many technologies. Contrary to the leakage current that only threatened NMOS transistors, PMOS transistors were also strongly affected by RINCE as also shown in Fig. 11 for the 130 nm technology. Similarly to the leakage currents, RINCE is linked to the evolution of trapped charges in the STI or in interface states at its borders with the Si; therefore it manifests differently with varying temperature and dose rate conditions. To avoid this effect in analog circuits, the guidelines distributed by the Foundry Service CERN team in the form of a complete document recommended avoiding NMOS and PMOS core transistors narrower than 0.8 and 0.4 μm respectively.

With hindsight, it is easy to observe how the transition from the 0.25 to the 0.13 μm generation was, radiation-wise, much more than a move to smaller feature sizes. In the quarter micron, designers were bound to use only ELT transistors, to systematically insert guard-rings, and to build their digital circuits with ELT-based standard cells from a minuscule library. The prize for this disciplined confinement to a limited design space was a radiation-tolerance insurance (at least up to the required 10–50 Mrad doses). The 130 nm brought back freedom to the designer, who could lay down transistors of (almost) any shape and size and use the wealth of digital cells in commercial libraries. However, the designer was now responsible for her/his choices, radiation effects in the circuit being determined by complex temperature and dose rate dependent effects—some of which strongly affected by transistor size. In summary, to make sound choices leading to reliable radiation tolerance all the engineers involved in the design and qualification of the ASICs needed at that point to have a solid understanding of the

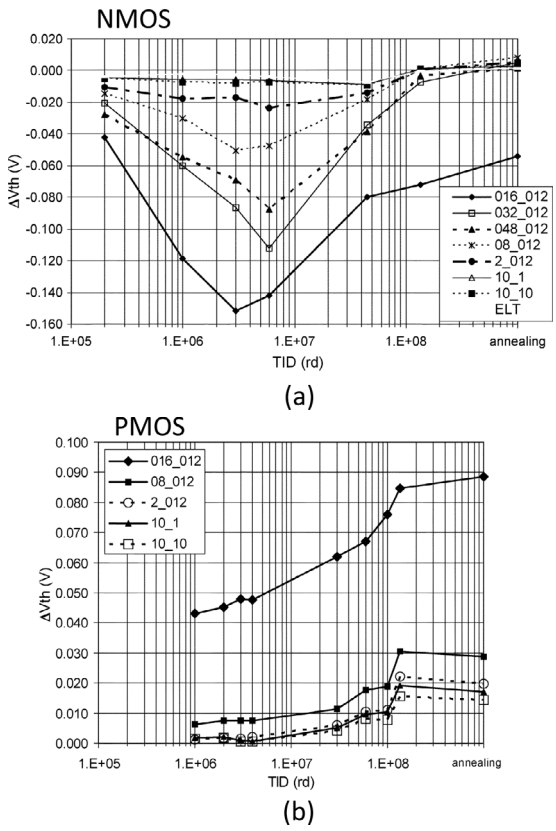


**Fig. 11.** Threshold voltage shift in NMOS (a) and PMOS (b) transistors of different gate width in the 130 nm technology. The aspect ratio W/L of the studied transistors in μm is shown in the insets. This was the first report of the RINCE.
*Source:* From [59].

radiation effects. This introduced a vulnerability in the development process, that originated some mishaps. One relevant example was the radiation-induced increase in the supply current observed in 2015 in the ATLAS pixel IBL (Insertable B-Layer), due to leakage current of transistors in the newly installed FE-I4 ASIC [60,61]. During its early operation in the ATLAS detector, the power consumption of the ASICs increased to the point that their supply had to be shut down for safety purposes. The task force diving into the problem soon understood that this was a consequence of the same source–drain leakage current increase in NMOS transistors reported 10 years earlier (Fig. 10). The low temperature (−10 °C) and high dose rate in the IBL environment contributed to worsen significantly the amplitude of the current peak with respect to the earlier transistor-level measurements. This problem was not detected during the qualification tests, during which the supply current was provided by an unlimited source – and not regularly monitored – and the chip was constantly functional. Once understood, the problem could be solved by an increase of the operating temperature to +5 °C which accelerated the evolution of the leakage current beyond the peak, and by the accumulation of dose during the operation. A large effort was devoted by the ATLAS collaboration to study the mechanism and even model it [62], a work that extended beyond the pixel detector system. The readout and control chips for the ATLAS ITK (Inner Tracker) upgrade foreseen in the Long Shutdown 3 (LS3) were in fact being developed in the same technology used for the FE-I4 chip, and designed with standard cell libraries and design techniques (no ELTs). The measurement of the current consumption of the available prototypes of the readout chip, the ABCstar, revealed the same type of supply current increase during accelerated tests at low temperature [63,64]. While the ASIC remained perfectly functional during exposure, the more than 2 times increase in supply current at the TID-induced peak challenges the capabilities of the power distribution system in the tracker, that cannot be increased without significant impact on the system layout. Although the readout and control ASICs were still in the prototype phase, a change in either technology (moving to another 130 nm CMOS technology whose TID performance was better) or design approach (introducing ELT transistors) was deemed incompatible with the available resources and schedule. Efforts were thus focused on dampening the peak, studying its precise characteristics in the projected environmental conditions, and even eliminating it by pre-irradiation of the samples before their deployment in the experiment. The latter approach can work only if exposure at room temperature without bias is efficient in producing interface states at the frontier between the STI oxide and the silicon substrate at the edge of the MOSFETs' channel. It is indeed the electrons trapped in the interface states that screen the channel from the holes trapped in the STI oxide and responsible for the leakage current. Since the activation of the interface states is based on hydrogen drift, a thermally-sensitive mechanism strongly influenced by bias, the efficiency of a pre-irradiation step at the wafer level (no bias) at room $T$ was far from being sure. Moreover, these interface states need to be stable (no annealing) during all operations on the pre-irradiated wafers preceding deployment in the experiment. Measurements revealed positive results, with the increase of the leakage current strongly reduced by a wafer-level exposure to 10 Mrad [64]. This pre-deployment irradiation at wafer level is thus part of the approved production sequence of the ATLAS ITK electronics, a $^{60}$Co source in Taiwan having been chosen for the exposure of the ≃ 800 wafers constituting the total production of ICs for the detector.

### 3.1.2. *Moving to a different supplier*

The semiconductor market changes rapidly, while the development cycle of a large High Energy Physics experiment typically lasts more than a decade. Manufacturers can suddenly change the access conditions to their technologies, or discontinue them with relative short notice. Our community is thus exposed to the risk of losing access to the CMOS technology used for an ASIC during its long prototyping phase, with dire consequences on the cost and schedule of the project. This might be alleviated by the prompt availability of an alternative technology for which the necessary design infrastructure has been developed. This infrastructure includes a fully characterized radiation behavior, established design kits and flows, as well as silicon proven general-purpose macro-blocks. This infrastructure was developed for the 130 nm process when CERN established a relationship with another large supplier in 2014. The initial radiation tests of this "backup" 130 nm process revealed an almost complete absence of TID-induced leakage currents, promising the elimination of concerns related to the detailed bias and temperature evolution of the current peak described above for the ATLAS pixel and ITK systems. This encouraged first the development of a full design infrastructure (kits and macro-blocks), then some HEP groups to adopt it for HL-LHC ASICs. Systematic measurements of a dedicated test structure repeated in every prototyping run indicated that the radiation response significantly changed in samples from different manufacturing sites (fabs), once more compelling the addition of a Standard Test Structure (STS) every time silicon is fabricated to constantly monitor the natural radiation tolerance of the process. This being influenced by details of the processing not disclosed to the customers and not necessarily kept identical in time, each lot could potentially have different radiation response—unless the radiation response is solely determined by the properties of the gate oxide itself, like in the case of ELTs in older technology nodes. The exploitation of the STS integrated in every run over time produced results of which examples are shown in Fig. 12. The leakage current peak appears systematically in transistors produced in one fab, but not in those from the other 2 fabs used for this technology. However, at large integrated TID doses, a non-negligible difference in the TID-induced transistor degradation is visible between different lots from the

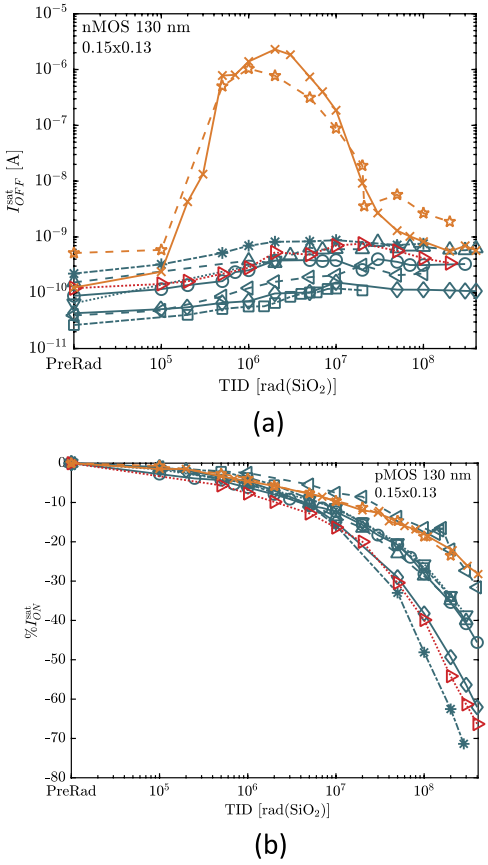


**Fig. 12.** Two examples of variability in the radiation response of 130 nm transistors. Different colors represent data from samples manufactured in different plants (Fabs), while different lines correspond to samples belonging to different production lots over a period of four years. (a) The TID-induced leakage current increases sharply in NMOS samples manufactured in one only of the three fabs. (b) The percentage decrease of the drive current with TID varies rather substantially in different production runs, also in the same fab, for minimum size PMOS transistors. Not shown, this variability as well as the absolute performance degradation get smaller for transistors with larger size (W).

same fab. This lot-to-lot variability in the radiation response becomes very visible only at very large levels of TID – unfortunately within the domain required for HL-LHC ASICs – and is probably associated to the natural dispersion of manufacturing parameters completely irrelevant for the pre-rad electrical characteristics.

The observed variability indicates that, in the absence of a systematic HBD approach eliminating the impact of the parasitic structures (STI oxides) on the active transistors, the natural radiation response of the technology has to be very regularly monitored for early detection of significant changes. Moreover, a comprehensive qualification procedure should be performed on a lot-by-lot basis for all ASICs.

With the results above, designers had a number of choices to produce reliably radiation-tolerant ASICs. Some chose to select for both prototyping and production the fab for which no significant increase of the leakage current was observed – this is an option authorized by the manufacturer – and abandon any dedicated HBD technique against leakage currents. This is equivalent to betting on the absence of processing modifications impacting charge trapping in the STI oxides during the whole prototyping and, more importantly, production cycle. It also assumes that the same fab remains available to manufacture all wafers necessary to equip the detectors, and hypothesis that is alas challenged in the current context of shortage in the semiconductor marketplace. So far this approach has led to ASICs successfully passing the radiation qualification tests, however most of them still need to be moved to production and surprises are still possible. Other designers

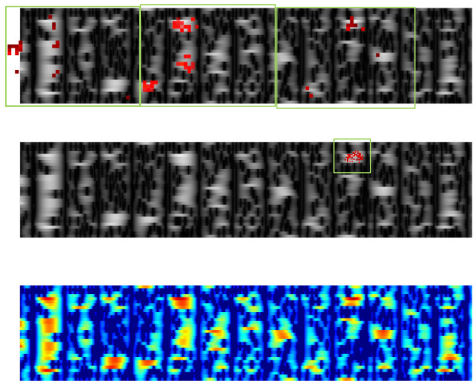

**Fig. 13.** Mapping of the SEL sensitive regions of a portion of the logic circuitry of the Velopix ASIC. In the two upper images the red dots represent locations where a single pulsed laser beam triggered SEL in the circuit. Only the areas highlighted in green to the left were scanned, with a much smaller step size for the lower image. The color image at the bottom is a color-coded representation of the resistance of every point of the circuit towards the substrate/well contacts. The correlation is clear: the point with highest resistance to the supply are those sensitive to triggering latch-up events.
*Source:* Courtesy of X. Llopart, CERN.

instead chose to continue using ELTs and guard-rings, relaxing the need for the selection of a specific fab and ensuring that the design is radiation tolerant even in the unlikely case of processing changes.

Some of the first ASICs designed in the 130 nm technology from the new supplier were also affected by an entirely different radiation-induced failure mechanism: Single Event Latch-up (SEL). These were circuits designed without HBD techniques, thus without the guard-rings that are very efficient in reducing the transient base-emitter voltage of the parasitic bipolar transistors involved in SEL. Both the VELOPIX (readout ASIC for the LHCb Vertex Locator detector) and the SAMPA (readout of the Alice TPC detector) were found to have a sensitivity to latch-up threatening their operation in the hadron-dominated LHC particle environment [65,66]. The detailed investigation of the problem, and in particular the mapping of the sensitive area with a pulsed laser shown in Fig. 13, evidenced how latch-up was only induced by charge deposition in regions of the circuit sufficiently far from substrate or well contacts. The resistance along the charge collection path in this area being excessive, the local base-emitter junction of a parasitic bipolar transistor was brought to forward bias after the strike and the latch-up mechanism was initiated.

It is interesting to note that in both designs the design rules imposed by the manufacturer on the maximum distance between substrate and/or well contacts were largely respected. It is also noteworthy that similarly laid-out designs in another 130 nm technology had not shown SEL sensitivity. It thus clearly appears that the maximum distance between these contacts for safe operation in a radiation environment is strongly technology dependent. Each technology has to be carefully characterized to find this parameter, and the safe distance has to be imposed during the design of every ASIC by adding a "custom" rule in the Design Rule Checker routines. This is precisely what was done in the case of the VELOPIX and SAMPA chps: the new prototypes that followed the modified design rules were successfully measured to be SEL-free.

### 3.2. The 65 nm node

During the first decade of the new millennium the development of ASICs for LHC upgrades was started in one of the selected 130 nm technologies, but the big upgrade program linked to the High-Luminosity LHC only kicked-off in the following decade. At that point, more advanced technologies were commercially available, opening the opportunity for better performance. Ambitious projects such as pixel

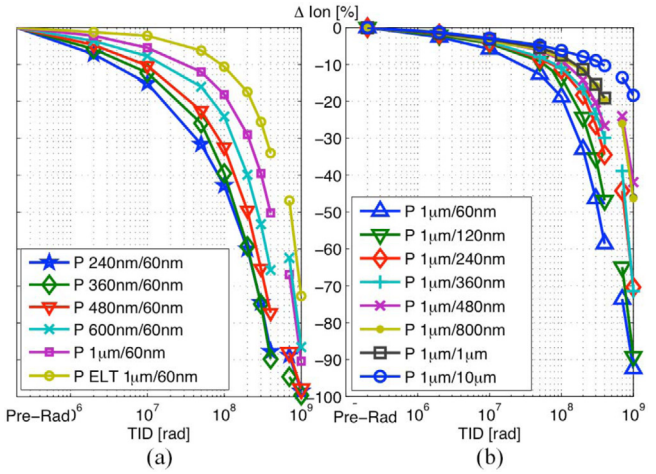


**Fig. 14.** Evidence of RINCE (a) and RISCE (b) in the TID-induced decrease of drive current of PMOS transistors in the 65 nm node. Narrower (a) and short (b) devices are increasingly affected.
*Source:* From [68].

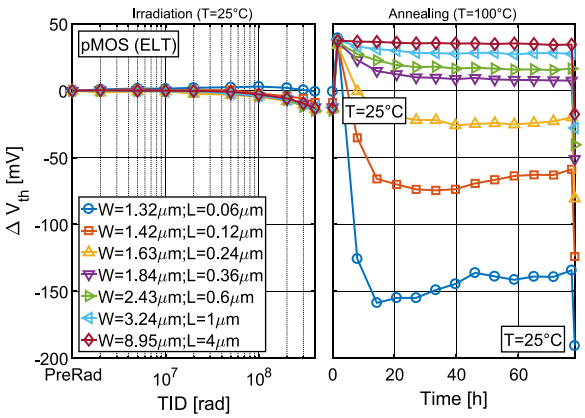


**Fig. 15.** Observation of the post-irradiation evolution of RISCE in PMOS transistors. During exposure to 400 Mrad very little threshold voltage shift is measured in devices of different size in the left portion of the graph. However, in the first few hours of the post-irradiation annealing at 100 °C the short-channel transistors exhibit a considerably and rapid shift.
*Source:* From [70].

detector systems and optical communication at 10 Gbit/s were in need for improved integration or speed with respect to what could be achieved with the 130 nm generation. The CERN EP/ESE group started an exploratory study of the 65 nm node, with the idea of including the technology from at least one supplier in the Foundry Services catalog of supported CMOS processes. Other groups joined the effort by measuring the radiation response of transistors in 65 nm samples from different manufacturers. The first radiation results on samples from the supplier that was eventually selected were very encouraging [67], suggesting that HBD was not required to meet multi-hundred-MRad tolerance. A contract for accessing the prototype and production lines of this manufacturer was stipulated. The 65 nm was made available to the HEP community via the CERN Foundry Service, and many groups started designs in this platform. With the increase of design activity, also testing opportunities multiplied and soon uncharted aspects of the radiation response of the technology emerged, that required several years of detailed study to be understood.

### *3.2.1. Complex radiation effects*

In addition to the narrow-channel effect (RINCE) discovered already in the 130 nm node, transistors in the 65 nm node showed also a very pronounced influence of the gate length on the radiation-induced degradation, that by analogy was called Radiation-Induced Short Channel Effect (RISCE) [68] (see Fig. 14). This was observable also on enclosed-layout transistors, thus excluding any contribution from mechanisms taking place in the STI oxide. This effect, together with a large set of interesting but largely unexplained observations, was presented at the 2015 NSREC [68]. Transistors appeared to be more severely damaged while both the gate and the drain terminals were biased, while up to that point the worst-case bias was typically determined only by the gate bias. Contrary to common wisdom in CMOS technologies, radiation-induced damage was milder at sub-0° C temperature. Also unexplained, transistors irradiated in asymmetric bias configurations became electrically asymmetric (source and drain could not be exchanged anymore without impact on the transfer and output characteristics). On the basis of all these observations, the 2015 paper concluded expressing concern – alas turning out to be well founded later – about possible true dose-rate effects.

Yet other surprising novel effects had to be discovered. On top of the list for originality, the post-irradiation evolution of the PMOS transistors serendipitously discovered by colleagues from the RD53 collaboration [69]. During high-temperature annealing, they observed that rather than the usual recovery of the performance, PMOSFETs actually showed a considerable additional degradation. This was later measured accurately in different conditions, as shown for example in Fig. 15. It took a good part of two years of work, with different measurement techniques performed on hundreds of transistors at CERN, University of Padova and Vanderbilt University, complemented with many discussions and much thinking, to shine light on most of the observed effects.

This work was presented at the NSREC conference in New Orleans in 2017, receiving the best paper award [70], and the damage mechanisms were further studied in [71]. The model explaining the main effects is schematically represented in Fig. 16. The paper concluded with a comment on the qualification procedure for circuits to be used in the cold ($\leq -10$ °C) LHC detectors, and specified these circuits should never be allowed to be warmed up under bias because thermal energy and voltage are at the basis of the damage mechanism. It concluded once again that low-dose rate measurements should be performed because the presence of Enhanced Low Dose Rate Sensitivity (ELDRS) was likely. This consideration was based on many similarities with radiation mechanisms typical of linear bipolar transistors, where the damage is due to radiation effects in poor quality oxides in the presence of a small electric field. RISCE and post-irradiation degradation in the 65 nm technology were in fact also traceable to radiation effects in the poor quality and low field insulators in the spacers (Fig. 16).

Studying enhanced low-dose rate effects on transistors that get significant damage only at multi-Mrad levels of TID is very complex and time consuming. It requires a radiation source where measurements can be performed over periods of many weeks, while keeping the devices under bias and regularly monitor their electrical characteristics. The setup should also offer the possibility to control the temperature to study its impact on the damage. For this reason, only a few reference measurements could be performed until, with the purchase of a second X-ray irradiation machine at CERN EP/ESE, a more systematic study at different temperatures could be done. After an early work published at RADECS 2017 [72], a complete summary and interpretation of the results was presented at the NSREC conference in 2020 and was recognized with the meritorious paper award [73]. As anticipated, short-channel transistors in the technology do exhibit a pronounced ELDRS, which considerably complicates the qualification procedure for ASICs (an example for PMOS transistors is shown in Fig. 17). One of the approaches followed for the qualification of bipolar technologies is based on high-temperature irradiation. This unfortunately cannot be applied in the 65 nm CMOS technology, since as shown in Fig. 16 the simultaneous presence of high temperature and voltage activates

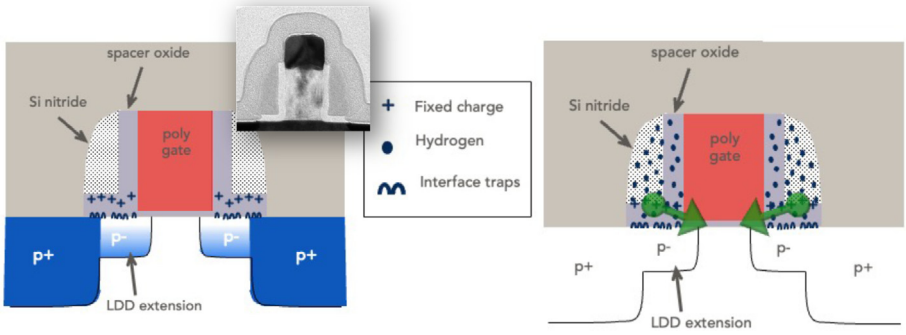


**Fig. 16.** Physical model explaining the complex evolution of defects in irradiated and annealed 65 nm transistors. During irradiation, charge trapped in the spacer oxide and at its interface with the LDD region underneath it influences the superficial effective doping (left). In PMOS transistors, both charge in the oxide and interface states is positive and generates and electric field reducing the effective p-doping of the LDD. This provokes an increase of the series resistance. TID exposure also frees hydrogen ($H^+$) in the spacer insulators (right). The drift of hydrogen is a thermally activated and electric-field driven process. During post-irradiation high-T annealing under bias, $H^+$ can drift to the gate oxide and de-passivate dangling bonds, giving origin to active interface states (the drift is represented by the green arrows in the right image). The small TEM inset shows the size of the spacer insulators in a real 65 nm transistor.

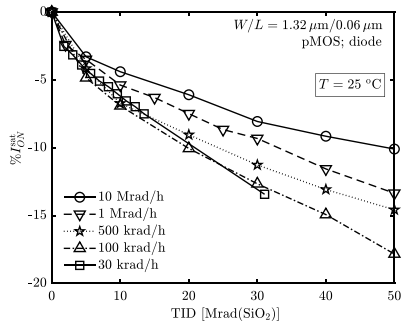


**Fig. 17.** Evidence of the Low-Dose-Rate effect in 65 nm PMOS transistors of short gate length biased in the diode configuration during exposure. The radiation-induced degradation in the on-current is considerably larger when the dose rate is decreased. *Source:* From [72].

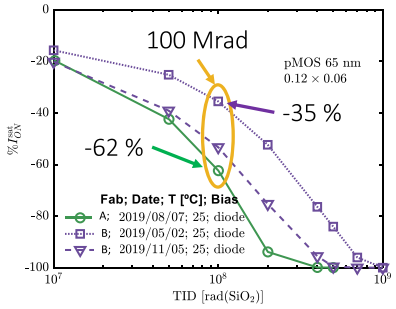


**Fig. 18.** Variability in the TID degradation of minimum size PMOS transistors in the 65 nm technology. At 100 Mrad, the decrease of the on-current can vary of almost 2x between different lots. Note that the statistical meaning is small, with only three lots tested in 2019.

a damage mechanism that is frozen at sub-0°C temperatures. The only viable solution is over-testing (reaching larger TID levels at High Dose Rate) or, whenever practical, perform much longer tests at a lower dose rates. The complexity of the qualification strategy is witnessed by the considerable effort invested by the RD53 community working on the development of the readout ASIC for the HL-LHC ATLAS and CMS pixel detectors [74]. In this case, the approach to meet the unique requirement of TID tolerance up to 1 Grad included also the choice of the most appropriate digital standard cell library amongst the large number distributed by the foundry. Radiation effects being strongly dependent on the transistors' size, libraries using devices with larger-than-minimum size lead to better tolerance. A compromise between area occupation, power consumption and radiation resilience was found by the RD53 collaboration and adopted for the ASIC design.

It should be mentioned that most of the above described effects have been in fact observed in samples from 65 nm technologies from different manufacturers [75]. It thus appears that they are a rule rather than an exception in this node. For what concerns the ELDRS, a limited set of measurements on 130 nm samples from the same manufacturer also revealed the presence of ELDRS—although of considerably smaller magnitude [72].

A final note on the 65 nm technology concerns its measured lot-to-lot variability in the TID-induced degradation, that has been monitored on the same test structure systematically included in all prototyping runs. As shown in Fig. 18, the variability at high doses is unsurprisingly comparable to the one reported earlier for the 130 nm, although the dataset is for the time being more limited. This type of variability has thus to be expected for any technology, and maybe to be even larger for technologies with smaller production volume.

### 3.3. SEE protection in 130 and 65 nm technologies

One of the consequences of the down-scaling from the 250 nm technology used for the first generation of LHC experiments to the 130 and 65 nm processes for the upgrades is a decrease in the charge necessary to induce SEUs in digital circuits. The threshold charge for SEU is in fact proportional to the node capacitance and to the supply voltage, and both followed this reduction in feature size. Because of the smaller SEU threshold, the error rate of standard cells in the LHC type of radiation environment increases, and the use of techniques to protect the digital content is unavoidable. The sensitivity of standard register or memory cells has been measured using dedicated test structures, and most often with the help of heavy ion beams as shown in Fig. 19 [67].

In some cases, different architectures for the same cells have been designed and compared [76]. These SEU-hardened cells evidenced that architecture alone was not sufficient to achieve the desired resilience, since it typically relies on duplication of the information on two different nodes. Because of the miniaturization, a single cell gets sufficiently small in these technologies for all its nodes to collect some charge from a single particle hit, making the duplication inefficient. This is highlighted by the increase of Multiple-Bit-Upsets (MBUs) in SRAM cells at moderate-high LET in Fig. 19(b). Nodes from different cells should thus be interleaved, which can be done by building macro-cells with multiple memory cells whose nodes are scrambled. In the case of heavy ions the distance separating every node of the duplicated pair should always be larger than the charge collection area from a single hit, which is a technology dependent parameter. In a hadron-dominated environment the fragments are emitted isotropically, thus the separation depends on the range of the fragments with sufficient

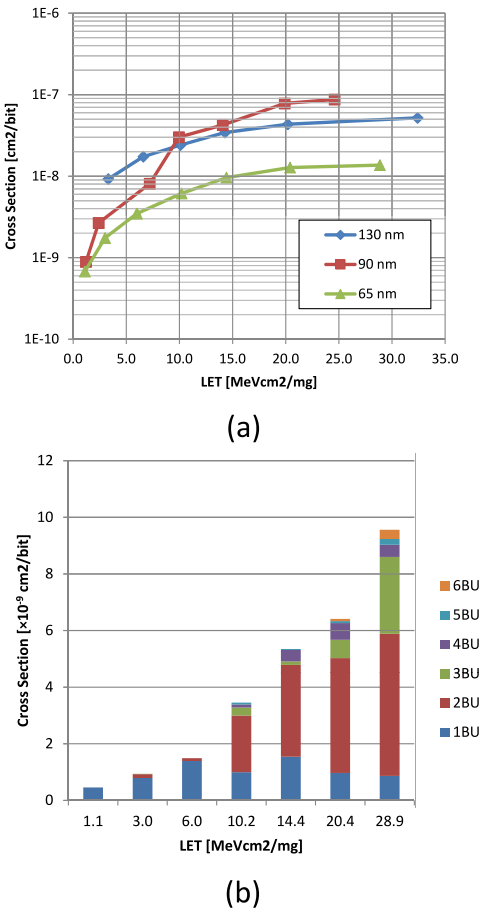


**Fig. 19.** Images of the SEU sensitivity of register and memory cells in the 65 nm technology. In (a), the cross-section during heavy ion irradiation for D-FF cells is compared for 130, 90 and 65 nm designs. While the saturation cross-section decreases in 65 nm because of the smaller area of the cells, the threshold LET seems to also decrease—although higher data granularity would be needed at very low LET to confirm it. In (b) the increasing occurrence of Multiple Bit Upsets (MBU) in 65 nm SRAMs clearly appears in particular at large LET of the ions. Events where up to 6 bits were upset (6BU) were observed.
*Source:* From [67].

LET to induce an error. These separation conditions are very difficult to put in practice, also because they impose severe constraints to the automatic Place and Route (*P&R*) digital design flows. For this reason, the SEU hardening approach by far most commonly used is the full triplication of the sensitive circuit portions (control, clock and reset signals) while the data path, where errors can be easily tolerated, is often left unprotected. The triplication needs to protect from both SEUs and SETs and should include the appropriate voters to eliminate errors from any of the triplicated paths and feedback a correction. In order to facilitate the addition of triplication paths to a generic digital design, a task that manually done can easily be error-prone, a tool has been developed at CERN by S.Kulis [77]. The Triple Modular Redundancy Generator (TMRG) is a toolset intended to assist the designer in the triplication process, also providing routines to simplify the implementation and verification processes. This open source tool has been widely employed by designers in the HEP community, with support provided by CERN-EP-ESE for its correct use. In a few cases where full triplication was not compatible with the density or power budgets, and where protection against SETs was needed, a protection concept based on time redundancy has been used. This was the case for instance of the ASICs developed by the RD53 collaboration for the HL-LHC ATLAS and CMS pixel detector systems. This approach relies on the finite and short duration of a transient propagating along a combinatorial logic chain. The sequential logic latching the signal from the chain samples its input three times, at a fixed time distance longer than the maximum duration of the SET. The three samples are then voted, filtering out the SET that has been sampled only once. Although in principle attractive, since it allows to avoid triplicating the full combinatorial chain, this approach is difficult to implement in practice when designing using automatic EDA tools. It introduces time constraints that make timing closure very difficult in the design flow.

During the design of the complex logic circuitry embedded in frond-end and control ASICs, it is of paramount importance to verify that the design satisfies all functional specifications and that it does not contain errors, even those that could only manifest in very specific conditions and that could thus possibly even escape detection during the physical testing phase. Design verification has recently gained popularity in HEP, and attention has been devoted to the verification of the designs' reliability to injected faults—events that in the field are produced by SEU and SET. This is a domain that is still in its infancy in our community, but expert verification engineers at CERN are actively working on the subject, with an eye on the industry-grade methodologies developed for similar problematics. The future will no doubt bring the elaboration of a recommended approach and the introduction of tools facilitating its adoption.

## 4. Radiation effects in power distribution ASICs

This short chapter evidences how the use of high-voltage rated technologies for the development of ASICs for LHC upgrades introduces new classes of radiation effects that are generally not apparent in the low-voltage technologies that have been described in this paper so far. In this context, high-voltage means 10 to 48 V, which requires the use of specific implants for isolation of devices and power domains as well as lateral or vertical MOS transistors.

### 4.1. High-voltage technologies and LDMOS

The front-end electronics of the first generation of LHC tracking detectors is powered without local on-detector voltage conversion and often regulation. This scheme is incompatible with the power requirements of upgraded HL-LHC trackers, where ASICs are powered at lower voltage and need higher current to be fed via massive power cables. In order to reduce this current, the most conventional solution is to distribute power at higher voltage and perform a local conversion and regulation with DC-DC converters [78]. However, this places the converters in the radiation and magnetic fields of the trackers, a very challenging environment for components using high-voltage technologies and ferromagnetic inductors. An R&D activity to develop specific radiation and magnetic field tolerant DC-DCs started at CERN in 2007. Since ferromagnetic cores saturate in the 40'000 Gauss field of the trackers, air-core inductors were the obvious choice [79]. Space and material budget specifications dictated the need for a DC-DC converter ASICs where both the control and power circuitry are integrated in the same silicon die, with an input voltage capability of at least 10–12 V. This voltage rating forces the use of technologies offering compatible transistors and wells. These technologies are normally built as extensions of existing low-voltage platform with the addition of an high-voltage module using vertical or, more commonly Laterally Diffused MOS transistors (LDMOS). These transistors have important differences with respect to the low-voltage MOSFETs, and in particular they use a lightly doped drift region to decrease the source–drain electric field. Alas, this makes the LDMOS sensitive to Displacement Damage (DD) effects, a mechanism that is instead generally negligible for the conventional MOSFETs. An example evidence of this sensitivity is shown in Fig. 20 [80]. The on-resistance of N-channel LDMOS transistors in different technologies increases very rapidly with the integrated proton flux after a technology-dependent level. A very remarkable feature of the DD sensitivity of the studied LDMOS transistors is that

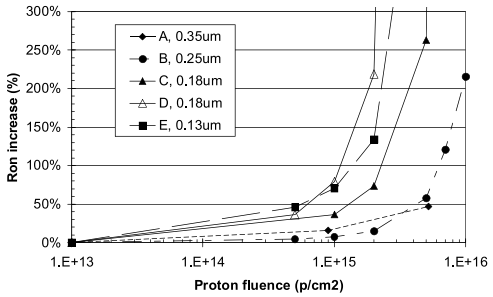


**Fig. 20.** Increase of the on-resistance of N-channel LDMOS transistors with proton fluence. Sample transistors were manufactured in 5 different technologies with a high-voltage module added to a core low-voltage process of minimum feature size indicated in the inset. The increase is very sharp after a threshold fluence that varies by an order of magnitude between the studied technologies.
*Source:* From [80].

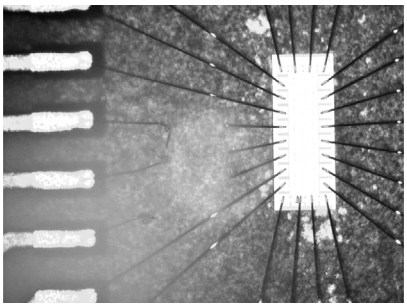

**Fig. 21.** Image of a test chip containing N-channel LDMOS transistors after exposure to Heavy Ions. The large drain–source current of SEB events provoked the melting of the aluminum bonding wires connecting the drain pad of the chip with the Dual-in-Line ceramic package.

protons and neutrons appear to introduce a degree of damage that does not follow the Non-Ionizing Energy Loss (NIEL) scaling normally used for the leakage current of silicon detectors [81]. This observation has not yet been published and measurements are still on-going.

The physical layout of the LDMOS cannot be modified safely, any modification possibly determining an impact on the distribution of the electric field and compromising the long-term reliability of the transistor. The same HBD technique based on Enclosed Layout Transistors (ELT) so successfully used in low-voltage technologies is thus not applicable. Initial experiments where ELT LDMOS were designed in one candidate technology showed, for instance, that the transistors behaved normally and did not show source–drain leakage current after TID exposure, but failed at low $V_{ds}$ after proton exposure - a mechanism not observed at all in LDMOS with standard layout. Without ELTs, circuits have to be designed tolerant to the radiation-induced source–drain leakage currents that naturally come with standard layouts - a radiation response that depends on the processing details and that can have lot-to-lot variability.

Several commercially available technologies with high-voltage extension were fully characterized, initially only for TID and DD effects [80]. An experimental work by P. Dodd and co-workers published in 2009 showed for the first time the evidence of Single Event Burnout (SEB) susceptibility in LDMOS transistors at an applied $V_{ds}$ below 10 V [82], triggering an urgent study on transistors in the technology that had been pre-selected on the basis of electrical, TID and DD performance. This revealed that the N-channel LDMOS transistors were sensitive to burn-out induced by heavy ions of LET of 10 $\mathrm{MeV{\times}cm^2mg^{-1}}$ at $V_{ds}$ smaller than 8 V. This indicates a likely occurrence of SEB for a converter with input voltage of 12 V in the LHC hadron environment. Modifications in the structure introduced by the manufacturer did not lead to considerable improvements, thus this technology was abandoned in favor of an alternative with inferior electrical performance but insensitive to SEB. Obvious consequences of the burn-out in some of the tested LDMOS are shown in Fig. 21.

### *4.2. A noticeable example of TID-induced failure*

One of the first deployment of the DC-DC converters ASICs eventually developed at CERN in the framework of the R&D effort mentioned in the previous subsection was in the CMS pixel detector system. About 1200 converter modules, whose core was the FEAST2.1 ASIC, were installed to power the front-end modules for the physics run of 2017. After a few months of smooth operation, some failures were observed once the luminosity of the accelerator was increased. In the following two months, about 5% of the installed converters failed. A systematic characterization of all the 1200 samples during the subsequent winter shutdown, that was extended to enable the replacement of all the modules, revealed that 35% of the converters had signs of damage.

A large series of experiments was conducted in the following months to uncover the origin of the failures, but this was complicated by the large number of unique features of the CMS pixel system (radiation background, operation temperature, magnetic field, proximity to the LHC beam line, grounding and shielding details) and by the difficulty in reproducing the same damage outside it. The turning point of the investigation was a dedicated test at the CERN IRRAD facility, when it was possible to expose 32 converters to a mixed field of radiation in proximity of the proton beam of the Protons Synchrotron (PS) accelerator at −25° C. The results of this experiment clearly indicated a strong correlation between the radiation background, the ambient temperature, and the failures, as well as the functional sequence necessary for the damage to happen. Using this same functional sequence during X-ray irradiation, while simultaneously observing the evolution of some of the circuit's nodes, it was possible to understand the failure mechanism.

As earlier pointed out, LDMOS transistors cannot be laid out as ELTs and circuits have to be designed to be compatible with the TID-induced source–drain leakage current in the N-channel LDMOS. One of the techniques to achieve this result is to add ELT core transistors in series to the LDMOS. This necessitates that the ELTs are always turned off when the LDMOS leakage has to be prevented. It is important to point out that there is no automatic tool helping the designer verifying that this is the case for every LDMOS and for every possible sequence of signals. In the case of FEAST2.1, one such vulnerability was not identified during the design phase: an N-channel LDMOS transistors in the circuit regulating an internally-created 3.3 V voltage supply rail was "unprotected" when the converter was held in the reset condition. When exposed to TID, the leakage current of the LDMOS was mirrored (and amplified by a factor of 500) and was integrated on the capacitance loading the 3.3 V supply, making it rise up to 8 V - beyond the breakdown voltage of the devices connected to the supply. This was only occurring during the reset of the circuit, in the TID range of 1–2 Mrad and at low temperature, when the leakage current peaks in the LDMOS transistors of the technology. Because of the simultaneous need of all these conditions, the vulnerability was not found during the qualification of FEAST2.1. Once understood, after more than 6 months of intense research, the problem was very easy to avoid even by a simple addition of an off-chip resistance.

This example TID-induced failure in the field, documented in a detailed report [83], demonstrates how even circuits that have been custom developed for radiation tolerance and extensively qualified can, in some unfortunate cases, still contain vulnerabilities that can generate dire consequences. In this case, the leakage current in a single transistor risked to compromise the successful data taking of the pixel detector and, therefore, of the whole of CMS.

## 5. Conclusion

As summarized in this article, in the last 30 years the HEP community struggled to develop, produce and deploy ASICs capable of reliable functionality in the extreme radiation environment of the LHC and – a fortiori – HL-LHC environment. During this lapse of time we moved from the military-grade radiation hard 1.2 - 0.8 μm CMOS and biCMOS technologies of the 80s to the 65 nm CMOS used today. In between we had to learn design techniques to make circuits robust against TID and SEE alike, as well as to develop and acquire methodologies and tools to efficiently study radiation effects and confidently qualify ASICs. This effort led to successful data taking during the first 2 LHC physics runs that used essentially the ASICs produced at the end of the 90s and at the beginning the new century, with some upgrade. The same electronic components are still used for physics run 3 that is now running and that will lead to the Long Shut-down 3 (LS3) scheduled in 2026–28, during which a major upgrade of the accelerator and detectors is foreseen. The new generation of ASICs in 130 and 65 nm upgrading the detector systems are still being developed and produced and will have to function in a much more challenging radiation environment (exceeding 1 Grad and $1 \times 10^{16}$ n/cm$^2$). Time will tell if these will be as successful as their forebears. Meanwhile the community is looking beyond LS3, starting to develop technologies and tools for ASICs useful for further detector upgrades, or for new high energy physics endeavours. A CERN-EP R&D effort has been launched including the qualification of a more advanced CMOS technology and prepare the infrastructure for complex System-On-Chip ASIC design leveraging on its high-performance and low-power capabilities [84]. A survey of the accessible options led to the exclusion of SOI technologies whose radiation response at ultra-high TID levels is strongly complicated by the presence of a still relatively thick buried oxide. FinFET technologies replacing the conventional bulk planar CMOS as from the 16 nm node have also not been considered the best fit for the next generation of HEP instrumentation for reasons of accessibility, cost and complexity. The best option appears to be the bulk 28 nm node, that is foreseen to remain available for a long time and that is widely accessible from several manufacturers. In the high voltage arena, Gallium Nitride (GaN) is emerging as an innovative technology bringing a revolution in the power distribution field. Initial results of its radiation tolerance are extremely promising, and an hybrid point-of-load step-down converter rated to 48 V input voltage and 10 A output current is already being brought to production readiness in the framework of the CERN-EP R&D activity [84].

To conclude this story of the last 30 years, it is useful to highlight the importance of the exchanges that our HEP community had with the radiation effects community at large, and fostered by the IEEE NPS Society and the RADECs association. As pointed out by many examples in this paper, only by being exposed to the expertise and original ideas of that community we could overcome the many original challenges we were confronted with. These exchanges should certainly be nurtured to enable maintaining in the HEP instrumentation world a critical mass of scientists with expertise in the field. Although a cursory analysis of recent data might give the impression that radiation effects could be almost neglected in modern technologies, we should not make the mistake of underestimating their complexity—which as devil lies in the details. As some examples in this article witness, overlooking this complexity has often brought misery that could have been avoided. Easily achievable ASIC reliable survival in the radiation environment produced by the HEP high luminosity proton colliders will continue to be a tantalizing idea.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgments

The story told in this article has too many protagonists for individual citation in a short section, but the author wishes to express his gratitude to all the colleagues who have significantly contributed to the work described here. It was an extremely pleasant and enriching experience to collaborate with so many talented and enthusiastic scientists, from many different Institutes and Countries. They achieved the amazing results exposed in this paper, or helped the accumulation of experience and knowledge that made them possible.

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