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Front-end electronics for silicon strip trackers: Architectures and evolution

Jan Kaplon

CERN, 1211 Geneva 23, Switzerland

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ABSTRACT

Tracking detectors based on segmented semiconductor sensors have been present in high-energy physics experiments for more than 40 years. The development of these sensors was always strongly linked to advances in CMOS technologies that offer features supporting the design of specialized ASICs for readout purposes. While in the beginning, the front-end electronics only provided simple signal reception and amplification, sending out the raw analog data, growing demands from the experiments lead designers to begin directly integrating more advanced features for data processing and storage, power management, calibration functions, amongst others, on-chip. This development was, and continues to be, possible due to CMOS technology evolution, in particular the scaling. Besides higher speed and better transconductance, today's sub-micron processes offer intrinsic ionizing radiation tolerance which, together with Single Event Effect (SEE) hardening techniques, allows design for reliable operation in a harsh radiation environment. Despite the enhanced functionality and greater number of transistors, higher time resolution and, in consequence, faster analog shaping and readout speed, the power consumption of typical front-end electronics measured per area of tracking detector remains of the order of a few tens of mW per square centimeter. The basic architecture of the input stage has also remained practically the same over the last 40 years. The optimal solution providing wide bandwidth and high open-loop gain at minimum power is the cascode: a cascade of common-source and common-gate amplifiers. Although each particular implementation differs slightly depending on the specific requirements and process used, the core of the preamplifier remains the same since its conception.

1. Introduction

This article reviews low-power front-end electronics designed for silicon strip tracking detectors built for high-energy physics experiments over the past three decades. The paper focuses on the architecture and evolution of the front-end input stages. As these are responsible for efficient interfacing with the sensor, they form the core of the front-end amplifier and ultimately determine the noise performance of the system.

For better readability, all formal analyses are presented in the appendices. As the key design parameters, the impact the open-loop gain, and the Gain Bandwidth Product (GBP) have on the performance of the input stages is studied in depth. This results in clear answers concerning the optimal architectures to be used along with strategies to improve the power supply rejection ratio (PSRR). Noise analysis provides guidelines to optimize the power consumption and timing response, as these are the primary requirements driving a tracker's front-end electronics. The outcomes are discussed in detail in Sections 3 and 4. The impact of CMOS technology scaling on the architectures of front-ends and the discussion regarding the use of bipolar processes as alternatives for scaled CMOS technologies are presented in Section 4. Sections 5, 6, and 7 give an overview of the input stage evolution on the examples of the circuits designed for three generations of the colliding machines. This development is shown in the context of more and more demanding requirements concerning time resolution and radiation hardness. Together with advances in CMOS technologies mainly linked to the scaling, improvements in terms of speed as well as better tolerance to ionizing radiation become accessible. Section 8 briefly discusses the problem of the detector leakage current. Section 9 gives an overview of progress in the evolution of readout architectures. Although this paper is focused on the front-end preamplifier stages, other on-chip functionality plays a fundamental role in the practicalities of multichannel front-end electronics in large-scale tracking systems, having an impact on the power consumption both at the ASIC and the detector system levels. The summary and prospects for the future can be found in Section 10.

2. Historical background

Tracking detectors based on segmented semiconductor sensors have been present in high energy physics (HEP) experiments for more than

E-mail address: jan.kaplon@cern.ch.

[1] The spatial resolution can be greatly improved in sensors optimized for charge sharing, where the analog information about the relative magnitudes of the charge signal measured in adjacent strips can be used [1].

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40 years [2]. Given that these trackers must provide the detection of relativistic particles with minimum scattering, a low-density material like silicon is an ideal candidate for the sensors to be used in such an application. In addition, the use of planar monolithic technologies, developed originally by the microelectronics industry, provided a reliable technology for both the prototyping work and for the construction of charged particle trackers for HEP experiments since the beginning [3]. Standard photolithography techniques, allowing for high resolution sensor segmentation, offer spatial resolutions of the order of ∼1 μm [4], determined by the pitch of the patterned strips.[1] In the past, the most common arrangement was for the diodes to be implanted on the silicon wafer in the form of strips, allowing for very short interconnections with the front-end electronics assembled next to the sensor using standard wire bonding methods. Consequently, the parasitic capacitance seen by the front-end input was minimized, optimizing the noise and charge collection efficiency — the two main components constraining the physics performance of the trackers. Despite many advantages, this scheme suffers from the drawback that the signal read out by the front-end connected at the end of the strips only provides one-dimensional information about the track position. This problem is overcome by combining information from another sensing layer with the strips tilted (stereo detectors) or perpendicular to the strips of the first layer. Even so, this can still lead to ambiguities for the track recognition at high multiplicities, especially for jet events. Therefore the length of the strip sensor is usually constrained by the probability of such events occurring in a given application. This depends on the particle flux after the collision at the sensor location in the experiment, which depends on the accelerator luminosity, the distance from, and how forward the sensor is, relative to the interaction point. Past and present detector modules exist with the strip length ranging from a few centimeters (e.g. 2.4 cm ATLAS ITK [5]) to tens of centimeters (e.g. 27 cm CDF SVX [6]). Although progress in interconnection techniques allows for two-dimensional pixel sensors bump bonded to the front-end electronics to be built, and the recent advancements in the development of monolithic active CMOS pixels offer sensor layers combined with the readout electronics on the same silicon wafer, silicon strip detectors are still an essential part of the presently developed trackers. Due to this well-established technology, relatively inexpensive manufacturing costs and assembly techniques, new trackers planned for HEP experiments under development are reaching hundreds of square meters of silicon, comprising several tens of millions of readout channels providing the required performance, whilst conforming to both the power and material budgets. For a fair comparison of power consumption between strip and pixel detectors, equivalent systems working in the same experiments should be considered i.e. having the same number of tracks per event, and take into account all service electronics necessary to transfer the data outside the detector. Taking the ATLAS detector at LHC as an example, we have to compare the 2 m^2 of pixels dissipating 15 kW of power with the 60 m^2 of SCT with the power consumption of 23 kW. Pixels are located closer to the interaction point in order to work with much higher hit occupancy per area. For efficient track recognition in the experiment, both detector systems are essential and thus these detectors contribute to this task in a complementary way.

As already mentioned, the power consumption of the front-end electronics measured per area of tracking detector is of the order of a few tens of mW per square centimeter of the detector surface, depending mainly on the speed of the front-end electronics and amount of data to be processed. For slow front-end electronics designed for early, relatively small scale trackers built at the LEP machine where the readout architecture was rather simple, the power dissipated by the first stage required mainly for noise optimization, was up to 90% of the overall power consumed by the ASIC. Typically, for the case of fast electronics designed for LHC the power dissipated in the input stage is between 30 and 40% of the overall power consumed by the front-end chip. The rest is spent in the readout part and various analog signal processing blocks which have to cope with high data rates, thus dissipating non-negligible amounts of power. Given that the noise specification, which from the point of view of the efficiency versus noise occupancy figure, does not vary from tracker to tracker (see analysis in footnote 2), and the fact that in general the power which is needed to keep it within specified limits is proportional to the speed of the front-end (non-linear function, see the noise analysis in the Appendix) it is not a surprise that power per surface area for the new trackers is higher than in the past. This increase is moderated by use of modern technologies allowing for better noise optimization due to the higher transconductance parameter, providing higher speed at lower inversion order (i.e. power) and operating with lower supply voltage. Silicon strip trackers have power densities (overall power including services) in the range of 10–40 mW/cm^2 depending if they are slow (LEP) or fast (LHC or High Luminosity LHC).

3. Driving issues for front-end electronics design

Despite the many advantages of silicon, the charge generated by a relativistic particle traversing the typical 300 μm thick sensor is of the order of 3.5 fC (see [7]), and in radiation sensor applications cannot generally be used directly without some form of amplification. The signal induced by the drift of the generated electron–hole pairs inside the sensor volume is sufficiently fast for tracking applications and, for a fully depleted sensor, is in the range of a few nanoseconds. The front-end amplifier connected to the excited strip must provide efficient transfer of this charge in the presence of the strip-to-strip fringing capacitances, with minimum noise and cross-talk to the neighboring channels. The fundamental readout configuration, resolving the problem of signal cross-talk and providing good efficiency of the signal collection is the charge sensitive amplifier (CSA). This is a high open-loop gain amplifier with shunt-shunt feedback consisting of an integrating capacitor and either an active or passive discharge circuit to avoid saturation of this stage in the signal processing chain.

Increasing the open-loop gain and the Gain Bandwidth Product allows for lowering the feedback capacitance and for increasing the charge gain, whilst at the same time, keeping low input impedance to preserve good charge collection efficiency and low cross-talk (see [8]).

Boosting the charge gain (the closed-loop gain of the CSA) is important from the standpoint of the noise-power optimization of the front-end chain as it allows for minimization of the power spent in the following stages of the front-end, whilst keeping the noise performance, preferably being determined by the input amplifier only, at the required level. For tracking applications, a comfortable signal-to-noise ratio providing both good efficiency of track finding and low noise hit rate should be around 14.[2] Therefore, for a minimum ionizing particle (MIP) signal from a non-irradiated 300 μm sensor equal to 3.5 fQ, the equivalent noise charge (ENC) should be lower than 1600 e^- rms.

[2] Let us assume that front-end output noise follows the Gaussian distribution (clean system with only pure noise sources and no EMI interference). In order to provide good tracking efficiency (defined as the detection of all particle hits) and low noise hit rate in a multichannel tracker system (sometimes several millions of channels) it would be sufficient to provide signal to noise ratio of 5. In this case the probability of the acceptance of the noise hit as a valid signal will be below 2.9 $\times 10^{-7}$ and the tracker system can be considered as noise free. When considering the practical implementations of the front-end amplifier connected to the silicon strip sensor, two additional effects have to be taken into account. First is the possible charge sharing in between two neighboring strips which in the worst case can reduce the signal seen by a single front-end amplifier to half of the total. The second effect is related to the energy loss distribution function of the particle traversing the sensor medium responsible for the signal creation. The exact value of the generated signal is the result of a stochastic process and follows the Landau distribution where the minimum signal (defined here as a signal generated with the probability at the level of 10^{-6}) to most probable signal ratio for a typical 300 μm sensor is around 0.7 (see [9]). All effects combined together set the required signal-to-noise ratio for MIP particle (defined as a most probable

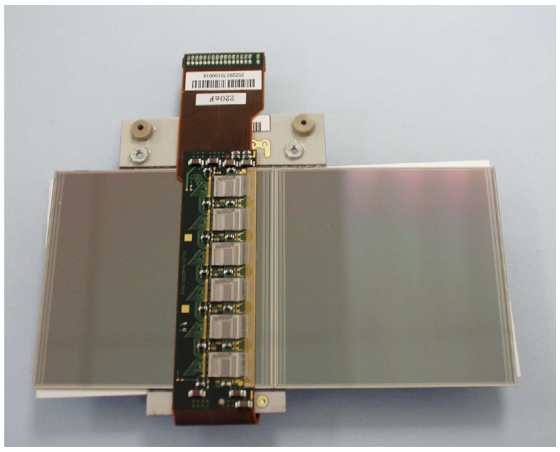

Fig. 1. Double sided, stereo angle, barrel silicon strip detector module of the ATLAS SCT. The strips (length 13 cm; two, 6.5 cm, detectors daisy chained) are readout by 12 128-channel front-end ASICs. The compressed binary data is send outside the module via optical links.

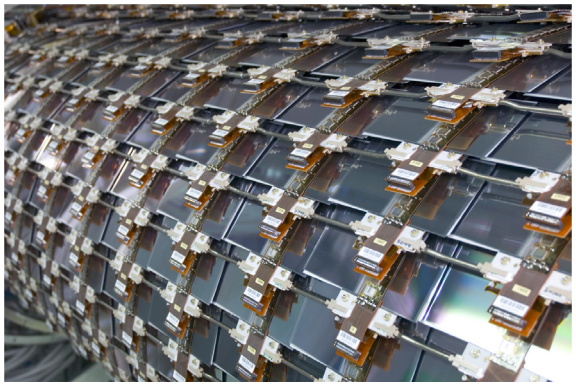

Fig. 2. The ATLAS SCT barrel. The SCT detector consists of 4088 modules (4 concentric barrels and 18 disks) and covers area of about 61 m^2. All services (front-end electronics, cables, optical links and readout are located inside the active volume of the detector.

Lowering the power consumed by the front-end electronics is required in order to reduce the material installed inside the tracker volume by optimizing the cooling system[3] and the power cables. These must be considered in addition to the silicon material of the sensors and ASICs and the support structures, although the latter is typically very light.

This material budget optimization through power consumption optimization is especially important for today's tracking electronics, where the elementary detector modules are used for the construction of large-area barrels with all service electronics located inside the active volume of the tracker, see Fig. 1 and Fig. 2.

value of the Landau distribution) close to 14. This number should be taken with some caution. For example, the silicon sensors optimized for very high spacial resolution (fine pitch), where the signal can be shared between more than two neighboring strips, will required signal-to-noise ratio proportionally higher. On the other hand, the tracker systems suffering from the serious radiation damages occurred during the experiment, where the signal-to-noise ratio drops down to e.g. 12 can still provide meaningful physical data accompanied in this case with slightly higher noise occupancy.

[3] There are many arguments to keep the trackers operating at low or even negative temperatures. The first is to minimize the sensor leakage current, a significant source of parallel noise for the front-end system, critical in the case of big area sensors read out by slow electronics. Another important reason is to prevent the reverse annealing of the sensors exposed to the radiation environment.

In this context, the power supply rejection ratio of the front-end electronics is an important aspect of the design as these systems operate in a multichannel environment, which often has many stringent constraints on the power supply system often resulting in sub-optimal performance. As for any single-ended amplifier working with feedback, a good PSRR can be maintained by providing high loop gain. For a preamplifier working with a high ratio of input to feedback capacitances, this can be obtained only by driving the open-loop gain up and keeping the bandwidth higher than the cutoff frequency of the filters used in subsequent stages of the signal processing chain to optimize the signal to noise ratio [8].

The classical theory of signal filtering in the presence of noise is described in [10] and [11]. Developed for the nuclear spectrometry applications in the middle of the sixties, the focus was primarily on enhancing the signal to noise ratio without emphasis on the power consumption or the time necessary for signal processing, both of which are constrained in front-end electronics for trackers. A good compromise between performance, power consumption, and simplicity, enabling for easy integration in multichannel ASIC is provided by band-pass $CR-RC^n$ filters. Because the filters optimizing the noise affect the signal spectra in the same way, and the signal is usually analyzed in the time domain, they are commonly named shapers. For the preamplifier with so-called continuous-time filtering, where the impedance responsible for the discharge of the feedback is a fixed value, they consist of one high-pass (so-called whitening section) and n low-pass stages. For preamplifiers working in a transimpedance configuration with the time constant of the feedback matched to the time constant of the shaper, the filters consist of only the low pass sections. The same rule applies for the preamplifier with a reset switch in the feedback, where the high pass limit is imposed by the integration time set by the control sequence. The particular implementation of the shaper will depend on the requirements concerning the final gain of the front-end channel, available power budget, and process used.

4. Input stage architecture: the key points

To build a high gain amplifier, the designer has two possibilities: assembling consecutive stages into the cascade of common-source amplifiers; or obtaining the high gain in one single stage by boosting the load impedance. The latter technique is employed in cascode circuits, a common-source, common-gate amplifier. In order to compare these two options, a number of aspects have to be taken into account. The most important are power consumption, achievable open-loop gain and gain bandwidth product, and possible limitations of speed due to the Miller effect. Detailed analysis of the frequency behavior and Miller effect in a CSA built with cascade and cascode amplifiers is shown in Appendix A. In summary, there are three reasons why the cascode topology is the standard solution for the input stages of front-end amplifiers for silicon sensors. The first is the suppression of the Miller effect, which might significantly limit the time response of the preamplifier; and the second is the fact that the cascode behaves similarly to the single-stage amplifier with one dominant, low-frequency pole. The latter of these makes it easy to compensate and provide excellent stability margins without any additional power consumption. The last argument to use the cascode is related to the noise versus power optimization. In a properly designed input stage, the series noise contribution is limited to the input device only. In consequence, the cascode, which is a single stage amplifier, provides better power to noise figure than the cascade amplifier which in the case of single ended architecture has to use two extra gain stages.[4]

Another question faced by the designer is whether to use a differential or single-ended input stage. All the designs implemented for use in experiments employing silicon trackers work in single-ended

[4] In case of the regulated cascode amplifier the difference will be limited to one gain stage

configuration, independently of the technology used. This choice has traditionally been driven by the very strict power consumption limits, noise minimization requirements, and also by the fact that strip detectors are intrinsically single-ended. The return of the signal has to be provided by the backplane of the detector and the system ground. This has some implications on the reference for the supply voltages, since to provide a clean signal return path, the source of the input transistor should be at the ground potential.

4.1. Noise optimization

The analysis of the noise performance of a generic front-end amplifier connected to $CR-RC^n$ filter is presented in Appendix C. The analysis is based on the fact that all noise sources in any amplifier can be represented by an equivalent series contribution and separate equivalent parallel contribution. These are transferred to the amplifier input [12]. Formulas (C.8) and (C.11) quantify how these contribute to the final ENC. In the general case, the series and parallel noise contributions can be equalized by varying the time response (t_{peak}) of the shaper. This provides the minimum ENC for a given noise spectra and could be done effectively for the electronics at LEP, where the time in between collisions permitted a rather relaxed peaking time of the front-end response. Nowadays the timing is often restricted by rather demanding requirements concerning the time resolution for the trackers build for high luminosity accelerators. Designing faster and faster front-end electronics, the series noise contributions intrinsically become more dominant (see (C.8)). Consequently, the noise optimization concentrates on the minimization of the series noise contribution, bringing total ENC below the required levels and keeping the power consumption within the allowable budget.

Although the voltage gain seen at the drain of the input transistor is usually low (e.g. see the analysis of Miller effect in the cascode presented in Appendix B.2), the dominant noise contribution in the cascode amplifier is the series noise of the input transistor, and the contribution from the cascode transistor is reduced with the intrinsic gain g_m/g_{d_s} of the input device (examples of noise contribution calculations for different transistors in cascode and regulated cascode amplifiers can be found in [13] or [14]). The series noise contribution from the active load or current sources has to be limited either by lowering its transconductance by increasing the transistor length (effective in old technologies) or resistive degeneration [15] (deep submicron processes and bipolar circuits). In a carefully optimized design, the dominant series noise contribution is from the input transistor only.

Since that the input transistor contributes as a series noise source, its contribution is proportional to the input capacitance and inversely proportional to the square root of its transconductance and response peaking time (see formula (C.14)). Even though longer shaping results in better noise filtering, the practical upper limit of the peaking time is the required time resolution of the front-end channel or, for the applications allowing for longer shaping, the parallel noise contribution.

Optimizing the dimensions of the input transistor involves a trade-off between the achievable transconductance at a given bias current, determined by the W/L ratio, and the gate capacitance, which is proportional to its area, thus $W \times L$. This optimization requires analytical formulas for the transconductance and intrinsic gate capacitances valid for the transistor biased in weak, moderate, and strong inversion regions. Although this can be easily provided by the use of the EKV model [16], prior to its existence, the optimization was done assuming that the input transistor operates in weak or strong inversion regions, which was not always true. Indeed, a good fraction of these earlier designs had the input transistor biased in the moderate inversion region. Some examples of the noise optimization before EKV era can be found in [17,18], an optimization example using the EKV model can be found in [19].

Table 1
Transit frequency of minimum length NMOS transistors biased with specific current for scaled CMOS processes calculated according to formula (1).

Process node	K_P	t_{OX}	f_T @I_{SPEC}
CMOS 3 μm	44.9 μA/V^2	50.5 nm	66 MHz
CMOS 2.4 μm	51 μA/V^2	40 nm	93 MHz
CMOS 1.2 μm	71.5 μA/V^2	25.8 nm	330 MHz
CMOS 0.8 μm	100 μA/V^2	16 nm	660 MHz
CMOS 250 nm	300 μA/V^2	5.8 nm	7 GHz
CMOS 130 nm	750 μA/V^2	2.2 nm	25 GHz
CMOS 65 nm LP	300 μA/V^2	2.6 nm	50 GHz

4.2. The impact of technology scaling

The input stage architectures have evolved to meet increasingly more demanding requirements from the experiments. These primarily concern the time resolution and readout speed, however, the advances in the CMOS processes, mainly the scaling, also play a significant part. A conventional figure of merit to compare different CMOS technologies in terms of their speed is the transit frequency (f_T), defined as the frequency at which the small-signal current gain of the device working in common-source configuration drops to unity. Usually, for a given process, the so-called peak f_T is provided. However, this is not a very meaningful figure of merit for the design of analog circuits as it represents only the highest possible value obtained typically for the minimum size transistor working in deep strong inversion. A much more relevant quantity might be the transit frequency calculated for a transistor operated in the moderate inversion region as this is the typical operating point of the transistors in a low power amplifier. Using the EKV model [16] it is relatively easy to derive the formula (1) for the f_T of a transistor biased with so-called specific current (I_{SPEC}) corresponding to the intersection of strong and weak inversion asymptotes. For the g_m/I_d methodology [20], now used more and more frequently for the design of low power amplifiers, this bias corresponds to the current at which the transconductance falls to 63% of its maximum value in weak inversion. Using the classical formula for $f_T = g_m/(2\pi C_g)$ and the EKV model for transconductance, specific current and intrinsic gate capacitance $C_g = C_{gs} + C_{gb}$ which for I_{SPEC} is approximately 0.55 C_{ox} one can obtain:

$$f_T\,@I_{SPEC} \cong \frac{1.15\ K_P\, t_{ox}\, U_T}{\pi\, \varepsilon_{ox}\, L^2} = \frac{1.15\ \mu_0\, U_T}{\pi\, L^2} \tag{1}$$

where K_P is the transconductance parameter, t_{ox} is the gate oxide thickness, U_T is the thermal voltage, L is the transistor length and μ_0 is the carrier mobility. Table 1 presents the calculated values of transit frequencies for the minimum length NMOS transistors biased with I_{SPEC} for the technologies used in HEP for tracking applications over the years.

One should keep in mind that Table 1 presents the comparison of f_T calculated for one specific bias in the middle of the moderate inversion region. For the designs implemented in old processes with very low K_P, most of the transistors except the input device were biased towards the strong inversion region providing higher speed than indicated by Table 1. It should be noted that the improvement of the calculated f_T for the scaled processes is due to the smaller transistor feature size and not better carrier mobility, which degrades slightly towards deeper submicron processes: for example: 656 cm^2/(V s) for 3 μm process node and 478 cm^2/(V s) for 130 nm CMOS. Therefore, to fully exploit the advantages of the scaled CMOS technologies in terms of speed it is necessary to use smaller transistor lengths. The subsequent degradation of the output conductance and, in consequence, the intrinsic gain of the scaled transistors has to be compensated by boosting techniques, namely cascoding of the loads and use of regulated cascodes.

For the CSA which is a close loop system, the frequency behavior and timing response will depend on the position of the internal poles of the amplifier, and feedback characteristics, as well as both the input

and output loads. As it was shown in Appendix A, for the cascode amplifier, the dominant pole depends on the cascode output impedance and the parasitic capacitance seen at this node. Consequently, the upper limit for the GBP of the cascode will depend on the transconductance of the input device and the cascode output capacitance. In CMOS cascode designs, the GBP is also affected by the position of the second, non-dominant, pole of the cascode which depends on the g_m of the cascode transistor and the capacitance seen at its source. This capacitance will consist of the gate–source capacitance of the cascode transistor, C_{gs}, (so in this sense the f_T of this transistor will be the upper limit for this pole), and all parasitic capacitances seen by this node. Note that these cannot be considered negligible because of the dimensions of the input and cascode transistors, as well as the extra current source (folded cascode bias or current source boosting the g_m of the input transistor in telescopic cascode).

Aside from the influence on the frequency behavior of the preamplifier, the dimensions of the input transistor have to be optimized for its noise contribution, as was discussed in Section 4.1. The scaled processes characterized with a higher transconductance parameter facilitates the biasing of the input transistor closer to the weak inversion region. This maximizes the transistor transconductance obtained at the given bias and minimizes the gamma noise factor, the combination of which results in a better power to noise figure.

Table 1 shows the values of f_T calculated for the minimum length of the transistor for various technology nodes. Usually for the analog design and in particular for low noise, low power, front-ends we use transistors of different lengths. Sometimes the length is constrained by the MOSFET noise performance, particularly the excess noise factor reported in many technologies for minimum size transistors. Sometimes the transistor length must be optimized for the intrinsic gain g_m/g_{ds} or for better matching, where the transistor area must be considered in addition to the speed as part of the optimization.

4.3. Bipolar technology: an alternative to scaled CMOS processes

Although the concept of the transit frequency was introduced to assess the frequency response of a single transistor working in common-source or common-emitter configuration, its physical interpretation based on the transit time of the charge carriers through the MOSFET channel or collector–emitter contacts in BJT [21] allows for its use as a general figure of merit for the comparison of various CMOS nodes and bipolar processes. Even so, in case of charge sensitive amplifiers, care should be exercised when using numbers presented in Table 1 when comparing CMOS processes with the bipolar technologies, as the latter offers small devices with very low parasitics and high f_T at low collector currents. Keeping in mind that the g_m for BJT depends mainly on the bias current and not the transistor dimensions, i.e. one can use small devices even at the CSA input,[5] it is not surprising that the designs implemented even in old bipolar technologies will have in general very high bandwidths. For example, the input stage of the ABCD chip (ATLAS tracker), detailed in Section 6, implemented in the DMILL BiCMOS process using a BJT with 4 GHz f_T (2 GHz for the biases used in the design) has an open-loop gain of the order of 65 dB and a GBP of approximately 1 GHz. A similar GBP was achieved for the input stage of the ABCStar chip (ATLAS tracker upgrade) implemented in a 130 nm CMOS process with the f_T of the NMOS transistors of about 25 GHz (see Table 1).

Of course, the choice between a CMOS or Bipolar process for a given application is impacted not only by the usually superior frequency behavior of the bipolar design, but also other issues like availability, price, lead time for manufacture, and now most importantly in the current era, the required radiation hardness. This last requirement, increasingly demanding for new experiments, can compromise the advantage of the higher transconductance of the bipolar devices. While the shot noise of a BJT can be much lower than the thermal noise of a MOS transistor for the same bias condition (resulting from the slope factor, gamma factor, and a possible excess noise factor in the MOS device, compare Eqs. (C.14) and (C.16)), the contribution from the base spread resistance of a relatively small BJT optimized for radiation hardness, coupled with the severe degradation of beta post-irradiation can increase the BJT noise [22] to an extent that exceeds the thermal noise of the equivalently biased MOS transistor. From this point of view, CMOS processes with a feature size of 130 nm and below, capable of providing the required speed, are a better choice for present and near-future tracking applications.

[5] However not the minimum size because of noise contribution from the base spread resistance.

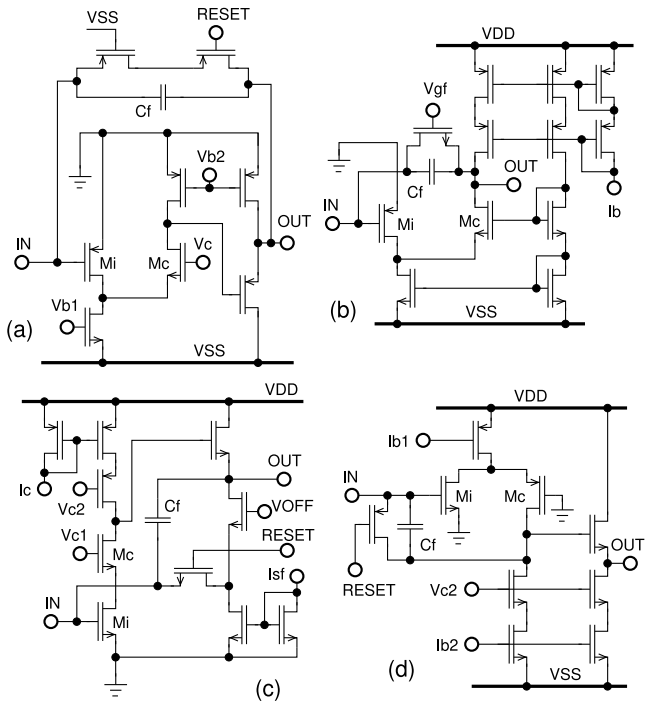

Fig. 3. Simplified schematic diagrams of the input stages; (a) MX3 chip, (b) AMPLEX chip, (c) SVX chip, (d) CAMEX chip.

5. Input stages: trackers for LEP and CDF

The successful construction and operation of the first silicon trackers at the UA2 experiment at CERN and at the Mark II experiment at SLC opened the way for larger scale detector systems in practically all HEP experiments. Larger-scale systems were subsequently built for the LEP and Tevatron experiments, starting from the middle of the eighties. At that time, designers had access to CMOS processes with a feature size of 3 μm, offering very good intrinsic gain for single transistors, much above 40 dB, but not much in the way of speed. Although the timing requirements imposed by the collider, namely the time between collisions, varied from case to case, in general, they were not very difficult to achieve with this technology node and, in most cases, it was possible to optimize the shaping time to get the requested noise performance at very reasonable current biases. This was important for lowering power consumption since the nominal supply voltage for this process was around 10 V. A limited but representative selection of the input stages designed at that time is presented in Fig. 3.

To provide power consumption below 2 mW per channel, as was required by most of the applications, one had to limit the current in the input device below 150 μA in order to leave some budget for the rest of the circuitry. Additionally, this meant powering at least the input transistor with a reduced supply voltage. This was easily

achievable in the folded cascode configuration used in the majority of the designs, where the input transistor was supplied with half of the nominal technology voltage, see Fig. 3. Reducing the bias in the cascode transistor with respect to the current in the input device and using a long transistor in the load, a reasonable open-loop gain of above 60 dB was achievable and was reported by most of the designs. This optimization has to be done with care since lowering the bias current of the cascode transistor affects the GBP of the preamplifier by effectively moving the non-dominant pole of the cascode towards lower frequencies. This usually requires stronger compensation, further limiting the bandwidth.

Although the bandwidth of the input stages was not always explicitly published, when absent, it can be easily estimated from the measurements of the signal rise time and of the extrapolated position of the dominant pole. This was done for the MX3 front-end and it was found that, when approximated this way, the GBP of the input stage was found to be around 30 MHz (see [23]). In general, the low bandwidth of the input stage was not a big issue for the designs targeted for LEP experiments, since the 22 μs beam-crossing interval allowed for very relaxed shaping times in the range of 1 to 2 μs (see MX3 noise optimization in [24]). As with many designs from those days, discharging the preamplifier feedback capacitor was accomplished using a reset transistor switched during the inactive phase of the readout. Despite the simplicity, this solution has some disadvantages, mainly the parasitic charge injection from the gate of the reset switch to the preamplifier input and possible interference from the digital control line to the input degrading the PSRR. In addition, designs targeting experiments at synchronous colliders make this solution rather unpopular today since it excludes possible use of the front-end designs in other domains like nuclear medicine, etc.

For the slightly faster Amplex chip (800 ns peaking time) designed originally for the UA2 experiment with Bunch Cross Over (BCO) period of 3.5 μs, the limited bandwidth of the input cascode loaded directly with the feedback and shaper input capacitances was an important contribution to the final shaping of the signal. The details of the design can be found in [18]. Although not ideal from the PSRR point of view, it was justified by the very low power consumed by the input stage, biased with only 50 μA (the required power consumption for UA2 tracker was below 1 mW per channel). Excellent noise performance at low input capacitances was obtained due to the novel approach for the feedback using long MOS device working in the linear region. With the equivalent resistance of this transistor reaching tens of MΩ, the parallel noise contribution was negligible, even for shaping times in the range of micro-seconds. The later implementations of the Amplex chip, the Viking chip, and the VA family of chips, in scaled processes had slightly faster preamplifiers and slower shapers (depending on versions 1.5 to 2 μs peaking time) and exhibited outstanding noise performance (see [17,25]).

Another approach was used for the design of the SVX front-end amplifier [6] designed for the CDF experiment (BCO period initially 3.5 μs, then reduced to 396 ns, and subsequently to 132 ns). The gain-bandwidth product obtained in the buffered telescopic cascode with an NMOS input device used to provide better transconductance at a given bias, was about 160 MHz. This was an excellent achievement for 3 μm CMOS process. Several different SVX versions were designed and manufactured over the years, using scaled processes for improved noise/power figures. As in the case of the ASICs designed for LEP experiments, the preamplifier uses a reset switch as a discharge device.

The CAMEX preamplifier [26–28] designed for the ALEPH experiment at LEP was built around a buffered folded cascode with an NMOS input transistor. The chip was implemented in the (slightly older at that time) 3.5 μm CMOS process, with t_{ox} of 80 nm. This process had a rather low transconductance parameter. Even with the NMOS device at the input providing better transconductance at the designed bias current, the GBP was only 3.5 MHz, and the open-loop gain was approximately 60 dB. Similar to the other designs, the preamplifier used a reset switch in the feedback network. It was the first front-end amplifier implemented in a CMOS technology to use a cascode in the input stage.

Although the size of the input transistors in these old designs was large, the possible contribution from the flicker noise could not be neglected, especially for longer shaping times.[6] Except for the cases where the circuit has been optimized for speed, like SVX or CAMEX, a majority of the input stages used PMOS transistors at the input which are intrinsically better from this point of view. Even though the flicker noise tends to decrease in scaled technologies (see [30]) this contribution should always be taken into account, even for present designs implemented in deep submicron processes, and especially when designed with longer shaping times. Given that current designs generally use smaller devices, care over the flicker noise optimization is especially important. In addition, the increase in flicker noise seen after exposure to ionizing radiation (see [31]) and the generally more pronounced effect seen with NMOS devices further increases the importance of careful design with respect to this parameter.

6. Input stages designed for trackers for the LHC

The effects of radiation on both the sensors and the electronics were recognized since the beginning as problematic, even at doses as low as a few tens of kRad. Although the effects on the front-end electronics were visible, the electronics designed for the LEP1 run possessed sufficient intrinsic hardness to provide stable data for the physics. With the increased luminosity of the LEP2 machine, the trackers [32] were upgraded with versions designed in rad-hard CMOS processes already available at that time: the MX7 used the 1.2 μm Harris [33]; and the SVX3D used the 0.8 μm Honeywell [34]. Although access to radiation hard CMOS technologies at the beginning of the nineties was possible within the HEP community, moving to high luminosity colliders, and especially the LHC, presented significant challenges, mainly due to the greatly increased beam-crossing rate. The 25 ns BCO period, originally planned for 15 ns, set very demanding requirements for the time resolution. Together with long sensor lengths (13 cm strips for the ATLAS SCT), this resulted in demanding bandwidth requirements for the front-end input stages. Since the existing CMOS technologies with 1.2 μm and 0.8 μm feature sizes were not suitable to design adequately fast preamplifier for typical input capacitances of 20 pF arising from the target sensor geometries, a logical solution was to exploit available bipolar technologies.

One initial candidate was SHPi process from Tektronix (later Maxim) offering fast, 9 GHz f_T bipolar transistors and p-channel JFETs with f_T of about 600 MHz. At the beginning of the R&D phase for the LHC electronics, several fast transimpedance amplifiers implemented in this process already existed, including a 35 ns peaking time amplifier/discriminator designed for the HERA experiment [35].

The FABRIC chip, designed for the NA50 experiment at the SPS [36], achieved performance closer to the LHC tracking detector requirements. With a peaking time below 15 ns at a power consumption of 1.3 mW per channel, it was the fastest, low noise and low power front-end build for any silicon strip detector at that time. The GBP of the input stage was around 3.75 GHz and the open loop gain was 68 dB. The simplified schematic of the input stage of FABRIC is shown in Fig. 4(a). The telescopic cascode built with two NPN transistors is loaded with a current source using a resistive-degenerated P-channel

[6] The absolute contribution to the total ENC from the flicker noise is independent of the response peaking time (see e.g [29].). For the slow front-ends, where the peaking time can be optimized in order to minimize the series and parallel noise contributions, the flicker noise imposes the limit for the achievable noise performance, which can be improved only by the increasing of the transistor area or correct choice of the transistor type (PMOS instead of NMOS). This is usually not the case for the fast front-ends optimized for low power, where the dominant contribution is from the channel thermal noise.

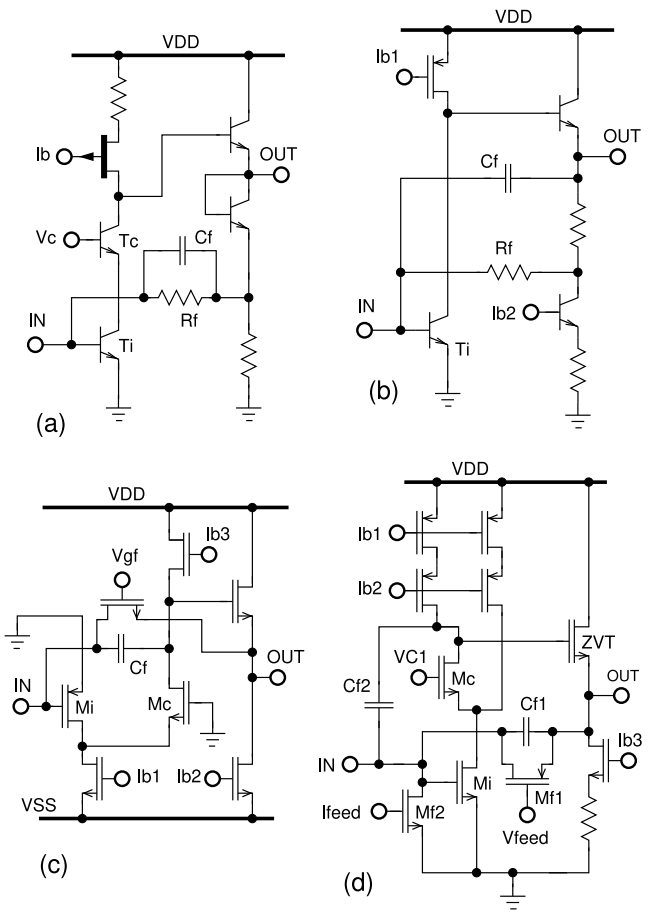

Fig. 4. Simplified schematic diagrams of the input stages of: (a) the FABRIC; (b) the ABCD; (c) the APV25; and (d) the ABC250 chips.

JFET and is buffered with an emitter-follower. The preamplifier works in transimpedance configuration i.e. the relatively low-value resistor provides fast discharge of the feedback capacitor with the time constant of the shaper. The same input stage architecture was used in the LBIC chip [37], the early prototype of the CAFE ASIC proposed for the ATLAS SCT with a design peaking time of 20 ns, more tailored for the LHC BCO.

In parallel to front-end ASIC implementations in Maxim's technology, a considerable effort was invested into prototyping in the radiation hard BiCMOS DMILL process [38], which became available for HEP users in 1994.

DMILL was offering fast, 4 GHz vertical NPN transistors, together with 0.8 μm radiation-hard CMOS process on the same die. The oxide covering the BJT was the same quality as used for the gate of the CMOS transistors, which was important since contrary, to the Maxim devices, the DMILL bipolar transistors did not suffer from a low dose rate effect (see [39]). This, together with the fact that on the same die complex CMOS digital logic for data processing could be implemented, were the main reasons why the DMILL technology was selected for the ATLAS SCT. The simplified schematic diagram of the input stage of the front-end chip for the ATLAS SCT, the ABCD ASIC, is presented in Fig. 4(b). The preamplifier is built with a common-emitter amplifier loaded with a long PMOS transistor, and buffered with an emitter-follower. The input transistor emitter area was optimized to $1.2 \times 10\,\mu m^2$. This choice was a compromise between the decreased radiation hardness seen in larger transistors due to the lower current densities resulting in more severe β degradation, and limiting the base spread resistance to approximately 100 Ω, due to its contribution as a series noise source. For this size, the base-collector capacitance is relatively small, and the Miller effect is negligible. Consequently, the use of a cascode in the input stage is not justified. The open-loop gain obtained in this stage is around 65 dB and the GBP is around 1 GHz with the first dominant pole placed rather high at around 3.5 MHz. The preamplifier works in a transimpedance configuration to avoid saturation of this stage given the expected signal rate. It is also optimal for lowering the input impedance and consequently the crosstalk. The power consumption of the analog part is around 2 mW per channel. Further details of the design can be found in [40].

The deconvolution method was proposed by the RD20 program at CERN as an alternative solution for front-ends designed in bipolar technologies (see [41]). This method uses a relatively slow, 75 ns peaking time, preamplifier/shaper stage and recovers the timing information using an Analog Pulse Shape Processor (APSP) circuit that processes consecutive 25 ns samples stored in the analog memory provided for each channel. Several prototypes were submitted in various standard and rad-hard processes, mainly 1.2 μm AMS, Harris and also 0.8 μm DMILL. The final chip designed and optimized for the CMS tracker, APV25 [42] was implemented in a 0.25 μm CMOS technology which became available for HEP users in 1998. The simplified schematic diagram of the front-end input stage is shown in Fig. 4(c). In general, it follows the architecture of the Amplex front-end amplifier. The unbuffered folded cascode with PMOS input device works in charge mode with the linear transistor in the feedback loop. In the final design, the peaking time of the preamplifier/shaper was reduced to 50 ns. The power consumed by one channel of the preamplifier/shaper and the APSP was around 1.35 mW. Details of the design can be found in [43].

The substantial reduction in threshold voltage shift induced by ionizing radiation in CMOS devices with oxide thickness below 10 nm had already been predicted in the middle of the eighties [44,45]. This was confirmed for the 0.25 μm process during the intensive qualification program pursued by RD49 collaboration at CERN [46]. The design of enclosed geometry NMOS transistors was proven to be an effective solution to the source–drain leakage issues arising due to the radiation-induced hole trapping effects in the field oxide isolation (FOX) [47]. In this way the HEP community gained access to this commercially available yet radiation tolerant CMOS technology, which solved all previous issues related to the use of specialized radiation-hard processes available up to that point. These issues were chiefly: high costs, relatively low yield, and long manufacturing time, amongst others.

Besides the radiation tolerance, the quarter micron CMOS technology was the first process offering the transistors with a f_T capable to compete with bipolar devices. Fig. 4(d) shows the input stage of the CMOS fast preamplifier designed with the specifications used for the bipolar front-end in the ABCD chip. The telescopic cascode built with the input NMOS transistor M_i is loaded with the low voltage cascode current source. An extra current source directly supplying the input transistor boosts its transconductance, effectively improving the bandwidth. The open-loop gain is around 83 dB with a GBP of about 600 MHz. The position of the first dominant pole is equivalent to the position of the dominant pole in the ABCD input stage, which has the same gain at 50 MHz of around 40 dB. The input transistor in this version is large, measuring 2000 μm wide by 0.5 μm long. The resulting parasitic capacitance lowers the position of the cascode's non-dominant pole, reducing the GBP compared to the bipolar version of the circuit. Nevertheless, the position of this pole is sufficiently high (around 100 MHz[7]) to not affect the AC parameters of the channel. An example of this is the crosstalk, which is even smaller than the equivalent bipolar version (6% versus 8% for 13 cm strips). The preamplifier works in transimpedance configuration with active feedback using a PMOS transistor M_{f1} biased in saturation, with a constant current source built with M_{f2} (see [48] for a good description of active feedback). With the 300 μA bias of the input transistor (to be compared with 200 μA in the

[7] The central frequency of the filter in the $CR - RC^2$ shaper for 22 ns peaking time is around 10 MHz.

ABCD) it provides the same noise and speed performance as the bipolar version at a lower power consumption (1.5 mW versus 2 mW), in part due to the lower supply voltage (2.5 versus 3.5 V). Further details of the design and performance are described in [19]. Although this front-end was not used in the ATLAS SCT (at that time the production of the DMILL version had been already launched), it demonstrated the possibility of designing fast CMOS front-ends in commercially available submicron processes and was therefore an important step towards the front-end electronics required to fulfill the design requirements imposed by tracking detectors for high luminosity LHC.

7. Upgrade for high luminosity LHC

The development of front-end electronics for tracker upgrades started right after the completion of the present generation of detectors, even before their layouts had been finalized. The R&D work was focused on the development of fast transimpedance amplifiers and shapers optimized for medium sized sensors with capacitances up to 10 pF, capable of dealing with the high predicted signal rates. Besides the increased detector granularity, the higher luminosity provided by the upgraded colliders had an impact on radiation hardness and noise performance requirements of the electronics. The latter of these is strongly affected by the increased signal degradation from the heavily irradiated sensors. In some regions of these trackers close to the interaction point, the predicted radiation levels are up to 100 MRad TID (Total Ionizing Dose), and required noise levels for the electronics are below 1000 e^- ENC. The higher granularity of the sensors has also an impact on the power budget for the electronics due to the increase channel count. In general, the strips will be 2 to 5 times shorter compared to the LHC detectors and ideally, the power should be scaled in proportion. As an example, for the ATLAS ITK where the strips will vary from 2.4 to 4.8 cm the analog power consumption should be below 400 μW per channel. Although the quarter micron node demonstrated its capabilities in terms of speed, it was clear that both the analog and digital power consumption would exceed the budget for front-end chip designs fulfilling the new requirements. The logical step was to move to the 130 nm process node which became commercially available for HEP users in 2007, and was subsequently characterized in terms of its radiation tolerance up to 100 MRad TID [49] at CERN. The appearance of a new type of device isolation, STI (Shallow Trench Isolation), permitted radiation-induced drain–source leakage in the regular NMOS devices to be kept within tolerable limits, allowing linear layout transistors to be used in most cases. The 130 nm node also provides very good noise performance with no excess thermal noise and reasonable flicker noise for channel lengths above 300 nm [50]. Increased flicker noise in NMOS transistors after irradiation with ionizing radiation was found to be caused by effects in the STI [51] and not the gate oxide. Consequently, all NMOS devices critical from the noise performance standpoint have to be designed with an enclosed geometry layout in order to keep to a steady level of flicker noise over the lifetime of the detector. To fully exploit the advantages of the 130 nm node in terms of speed, one has to scale the design down i.e. to use a smaller length of the transistors (see Table 1). The main consequence of this is a drop in the intrinsic gain to below 30 dB for transistor lengths around 300 nm. The high open-loop gain for the cascode amplifier can still be maintained if the boosting technique is used. It has been demonstrated that with an NMOS regulated cascode amplifier loaded with regulated active load, an open loop gain of 80 dB and the GBP above 1 GHz is achievable [14].

Fig. 5 shows the input stage of the ABCStar front-end for ATLAS ITK implemented in 130 nm node. The preamplifier is built with a telescopic regulated cascode amplifier with the NMOS input transistor biased in the moderate inversion region with 130 μA. The input cascode is loaded with a low-voltage cascode current source. An extra current source boosts the transconductance of the input transistor, optimizing the bandwidth. The GBP is around 1.5 GHz and the open-loop gain is around 75 dB, which is sufficiently high for the intended

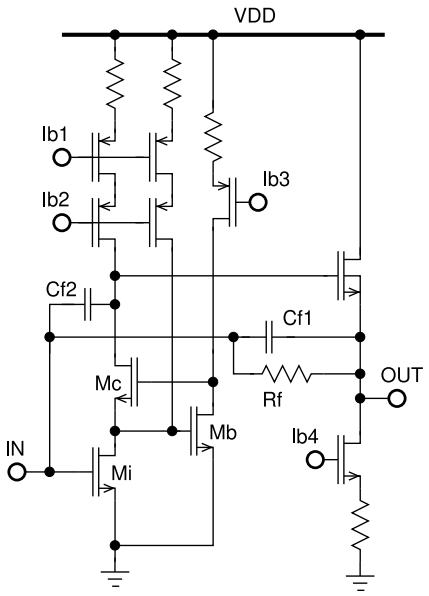

Fig. 5. Simplified schematic diagrams of the ABCStar input stage.

detector size of up to 5 cm length, with an expected capacitance of 5pF. In addition to the number of transistors with various threshold voltages and metal–insulator–metal (MIM) capacitors, the 130 nm node offers high-value polysilicon resistors which can be used for both the preamplifier feedback and the degeneration of all current sources. The preamplifier works in transimpedance mode to allow the correct processing of the high signal rates expected. The architecture of the preamplifier, typical for input stages designed for LHC front-ends, is optimized for the bandwidth and provides optimal power to noise figure for the fast shaping times typical for the LHC electronics. The contribution from the flicker noise from the input transistor is less than 5% and does not degrade with the irradiation since all NMOS transistors in the preamplifier are laid out with an enclosed geometry configuration. With the overall current consumption of 260 μA per channel and peaking time of the shaper in the range of 22 ns, it shows good noise performance compatible with the requirements imposed by the heavily irradiated sensors expected in the future experiment. The details of the design and performance can be found in [52].

In addition to the 130 nm node widely used for the design of front-end ASICs for TID levels below 100 MRad, the HEP community is currently exploiting the 65 nm technology node for chips foreseen to operate in a more severe radiation environment. This technology has been qualified at CERN for doses up to 500 MRad and is used primarily for front-end pixel chips installed close to the interaction point or for on-detector fast digital chips for data aggregation and transfer. Nevertheless, it can be also used for the design of front-end electronics for strip sensors. The 65 nm variant selected for these applications is a low power version (LP) with 2.8 nm (relatively thick) gate oxide, and lower transconductance parameter, comparable to that of the 250 nm technology. It has the advantage of smaller transistor feature sizes, thus a higher f_T, and good noise performance. The smaller transistor length results in a necessary compromise between the GBP of the input amplifier and its open-loop gain that must be made during the design optimization. The example of the application of this technology node might be the amplifier designed for the CMS outer tracker modules with strip sensors of 2.5 cm. This application requires tolerating TID doses up to 200 MRad, therefore the 65 nm process is a more appropriate choice than the 130 nm node. With practically the same architecture as that used for the ABCStar chip, the preamplifier has 65 dB open-loop gain and a GBP of 2.7 GHz. In this case, the open-loop gain, which is sufficiently high for the intended length of the strips, has been

traded off to obtain better bandwidth and consequently better PSRR at high frequencies. This optimization is necessary because the chip will be supplied directly with a DC/DC converter situated on the detector module. The details of the design can be found in [53].

8. Dealing with sensor leakage current

The silicon strip tracker example input stages examined so far do not comprise special circuits for the compensation of the sensor leakage current in contrast to the typical pixel design [54]. The reason is twofold. Firstly, the typical front-end for strips is optimized to give an adequate signal-to-noise ratio at minimum power consumption. Adding another contribution from the compensation circuit will result either in deterioration of the noise performance to below a level deemed acceptable, or an increase of power to compensate for the noise degradation. Secondly, most front-end designs can tolerate sensor leakage current to an appropriate level without any impact on the performance. For the LEP experiments, where most of the sensors were DC coupled, the preamplifiers could be reset every BCO cycle. In addition, the front-ends were insensitive to slow drifts of the preamplifier output voltage caused by evolving leakage currents due to double correlated sampling performed before the output stage. The same approach of double correlated sampling was used in the SVX family of chips [55]. Although this method was effective for compensation of the DC drifts due to leakage current and cancellation of low frequency noise, one should keep in mind that it causes the increase of the series white noise contribution by about 40%. For that reason double correlated sampling was used in slow electronics where the noise could be optimized by increasing the shaping time and equalizing the contributions of series and parallel noise sources. It has been completely abandoned in fast front-end electronics where the dominant contribution is from the thermal noise of the input transistor.

As the Tevatron's BCO rate rendered it impossible to reset the preamplifier with each BCO as had been done at LEP and earlier colliders, the dynamic range of the front-end channel was set to ±200 fC to allow for initialization of the preamplifier during the periodic beam gap. Due to its resistive feedback architecture and dynamic range, the Amplex type preamplifier could tolerate a reasonable level of leakage as well (see [18]).

Although fast transimpedance preamplifiers with resistive feedback can tolerate some leakage current without degradation of the analog performance, the voltage drift at the output will diminish the margins for the DC operating point of the device in question. This concerns especially those front-ends designed in submicron CMOS processes for binary readout, operating at relatively low supply voltages, and with a rather high gain and low input dynamic range, typically below 10 fC. In this case, the extra DC shift in the preamplifier output voltage caused by the leakage combined with process and temperature variations (PVT) can give a non-operational circuit for some corners. This was already the case for the electronics for the LHC trackers. Advancements in sensor technology allowed AC coupling of the sensor to the input stage avoiding this situation, and all the large-scale silicon trackers built for the LHC detectors were built like this.

9. The evolution of read-out architectures

Besides the reception of signals from semiconductor sensors, the front-end chip should provide amplification, noise reduction, and temporary storage of detector signals before sending them out in either an analog, digital, or binary format. Recently an emphasis on enhanced timing information about the signal arrival time and duration has become important for certain applications.

The conditions of the experiment, surface area, number of channels, collisions rate, and the output data rate, have had an important impact on the required architecture of the readout part of the front-end ASIC. On the other hand, the implemented functionality is always a balance between requirements from the experiment and the integration scale of the available technology, the latter restricting the maximum number of the transistors employed on a single chip due to finite area and limited power budget.

The CMOS 3 μm technology first used for HEP applications allowed the integration of relatively simple digital blocks. For the LEP experiments (number of channels below 150 k, and rather relaxed BCO period=22 μs), all the analog sampled data from each channel could be sent by multiplexing them off-detector directly to digitizing, analysis, and acquisition modules. The MX family of chips used widely in the LEP trackers comprised only a per-channel preamplifier, sample and hold circuit (s&h), and the output multiplexer. The shaper functionality was implemented using series resistors and a sampling capacitor creating a simple low pass RC filter improving the signal to noise ratio. The signal gain obtained in the preamplifier stage, of the order of 2.5 mV/fC, was enhanced with an off-chip differential line driver built with discrete components [56,57].

Although the first version of the SVX chip, designed in 3 μm process [6], had a similar readout scheme incorporating the switched capacitor stages in addition to act as low pass filters and discriminators allowing for sparse data readout, the change in the BCO period (from 3.5 μs down to 396 ns and later to 132 ns) required major modifications in the architecture for subsequent implementations. The SVX2 chip [55] designed with 1.2 μm UTMC process consists of a 32 cell deep analog memory built with a capacitor matrix allowing for local data storage before the selection was performed with an external trigger signal. The double correlated sample data were subsequently digitized with a per-channel Wilkinson ADC and stored in an output FIFO. In the sparse data mode, only the channels with signals above the threshold were tagged for the readout, which additionally reduced the quantity of data to be send out of the chip.

The subsequent version, the SVX3 [58], implemented in the radiation hard Honeywell 0.8 μm process, allowed for simultaneous read-write operations on the analog memory. The depth of the dual-port analog memory was extended to 47 cells, from which 4 cells were reserved for tagging as a second-level buffer. This architecture, comprising a primary data storage buffer written to at the BCO rate, followed by a second level buffer in which data selected by the first level trigger decision were stored, became the standard readout scheme for all tracker front-end chips at high luminosity colliders.

The AMPLEX front-end was probably the first design employing a high open-loop gain amplifier in the shaper stage to provide both first-order CR-RC shaping and extra voltage gain. It should be borne in mind that at that time CMOS processes did not offer high-value resistors and long MOS transistors biased in the linear region were used instead. Although in the original 3 μm version of the AMPLEX chip the preamplifier bandwidth also contributed to the shaping of the signal, later versions (Viking and VA family) had faster preamplifier stages and a longer shaping time between 1.5 and 2 μs. This resulted in better PSRR and PVT independence, as well as excellent noise performance. For the design presented in [17] implemented in a MIETEC 1.5 μm process, the gain of the full chain was around 15 mV/fC and the peaking time was equal to 1.5 μs. Having been sampled in the S&H circuit, the channel outputs were subsequently read out serially through an output multiplexer. The power dissipated in the shaper stage was less than 10% of the overall power dissipated in the preamplifier. A similar shaper architecture was used in the electronics designed in the scope of the RD20 program, including the APV family of chips.

The APV25 front-end ASIC designed for the CMS experiment at the LHC is a good reference for analog readout architectures. Access to the full and uncompressed information from each channel of the electronics for a given time slot allowed for enhancement of both the spatial resolution and signal-to-noise ratio in the presence of so-called common-mode noise. Besides the preamplifier and relatively slow shaper (50 ns peaking time) the core of the readout part was the analog memory block (ADB) consists of 192 capacitor cells from which

160 are reserved for the first level trigger buffer, and the remaining locations provide buffering for up to 10 events in deconvolution mode. The signal gain of the channel was around 25 mV/fC, which was sufficiently high to keep the contribution from the non-uniformity of the ADB cells to the output noise at a negligible level. The ADB was read out by the APSP processor which could work either in peak or deconvolution mode. The information from all channels was read out through an analog multiplexer and sent off-detector using analog optical links. The details of the performance of the APV25 ASIC can be found in [42].

There are several arguments for transmitting only binary hit information from the detector module. The main advantages of the binary readout scheme are the simplification of the off-detector electronics and substantial reduction of data to be sent out resulting in a lower number of the optical links, which in addition can be the standard digital grade. For a big tracking system, this design choice will result in lower costs and a significant reduction of the material installed inside the detector. For comparison, the CMS experiment requires one analog optical link per 256 readout channels (two APV25 chips), whereas the ATLAS experiment employs a binary readout architecture allowing for data compression resulting in two, redundant, digital optical links for 1536 readout channels (12 × 128 channel ASICs). The main consequences of these system-level simplifications resulting from a binary readout architecture are more demanding requirements on the PSRR of the front-end, and increased immunity of the full processing chain to external and internal interference as well as common-mode noise. Besides the requirements concerning noise, speed, and power consumption, the variation of gain and discriminator thresholds in between channels becomes a critical problem. This issue is usually solved with a twofold approach. Firstly, the gain of the preamplifier-shaper stage is increased and optimized with respect to the required dynamic range. Designing for a gain of between 50 to 100 mV/fC and good linearity below 6 fC are reasonable trade-offs allowing for trimming and calibration of the binary chain. Secondly, each channel is usually equipped with a local, few-bit DAC allowing discriminator offsets to be trimmed. The first large-scale binary tracker was the ATLAS SCT detector (Semi-Conductor Tracker) employing the ABCD3T ASIC [40] implemented in DMILL rad-hard BiCMOS process. The fast, transimpedance preamplifier is followed by two shaper amplifiers providing both integration and amplification of the signal. The first stage of the shaper is built with the cascade of a common emitter amplifier followed by a common source amplifier, enclosed with strong resistive feedback. This architecture provides good gain and timing stability over PVT variations. The second, AC coupled, stage of the shaper is a single-ended to differential amplifier, which also serves as the threshold interface for the discriminator. This architecture, typical for the bipolar binary front-ends and optimal from the point of view of PSRR, is also used in a number of CMOS submicron implementations (see [19,52]). The gain of the full chain is about 50 mV/fC with the peaking time around 20 ns allowing for the use of a simple leading edge discriminator. The overall shaping function of the circuit is somewhere between a 2nd and 3rd order CR-RC filter constructed using a faster preamplifier and two shaper stages contributing with one short and two slower time constants. Besides the front-end part, the ABCD3T chip comprises a binary pipeline for first-level trigger (132 delay cells), 32 bit deep derandomizing FIFO for 8 events (3 time slots per event are stored), data compression logic, and readout control logic. More details of the operation of the chip can be found in [40].

The overall readout architecture of the front-end chips designed for the high luminosity upgrade is similar to the existing versions currently in use in the LHC experiments. Both ATLAS, as well as CMS, are planning to use a binary scheme for the High Luminosity upgrade. Current progress in the scaled CMOS processes allows for the implementation of more transistors on a single chip resulting in more advanced and redundant functionality, a good example of which is the triplication of essential digital blocks to improve robustness against Single Event Effects (SEE). The memory depth for the first and second-level buffers is bigger than in the past. In the case of the front-end chips for ATLAS and CMS, the latency of the first level buffer has been increased to 12.8 μs. Unlike the current tracking detectors, the possibility for the tracker to generate trigger primitives that contribute to the level 1 trigger has been considered, with an interesting approach to this having been adopted by the CMS chips (CBC2 and SSA). By comparing the information from two layers of the detector module using so-called stub logic, the front-end ASIC can reject the patterns created by low transverse momentum tracks, which are not interesting from the physics point of view (see [59,60]). In addition to the signal processing components, today's front-end ASICs also feature many analog blocks for power management (power regulators), on-chip calibration, bias generators, and monitoring blocks, including ADCs. Modern submicron processes offer various threshold transistors, metal-oxide-metal capacitors, high-value resistors, and inductors. The low resistivity metals facilitate the reliable distribution of power inside the front-end ASIC. All these features increase the level of integration achievable within the area, power, and schedule requirements. As boosting of the speed of the devices comes at a cost for the intrinsic gain of a single transistor, this has an impact on both the input stage and shaper amplifier architectures. For example, the cascade of common source amplifiers used in ABC family chips, providing good performance at very low power, has been replaced in the final ABCStar design by a buffered folded cascode amplifier, providing a better open-loop gain [52]. Nevertheless, scaled CMOS processes bring net positive effects on the analog parameters of the front-end circuits as they can also provide more advanced functionality due to the smaller transistor sizes, higher speed at lower power, and better radiation tolerance for TID as well as SEE.

10. Summary and prospects

Although the selection of front-end designs presented here is rather limited, it forms a relatively comprehensive summary of the front-end instrumentation designed for, and successfully used in, large scale tracking detectors built for HEP over the last 30 years. Each of the chosen examples represents a key milestone in the evolution of the design expertise in the HEP domain and has had an important impact on the design of front-end ASICs for similar and subsequent applications. The MX family of chips dominated the LEP experiments [32], while the SVX family chips were used for decades in the experiments at the Tevatron [61]. The successors of AMPLEX chip (Viking and VA family) were used for the Belle I experiment tracker [62] at KEK, and in the AMS tracker installed on the International Space Station [63]. The RD20 family of chips were used in the CMS tracker, the VELO detector in LHCb experiment (Beetle chip, [64]), the upgraded Belle II tracker (APV25, [65]), and in experiments at Hera (HELIX chips [66]). The BiCMOS ABCD front-end chips have been installed in the ATLAS SCT detector since 2004.

Looking to the near future, commercially available deep submicron processes accessible to the HEP community are well suited for the design of front-end electronics intended for the present upgrades of high luminosity LHC trackers.

Given the relatively long design and construction timescales foreseen for the next generation of colliders and the associated experiments, it is difficult to precisely say how the expected environment and tracking requirements will drive the performance specifications of the front-end electronics for these tracking detectors. Given the continual advancements made by the CMOS industry, it is also hard to predict the CMOS technologies that will be available to us at that time.

The required front-end architectures will also depend on the sensor technologies available and suitable for these trackers. The progress and development of monolithic CMOS sensors, especially their radiation hardness and charge collection speed, introduces new and exciting possibilities to simplify and further automate the integration and construction of such detectors.

At the time of writing CERN has launched several R&D programs focusing both on sensors and front-end electronics with the emphasis on possible applications at the Future Circular Collider (FCC). The specifications derived from the predicted luminosity, time resolution, and radiation hardness are extremely challenging and the radiation hardness in particular far beyond that possible with the CMOS processes currently in use. HEP groups are starting to look at 28 nm node and CERN will launch the intensive qualification program for this process soon.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Frequency behavior of the cascade and cascode amplifiers

The schematic diagram and the equivalent model of a generic three-stage[8] cascade amplifier is shown in Fig. A.6(a) and Fig. A.6(b) respectively. The evaluation of the frequency characteristic can be done using a simple chain-type calculation. For the simplicity of the calculations and easier interpretation of the results, one can assume that the load impedance is equal to the output impedance of a given active transistor in the common-source stage i.e. $r_{L1} = r_{ds1}$, $r_{L2} = r_{ds2}$ etc. This assumption is reasonable, since for any load impedance, the obtainable gain will be limited by the r_{ds} of the active transistor connected in parallel. The gain of the first stage, yielding the Miller effect, is given by expression (A.1). The bandwidth is limited with a single, high-frequency pole determined by the r_{ds} of the input transistor and the parasitic capacitance seen at its drain.

$$K_{v1}(s) = -\frac{1}{2}\frac{g_{m1}\, r_{ds1}}{(1 + s/P_1)} \quad \text{where} \quad P_1 = \frac{2}{C_1\, r_{ds1}} \tag{A.1}$$

Obviously, the gain of the full chain is a product of the gains of all stages and the circuit will consequently have three high-frequency poles located close to each other. Although this input stage circuit is designed with capacitive and resistive feedback and not in unity gain configuration, its frequency compensation is still demanding and usually requires the use of relatively high-value capacitors with the consequence of an increase in power consumption.[9] Indeed, the per channel power consumption of the Microplex chip, the first front-end ASIC for strip sensors implemented in 5 μm NMOS process, which used the cascade of common-source amplifiers in the preamplifier stage [68], was in the range of 12 mW. This was almost an order of magnitude higher than early front-ends using a cascode input stage.

Fig. A.7 shows the simplified schematic diagram of a telescopic cascode amplifier built with NMOS devices. Understanding this circuit is most easily achieved using nodal analysis of the equivalent schematic, which is shown in Fig. A.7(c). Eqs. (A.2)a … (A.2)d give the current i_2 flowing through r_{ds2}. Solving for v_o and v_1, expressions for the cascode

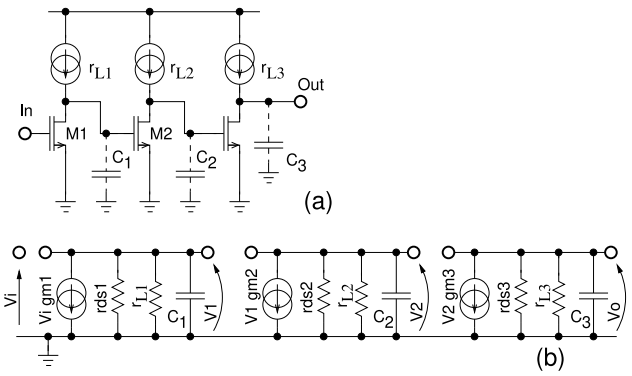

Fig. A.6. The cascade of common-source amplifiers. Simplified schematic diagram (a) and equivalent model (b).

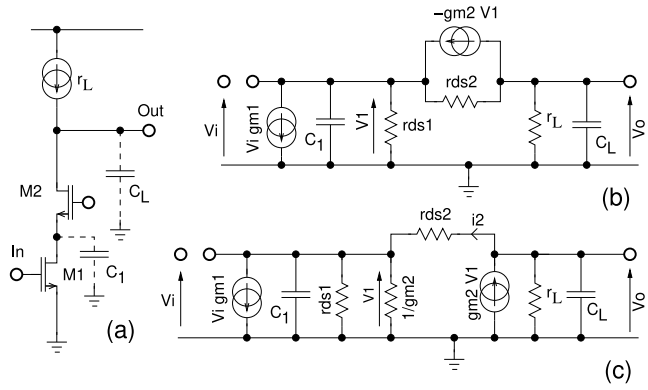

Fig. A.7. The cascode (common-source, common-gate) amplifier: (a) schematic diagram, (b) equivalent model, (c) equivalent model after source rearrangement and substitution.

gain (K_v) and the gain seen at the drain of the input transistor (K_{v1}) are derived, which are important to evaluate the Miller effect.

$$i_2 = g_{m2}\, v_1 - \frac{v_o}{Z_L} \tag{A.2a}$$

$$i_2 = v_i\, g_{m1} + v_1 \left(\frac{1}{r_{ds1}} + g_{m2} + s\, C_1\right) \tag{A.2b}$$

$$i_2 = \frac{v_o - v_1}{r_{ds2}} \tag{A.2c}$$

$$Z_L = \frac{r_L}{1 + s\, C_L\, r_L} \tag{A.2d}$$

Considering two different cascode load cases facilitates the interpretation of the analysis results. For those preamplifier circuits implemented in old processes with high intrinsic transistor gain, the cascodes were usually loaded with a single long channel transistor current source. This easily provided an open-loop gain in the range of 60 dB which was sufficiently high for these early designs. To simplify these calculations, it is assumed that the output conductance of the load is equal to the output conductance of the cascode transistor ($r_L = r_{ds2}$). This assumption is reasonable since the cascode transistor is usually optimized for high output conductance and low parasitic capacitance, i.e. a narrow transistor with lower g_m but high r_{ds}. This is unlike the input transistor, which is always optimized to minimize the noise contribution by designing a wide but short channel device with relatively low r_{ds} and thus high g_m. Solving Eqs. (A.2) and replacing the r_L with r_{ds2} we get simplified formulas for the gain of the first stage (K_{v1}) and the cascode gain (K_v) loaded with a single transistor current source (expression (A.3) and (A.4)). These approximations rely on the assumption that the transistor's g_m is much greater than its g_{ds} and the fact that the dominant and high frequency poles of the cascode are well

[8] From the stability point of view the cascade must be an inverting amplifier, therefore the minimum number of stages for a single ended configuration is three.

[9] The comprehensive selection of available frequency compensation techniques for multi-stage amplifiers can be found in [67].

separated what allows correct application of pole splitting techniques.

$$K_v(s) = -\frac{g_{m1}\, r_{ds2}}{(1+s/P_1)(1+s/P_2)} \quad \text{where} \quad P_1 = \frac{1}{C_L\, r_{ds2}},\ P_2 = \frac{g_{m2}}{C_1} \tag{A.3}$$

$$K_{v1}(s) = -2\,\frac{g_{m1}}{g_{m2}}\,\frac{(1+s/Z)}{(1+s/P_1)(1+s/P_2)} \quad \text{where} \quad Z = \frac{2}{C_L\, r_{ds2}},\ P_1 = \frac{1}{C_L\, r_{ds2}},\ P_2 = \frac{g_{m2}}{C_1} \tag{A.4}$$

From Eq. (A.3) it can be seen that the gain of the cascode is the product of the transconductance of the input device and the output impedance of the cascode transistor. As the bias of the input transistor sets its transconductance, g_{m1}, it is usually the result of optimizing the noise performance whilst remaining within the allowable power budget. Consequently, tuning the gain appropriately requires increasing r_{ds2} to the necessary level. This is usually done either by increasing the channel length or by lowering the bias current. Using a folded cascode configuration is a commonly used technique to achieve this by the latter means. As a result, the transconductance of the cascode transistor g_{m2} is usually much lower than the transconductance of the input device g_{m1}. Consequently, the low-frequency gain seen for the practical implementation of the cascode input stage (M_1 drain), responsible for the Miller effect, is higher than its desired value but still much lower than the gain of the cascade (see the comparison in Fig. A.8). Note that the gain of the first stage is limited at higher frequencies by the dominant low-frequency cascode pole, however its impact is limited by the zero located at twice its frequency.

The cascode amplifier gain plot exhibits two well-separated poles: one dominant at low-frequency whose position depends on the cascode load capacitance and output impedance; and a second at high-frequency, defined by the transconductance of the cascode transistor M_2 and the capacitance seen at the drain of the input transistor, M_1. Hence, the cascode behaves more like a single-stage amplifier and its frequency compensation is much easier than in the case of the cascade amplifier.

For applications requiring higher open-loop gain or for designs implemented in processes with lower intrinsic transistor gain, it is necessary to boost the load impedance by employing cascode current sources. To simplify of the analysis and attain more clarity in the expressions, one can assume that the load impedance is equal to the output impedance of the cascode amplifier, i.e. $r_L = g_{m2}\, r_{ds1}\, r_{ds2}$. See [69] or [29] for a good treatment of the analysis of the cascode output and cascode current mirror impedances. Solving Eqs. (A.2) and substituting r_L by $g_{m2}\, r_{ds1}\, r_{ds2}$ the expressions for the gain of the cascode and its first stage shown in (A.5) and (A.6) are obtained.

$$K_v(s) = -\frac{1}{2}\,\frac{g_{m1}\, g_{m2}\, r_{ds1}\, r_{ds2}}{(1+s/P_1)(1+s/P_2)} \quad \text{where} \quad P_1 = \frac{2}{C_L\, g_{m2}\, r_{ds1}\, r_{ds2}},\ P_2 = \frac{g_{m2}}{C_1} \tag{A.5}$$

$$K_{v1}(s) = -\frac{1}{2}\,\frac{g_{m1}\, r_{ds1}\,(1+s/Z)}{(1+s/P_1)(1+s/P_2)} \quad \text{where} \quad Z = \frac{1}{C_L\, r_{ds2}},\ P_1 = \frac{2}{C_L\, g_{m2}\, r_{ds1}\, r_{ds2}},\ P_2 = \frac{g_{m2}}{C_1} \tag{A.6}$$

Note that the gain is boosted by the higher value of the output impedance which also shifts the dominant pole towards lower frequencies whilst preserving the GBP. Although the gain seen at the drain of the input device (K_{v1}) is now comparable to that of the cascade, its bandwidth is severely limited in this case by the low-frequency pole defined by the cascode output impedance and load capacitance. The high-frequency zero defined by C_L and r_{ds2} also has an impact on the K_{v1} characteristic, limiting the effect of the low-frequency pole at higher frequencies. This effect gives it practically the same gain as that of the low gain cascode at higher frequencies.

The comparison of the gain of the first stage of the cascade and cascode amplifiers calculated for one hypothetical design is shown in Fig. A.8. Although it is clear that the worst Miller effect will be visible using the CSA built with the cascade preamplifier, it is less so as to whether a high or low gain cascode is optimal from this perspective. The next section details the comparative time-domain analyses for both structures configured for CSA operation (see Fig. A.9).

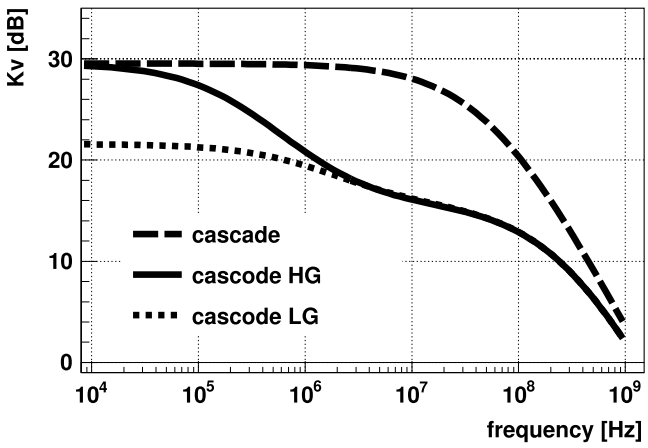

Fig. A.8. The gain of the first stage of the cascade ($r_L = r_{ds1}$), cascode loaded with cascode current source (high gain (HG) cascode, $r_L = g_{m2}\, r_{ds1}\, r_{ds2}$) and cascode loaded with single transistor current source (low gain (LG) cascode, $r_L = r_{ds2}$). For this calculation, the following transconductances and output impedance's were used: $gm_1 = 3\,\text{mS}$, $gm_2 = 0.5\,\text{mS}$, $r_{ds1} = 20\,\text{k}\Omega$, $r_{ds2} = 400\,\text{k}\Omega$, $C_1 = C_L = 300\,\text{fF}$.

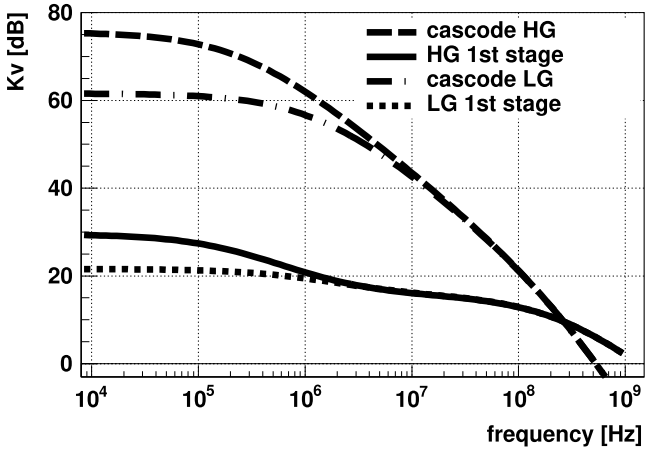

Fig. A.9. Comparison of the frequency characteristics of low gain (LG) and high gain (HG) cascode amplifiers calculated for $gm_1 = 3\,\text{mS}$, $gm_2 = 0.5\,\text{mS}$, $r_{ds1} = 20\,\text{k}\Omega$, $r_{ds2} = 400\,\text{k}\Omega$, $C_1 = C_L = 300\,\text{fF}$.

Appendix B. The impact of the Miller effect on preamplifier response

Although the analysis of the Miller effect in the cascade and cascode amplifiers in the frequency domain confirms the advantage of the cascode topology, quantitative evaluation should be done in the time domain for the circuits working in CSA configuration, especially for the comparison of the low and high gain cascode versions. The presented examples show the preamplifiers working with pure capacitive feedback only. This provides the simplicity of the calculations and clearer interpretation of the results. For the same reasons only one dominant pole in the frequency characteristics of the circuits analyzed is considered. The analysis of the preamplifier built with different types of feedback working in charge or transimpedance modes and its impact on the charge collection efficiency, input impedance, amongst other parameters, can be found in the literature (e.g. [29]).

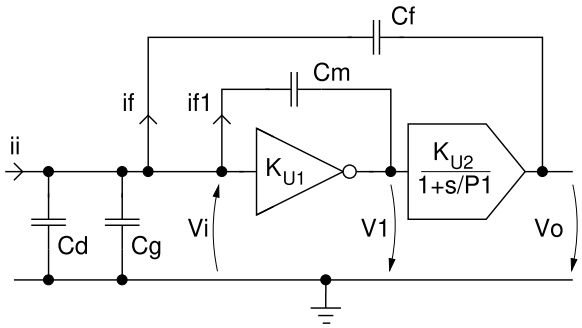

Fig. B.10. The equivalent schematic diagram of charge sensitive preamplifier build with cascade of common source amplifiers.

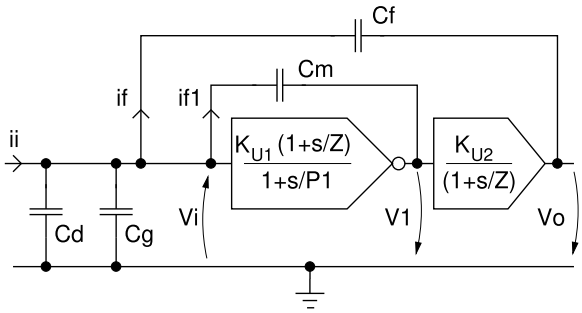

Fig. B.11. The equivalent schematic diagram of charge sensitive preamplifier built with a cascode for evaluation of the Miller effect on its response amplitude and timing.

B.1. The preamplifier built with cascade of common source amplifiers

The schematic of a generic charge sensitive preamplifier built with a cascade is shown in Fig. B.10. It consists of a wide-band input amplifier and a second stage with one dominant, low-frequency, pole providing frequency compensation of the amplifier operating in CSA configuration. When single-ended amplifiers are used, the second stage is also built with the cascade of two amplifiers to provide non-inverting operation. The circuit is evaluated using nodal analysis.

$$i_i = v_i\, s\,(C_d + C_g) + i_f + i_{f1} \tag{B.1a}$$

$$i_f = s\,C_f\,(v_i + V_o) \tag{B.1b}$$

$$i_{f1} = s\,C_m\,v_i\,(1 + K_{U1}) \tag{B.1c}$$

$$v_o = v_i\,\frac{K_{U1}\,K_{U2}}{1 + s/P_1} \tag{B.1d}$$

$$K_U = K_{U1}\,K_{U2} \tag{B.1e}$$

Solving the set of Eqs. (B.1) for v_o we obtain the expression (B.2) in the operator domain.

$$v_o = i_i\,\frac{K_U}{s\,((C'_{in} + K_U\,C_f) + s\,C'_{in}/P_1)} \quad \text{where} \quad C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \tag{B.2}$$

Assuming that the preamplifier is responding to a Dirac delta charge pulse, the inverse Laplace transform yields Eq. (B.3), which describes the preamplifier response in the time domain.

$$v_o(t) = A\left(1 - e^{-\frac{t}{\tau_p}}\right) \quad \text{where} \quad A = \frac{1}{C_f + C'_{in}/K_U} \approx \frac{1}{C_f} \quad \tau_p = \frac{C'_{in}}{P_1\,(C'_{in} + K_U\,C_f)} \approx \frac{C'_{in}}{GBP\;C_f} \quad C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \tag{B.3}$$

Assuming sufficient open-loop gain, i.e. $C'_{in}/K_U \ll C_f$, the preamplifier response to the Dirac delta pulse will be a voltage step of amplitude equal to $1/C_f$. The rising edge slew rate is characterized by the time constant proportional to the total input capacitance C'_{in}. This corresponds to the Miller capacitance, C_m multiplied by K_{U1}, and is inversely proportional to the GBP of the amplifier stage and feedback capacitance C_f.

B.2. The preamplifier built with a cascode

The evaluation of the Miller effect in a cascode can be achieved by analyzing the equivalent circuit shown in Fig. B.11. The first stage of the cascode is represented by the block with one dominant low-frequency pole, P_1, and one high frequency zero, Z, and shown mathematically in expressions (A.4) and (A.6).

In order to correctly describe the overall frequency characteristics of the cascode given by expressions (A.3) and (A.5), the second stage is represented by a single pole circuit introduced to cancel the zero of the first stage. As in the previous case, the non-dominant, high-frequency pole P_2 is omitted from the analysis.

The circuit can be evaluated using nodal analysis.

$$i_i = v_i\, s\,(C_d + C_g) + i_f + i_{f1} \tag{B.4a}$$

$$i_f = s\,C_f\,(v_i + v_o) \tag{B.4b}$$

$$i_{f1} = s\,C_m\,(v_i + v_1) \tag{B.4c}$$

$$v_1 = v_i\,\frac{K_{U1}(1 + s/Z)}{1 + s/P_1} \tag{B.4d}$$

$$v_o = v_1\,\frac{K_{U2}}{1 + s/Z} \tag{B.4e}$$

$$K = K_{U1}\,K_{U2} \tag{B.4f}$$

Solving the set of Eqs. (B.4) for v_o we obtain the expression shown in (B.5) in the operator domain.

$$v_o = i_i\,\frac{K_U}{s\,((C'_{in} + K_U\,C_f) + s\,(C_{in}/P_1 + C_m\,K_{U1}/Z))} \quad \text{where} \quad C_{in} = C_d + C_g + C_f + C_m \quad C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \tag{B.5}$$

Assuming a Dirac delta charge pulse at the preamplifier input, the inverse Laplace transform yields its time-domain response as is shown in Eq. (B.6).

$$v_o(t) = A\left(1 - e^{-\frac{t}{\tau_p}}\right) \quad \text{where} \quad A = \frac{1}{C_f + C'_{in}/K_U} \approx \frac{1}{C_f} \quad \tau_p = \frac{C''_{in}}{P_1\,(C'_{in} + K_U\,C_f)} \approx \frac{C''_{in}}{GBP\;C_f} \quad C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \quad C''_{in} = C_d + C_g + C_f + (1 + K_{U1}\,P_1/Z)\,C_m \tag{B.6}$$

One can notice that the Miller effect for the cascode is mitigated with the ratio of high-frequency zero and the dominant pole of the cascode amplifier.

Calculating $K_{U1}\,P_1/Z$ for both low and high gain cascodes using the respective expressions for K_{U1} (equal to $K_{v1}(0)$ here), P_1, and Z from formulas (A.4) and (A.6), the same equivalent input capacitance is found, see (B.7).

$$C''_{in} = C_d + C_g + C_f + (1 + g_{m1}/g_{m2})\,C_m \tag{B.7}$$

This shows that both versions are the same from this point of view and the effective gain giving rise to the Miller effect for the cascodes working in CSA configuration is equal to g_{m1}/g_{m2}. Thus from the perspective of the charge collection efficiency and input impedance minimization, the high gain cascode is preferable.

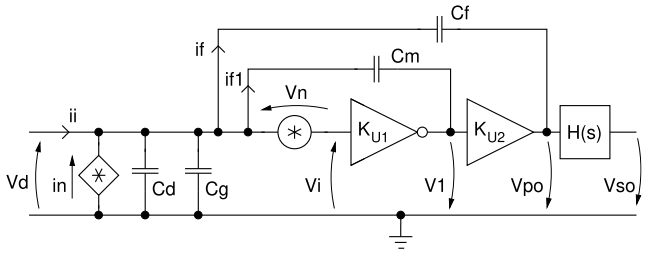

Fig. C.12. The equivalent schematic diagram of the front-end channel with two-stage preamplifier for evaluation of the noise performance with focus on the Miller effect.

B.3. Understanding the Miller effect in the CSA

It is important to understand that the mechanism responsible for the Miller effect resulting in the degradation of the CSA speed is not the signal bandwidth limit imposed by the *RC* of the source resistance and capacitance at the amplifier input, as shown in the typical example.

Although the impedance of the silicon sensor is high enough for the equivalent circuit to be represented by an ideal current source with a parallel parasitic capacitance, the current signal delivered by the detector is not affected by the sensor capacitance nor by amplifier input capacitance. Instead, it is the preamplifier response degrading due to its limited GBP and the increase in the overall input capacitance, amplified by the Miller effect, as can be seen in formulas (B.3) and (B.6).

Whilst increasing C_f can recover good timing performance in cases where poor circuit design results in the input stage GBP being too low, this must be avoided as it requires increasing the power consumed in the shaper stage to not to degrade the overall noise performance.

It can be seen through examination of expressions (B.3) and (B.6) that the rising edge of the preamplifier response is limited in proportion to the time-constant imposed by the total input capacitance, C'_{in}=(B.2) or C''_{in}=(B.7), and inversely proportional to the GBP, and the feedback capacitance, C_f. Thus for a CSA implemented with a purely capacitive feedback loop, the input impedance can be considered as $1/(\mathrm{GBP}\times C_f)$

Appendix C. Noise analysis of the front-end amplifier

To simplify the analysis, all noise sources are considered to be uncorrelated and have white spectra. Fig. C.12 shows the simplified schematic diagram of a CSA amplifier connected to a CR-RC shaper.

The noise sources i_n and v_n represent the equivalent parallel and series noise sources of the front-end amplifier. In this particular analysis, the impact of the Miller effect on the noise performance of the generic CSA is also extracted.

For this, we assume that the preamplifier is built with a wide-band input stage and the bandwidth limitation is imposed by the shaper stage only. Hence, the worst-case scenario for the Miller effect is considered.

The response of the preamplifier-shaper chain, as well as the output noise, can be calculated by solving the set of Eqs. (C.1)a through (C.1)g.

$$v_n = v_d - v_i \tag{C.1a}$$

$$i_f = s\,C_f\,(v_d + v_{po}) \tag{C.1b}$$

$$i_{f1} = s\,C_m\,(v_d + v_1) \tag{C.1c}$$

$$s\,(C_d + C_g)\,v_d + i_f + i_{f1} = i_i + i_n \tag{C.1d}$$

$$v_1 = v_i\,K_{U1} \tag{C.1e}$$

$$v_{po} = v_1\,K_{U2} \tag{C.1f}$$

$$K_U = K_{U1}\,K_{U2} \tag{C.1g}$$

To proceed with this, its response to a delta Dirac input current pulse is considered, and v_{po} is calculated, having disabled both noise sources by setting them to zero: i_n=0 and v_n=0.

$$v_{po} = i_i \frac{1}{s\,(C_f + C'_{in}/K_U)} \quad \text{where}$$
$$C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \tag{C.2}$$

The transfer function of the $CR - RC^n$ shaper is given by Eq. (C.3).

$$H(s) = \frac{s\,\tau_s}{(1 + s\,\tau_s)^{n+1}} \tag{C.3}$$

The Laplace transform of the preamplifier response in the operator domain multiplied by the shaper transfer function gives the response of the full chain to the Dirac delta pulse applied at the input.

$$v_{so}(t) = \frac{Q_i}{C_f + C'_{in}/K_U}\,\frac{1}{\Gamma(n+1)}\left(\frac{t}{\tau_s}\right)^n e^{-\frac{t}{\tau_s}} \tag{C.4}$$

where $\Gamma(n+1)$ is the Gamma function.

The expression (C.4) has a maximum described by Eq. (C.5).

$$v_{soMAX} = \frac{Q_i}{C_f + C'_{in}/K_U}\,\frac{1}{\Gamma(n+1)}\left(\frac{n}{e}\right)^n \quad \text{for} \quad t_{peak} = n\,\tau_s \tag{C.5}$$

To calculate the transmittance of the preamplifier for the series noise source v_n the parallel noise source is disabled: i_n=0, and the input signal set to zero: i_i=0. Solving Eqs. (C.1) yields Eq. (C.6).

$$v_{po} = v_n \frac{C_{in}}{C_f + C'_{in}/K_U} \quad \text{where}$$
$$C_{in} = C_d + C_g + C_f + C_m \quad \text{and}$$
$$C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \tag{C.6}$$

Transforming Eq. (C.6) into the frequency domain, applying the filter transmittance and integrating over the whole frequency range we obtain the sigma noise at the output of the full chain. This result is given in Eq. (C.7).

$$\sigma^2_{noS} = \int_0^\infty \frac{\overline{v_n^2}}{\Delta f}\,\frac{C_{in}^2\,|H(j\omega)|^2}{(C_f + C'_{in}/K_U)^2}\,df \tag{C.7}$$

Dividing the output noise by the signal amplitude extracted from (C.5), the series noise contribution to the equivalent noise charge shown in Eq. (C.8) is obtained.

$$ENC_S = \frac{\sigma_{noS}}{v_{soMAX}} = F_V\,\frac{C_{in}}{\sqrt{t_{peak}}}\,\overline{v_n}$$
$$\text{where} \quad F_V = \frac{n}{\sqrt{2}}\left(\frac{e}{2n}\right)^n \sqrt{\Gamma(2n-1)} \tag{C.8}$$

Calculating the transmittance of the preamplifier for the parallel noise source i_n proceeds by a similar methods, by disabling the series noise source: v_n=0, and input signal: i_i=0, and subsequently solving Eqs. (C.1) for v_{po}. The resulting expression is given in (C.9).

$$v_{po} = i_n \frac{1}{s\,(C_f + C'_{in}/K_U)} \quad \text{where}$$
$$C'_{in} = C_d + C_g + C_f + (1 + K_{U1})\,C_m \tag{C.9}$$

Transforming Eq. (C.9) into the frequency domain, applying the filter transmittance, and integrating over the whole frequency range, the sigma noise at the output of the front-end, shown in Eq. (C.10), is obtained.

$$\sigma^2_{noP} = \int_0^\infty \frac{\overline{i_n^2}}{\Delta f}\,\frac{|H(j\omega)|^2}{(C_f + C'_{in}/K_U)^2\,\omega^2}\,df \tag{C.10}$$

Dividing the output noise by the signal amplitude described by (C.5) the parallel noise contribution to the ENC shown in (C.11) is finally obtained.

$$ENC_P = \frac{\sigma_{noP}}{v_{soMAX}} = F_I\,\sqrt{t_{peak}}\;\overline{i_n}$$
$$\text{where} \quad F_I = \frac{1}{\sqrt{2}}\left(\frac{e}{2n}\right)^n \sqrt{\Gamma(2n)} \tag{C.11}$$

Obviously the total equivalent noise charge will be the quadrature sum of the partial contributions, as shown in Eq. (C.12).

$$ENC^2 = ENC_S^2 + ENC_P^2 \tag{C.12}$$

Since the Miller effect impacts both the output noise and the gain of the preamplifier by the same factor, the ENC is unaffected.

The whole noise analysis is done assuming that the preamplifier does not contribute to the signal shaping, which is an ideal case for the processing chain. In reality, especially in the case of fast and low-power electronics, the preamplifiers work with limited bandwidth, and quite often the time constants of the shaper stages, which are also optimized for low power, are not equalized. Although this does not change the general noise model for the CSA, its effect has to be taken into account in order to match the measurements from the silicon to the predicted numbers.

In a well-designed cascode amplifier, the dominant noise source is the channel thermal noise of the input device. In the original Van der Ziel noise model, it is represented by the current noise generator connected between drain and source of the transistor [70]. Considering that it is in fact a series noise source, it is quite often represented by the equivalent voltage noise generator connected to the gate of the transistor with the spectral density defined by Eq. (C.13),

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{4\,k\,T\,\gamma\,n}{g_m} \tag{C.13}$$

in which: g_m is the transconductance of the transistor; T is absolute temperature; k is the Boltzmann constant; n is a slope factor [16]; and γ is a bias dependent parameter taking values from 1/2 to 2/3 for an ideal transistor operating from weak to strong inversion. Having this form, the spectral density can be directly used for the calculation of its contribution to the ENC by replacing $\overline{v_n}$ in the formula (C.8).

$$ENC_S = \sqrt{\frac{4\,k\,T\,\gamma\,n}{g_m}}\,F_V\,\frac{C_{in}}{\sqrt{t_{peak}}} \tag{C.14}$$

For the front-end amplifiers using BJT devices at the input, the dominant noise is the shot noise of the collector current of the input transistor with the noise spectra density defined by Eq. (C.15):

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{2\,k\,T}{g_m} \tag{C.15}$$

and with the following contribution to the ENC of the front-end given by Eq. (C.16).

$$ENC_S = \sqrt{\frac{2\,k\,T}{g_m}}\,F_V\,\frac{C_{in}}{\sqrt{t_{peak}}} \tag{C.16}$$

The detailed noise analysis of front-end amplifier built with bipolar transistors can be found in [22].

Besides the thermal or shot noise of the input transistor, one has to take into account the parallel noise sources related to the feedback circuit and the leakage current of the sensor. For example, the feedback circuit using a simple resistor is contributing with the noise spectra density given in Eq. (C.17).

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4\,k\,T}{R_f} \tag{C.17}$$

The corresponding ENC contribution is defined by Eq. (C.18).

$$ENC_P = \sqrt{\frac{4\,k\,T}{R_f}}\,F_I\,\sqrt{t_{peak}} \tag{C.18}$$

The detector leakage current will contribute with the spectral density given by Eq. (C.19).

$$\frac{\overline{i_n^2}}{\Delta f} = 2\,q\,I_{leak} \tag{C.19}$$

where q is the elementary charge. The ENC contribution from the leakage current is shown in Eq. (C.20).

$$ENC_P = \sqrt{2\,q\,I_{leak}}\,F_I\,\sqrt{t_{peak}} \tag{C.20}$$

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