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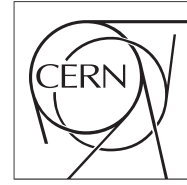
Conference Report

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Software Tools for Hybrid Quality Control for the CMS Phase-2 Outer Tracker Upgrade

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Abstract

ABSTRACT: Fifty thousand hybrid circuits of five different types will be manufactured for the Phase-2 Upgrade of the CMS Outer Tracker. These circuits must undergo a strict quality control process, composed of functional testing and visual inspection, before they can be assembled into modules. The hybrids will be functionally tested first at the manufacturing site. Afterwards, they will be visually inspected and functionally tested again at CERN or at collaborating institutes. Results from these processes will be stored in the CMS production database. This paper presents the software tools developed to carry out these tasks.

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Software Tools for Hybrid Quality Control for the CMS Outer Tracker Phase-2 Upgrade

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Contents

1. Introduction

The CMS Phase-2 Outer Tracker Upgrade is based on two module types (**Figure 1**): a module with two strip sensors, know as the 2 Strip Module (2S module), and a module with a strip sensor and a macro-pixel sensor, known as the Pixel Strip Module (PS module) [1]. These modules are formed by five different hybrid types: 2S Front-End Hybrid (2S-FEH), 2S Service Hybrid (2S-SEH), PS Front-End Hybrid (PS-FEH), PS Readout Hybrid (PS-ROH) and PS Power Hybrid (PS-POH).
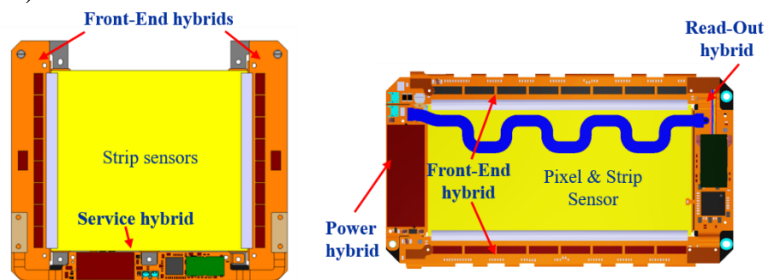

Figure 1: The 2S module (left) and the PS module (right).

These hybrids are built using flexible circuits glued to carbon fibre stiffeners. In some cases the circuits have to be folded and the ASICs used are bump-bonded. The manufacturing of the hybrids is therefore very complex and faults might happen at any step of the process. In addition, when the tracker modules are assembled the hybrids are glued, making repairs impossible.

In total, almost 50000 hybrids [2] will be manufactured for the Phase-2 Upgrade. They will undergo a thorough quality control process, consisting of visual inspection and functional testing. **Table 1** provides an overview of the hybrids that will be quality controlled at the different sites.

Quality control site	Visual Inspection	Functional Test
Manufacturer	-	100% of the hybrids
CERN	66% of the hybrids	100% of the 2S hybrids, 33% of the PS hybrids.
INFN Catania	-	66% of PS-FEH
INFN Genova	-	66% of PS-POH and PS-ROH
Wigner RCP	33% of the hybrids	-

Table 1: Distribution of hybrids to be processed at each location.

Since the hybrids will be inspected and tested at multiple sites by different operators, several software tools were developed for these tasks. Their goal is to simplify and unify the procedures. The next sections will provide an overview of these tools.

2. Visual Inspection

The visual inspection of the hybrids is a manual process where several key points are checked, such as component placement and soldering correctness, alignment of hybrid layers and correct gluing, cleanliness and flatness of the circuit and quality of the wire-bond pads. Specific measurements and wire-bonding tests are also performed on a sampling basis.

A web application was developed to gather the visual inspection data, to generate reports and to store all the results in a central database. This application uses Python and Flask for the back-end server, and standard JavaScript and HTML for the front-end pages. The application allows for old reports to be edited to update the hybrid status, and stores a history of all the hybrid visual inspections through its life. This allows monitoring a hybrid after different events, such as transport or repairs. At the end of a visual inspection, the hybrid is either accepted, rejected or flagged for repair.

3. Functional Testing

3.1 Tested features and test system

The functional test of the hybrids checks for correct electrical connectivity and performance. This means testing the digital input and output lines of all ASICs and the analog inputs (sensor channels) of the sensor readout ASICs. For the hybrids with optical readout (PS-ROH and 2S-SEH), the optical links are also tested. The hybrids tasked with power delivery (PS-POH and 2S-SEH) are characterized (efficiency, performance at different loads and input voltages, etc.).

To be able to perform these tests, a high throughput modular test system was required. The designed system is based around a multiplexing crate in which different plug-in test cards can be plugged. There is one test card design to test each hybrid type. A single system can be used to test all the hybrid types, which makes it quite versatile.

The test system consists of a Linux machine connected via Ethernet to an FPGA-based readout board, which is in turn connected to the multiplexing crate and controls the multiplexer. It also interfaces with the ASICs present in the hybrids. The computer is connected directly to the crate via USB, used to identify and control the test card. In **Figure 2**, the structure of the system is shown, together with the necessary software and firmware components for its operation.

The developments needed for the running of the system can be divided into two groups. The first group contains the developments to test a specific hybrid type: software for test card control, firmware for the FPGA and test procedures. The second group contains the software needed to run the full system for all hybrid types. Both are described in the next subsections.

3.2 Hybrid-specific software and firmware

For the control of the test card features a USB device is used. This device is present for every test card design and allows the identification of the selected card ID and type as well as the control of the card. To interface with this USB device a custom driver has been developed for each test card type. In addition, two of the test card designs include a microcontroller (the PS-POH and 2S-SEH test cards). It controls some of the test card features and communicates with the computer via the USB device described above. For each of these test cards, custom firmwares were developed.
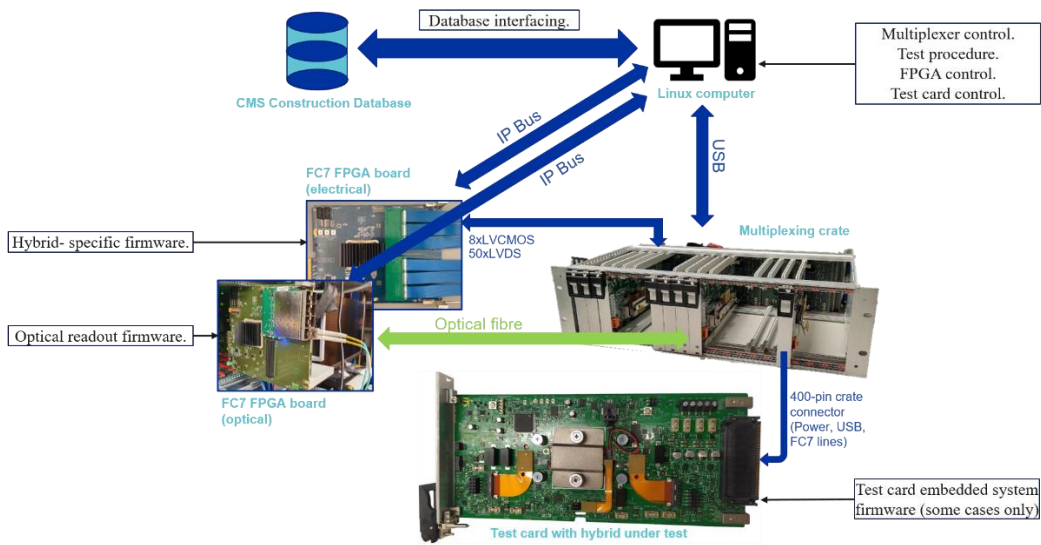
Figure 2: Structure of the test system.

The readout board used for the system is the FC7, a μTCA-compatible AMC based on the Kintex 7 FPGA [3]. The firmware used in the FC7 is the μDTC (μ Data Trigger Control). This project is the base for testing all CMS Inner and Outer Tracker Phase-2 objects: ASICs, hybrids and modules [4]. It provides support for electrical and optical readout of the hybrids and for control of the ASICs on the hybrids via fast and slow control. It also controls the signals to configure the multiplexing crate. A very simplified diagram of the structure of the μDTC firmware can be seen in **Figure 3**. This firmware has to be built specifically for every hybrid type, since not all the hybrids use the same ASICs. For the complete test system, six different images are used: two for electrical readout (PS and 2S FEHs), two for optical readout (PS-ROH and 2S-SEH), one for "high voltage" mode enabling (to test the PS-POH) and one with only the multiplexing control.
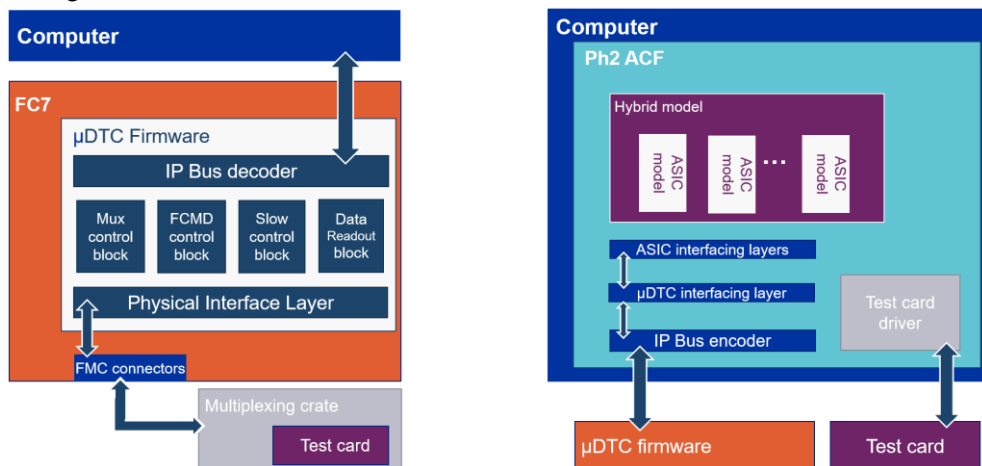

Figure 3: (Left) simplified block diagram of the μDTC firmware and (right) simplified block diagram of Ph2 ACF.

The next development category is for test procedures. These are developed using the Phase2 Acquisition and Control Framework (Ph2 ACF) [5]. This framework, developed in C++, provides the necessary classes to interface with the μDTC firmware, wrapping the firmware calls and

handshakes into functions. The framework allows representing the structure of ASICs inside a hybrid, and has classes representing each object (ASIC, hybrid, etc.) and the default configurations for each hybrid type. The test procedure uses all these layers and the test card driver to test the hybrid features. As in the case of the µDTC firmware, there is one test procedure per hybrid type. The structure of the framework is shown in **Figure 3**.

Figure 4 shows the flow diagram of a test procedure. This is done for all the hybrids before hybrid-specific tests are run. These first steps verify the basic functionality of the hybrid in terms of powering and the basic functionality of the ASICs.
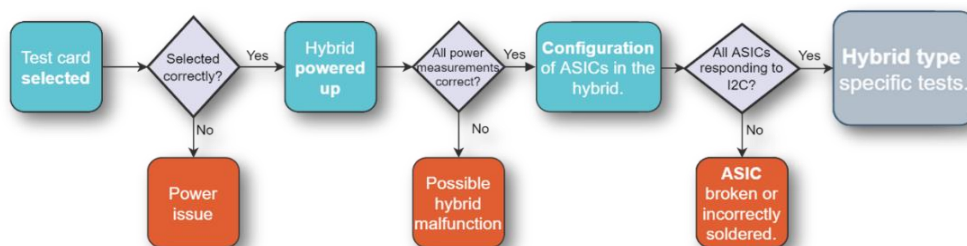

Figure 4: Flow diagram of a test generalized to all hybrid types.

After these steps are successfully performed, the procedure continues to the tests specific to the hybrid type. One example of these tests is the test performed on the analog channels of the Front-End Hybrids. **Figure 5** shows the basic concept of the open and short finding algorithms.
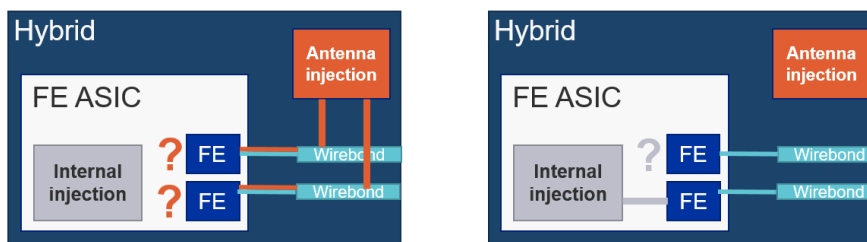

Figure 5: Analog channels opens (left) and shorts (right) finding procedures.

To find opens, a test feature designed in the hybrid allows to inject pulses in the traces that go to the analog channels in the FE ASICs. To find shorts, the internal charge injection feature in the ASIC is used to inject charge in a few channels only. After injection, the FE ASIC is read out to find whether the expected channels recorded hits.

3.3 Use of the full test system

To allow for the use of the test system by non-experts for all the different hybrid types a graphical tool was required. The goal is to reduce to the minimum the complexity of testing five different objects, making the system as transparent as possible.

The tool developed is the CrateTester, which acts as the top layer of the software and is the manager of the testing at a global level. This graphical tool takes care of mapping test card and hybrid position in the crates and of controlling the power supply and multiplexing crate. It can manage multiple crates in parallel and it handles all the different hybrid types: selecting the appropriate test procedure and firmware to run the test, processing the results and generating the hybrid status. At the end of all the tests it stores the test results in the CMS Construction Database. **Figure 6** shows the steps that are taken to run the tests.
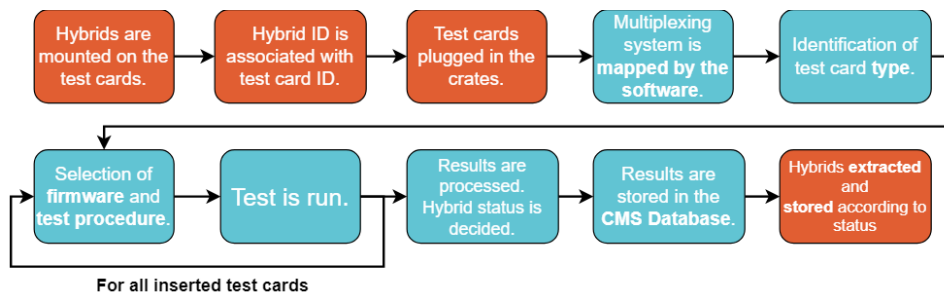
Figure 6: Workflow of a test run using the CrateTester GUI. In orange the steps taken by the operator, in blue the steps that are automated.

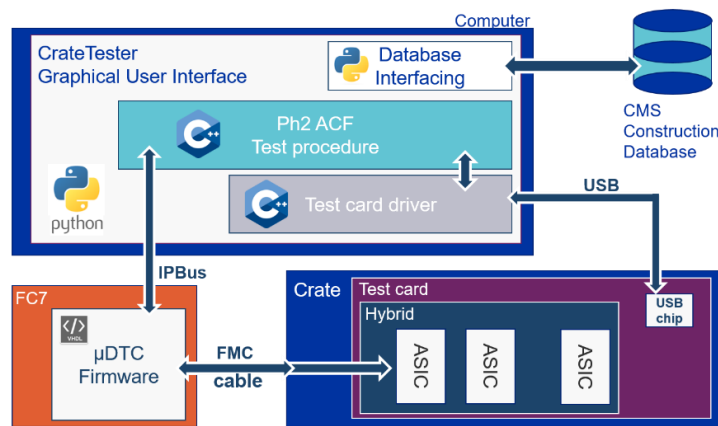**Figure 7** shows how all the software and firmware components needed to operate the test system are related.

Figure 7: Simplified block diagram of the test system software and firmware.

4. Conclusions

Both the visual inspection application and the test system were used extensively during the hybrids prototyping phase. During this time, the VI application design was iterated with feedback from the visual inspection experts. The test system was used to test all the prototypes, and it was verified to work at cold and during extended periods of time, an exercise that was used to further develop and debug the testing software and firmware. **Table 2** shows the number of hybrids that were quality controlled during the prototyping phase.

In this phase all the steps were happening in parallel: visual inspection and testing of the hybrid prototypes, debugging of the test system hardware and development and debugging of test system software and firmware.

The current status is that the visual inspection application is finalized, the test card drivers and firmwares are finalized and the μDTC firmwares and Ph2 ACF test procedures are being finalized. The integration of all different test procedures in the CrateTester software is also close to completion.

Hybrid type	2S-FEH	2S-SEH	PS-FEH	PS-ROH	PS-POH
No. of quality controlled hybrids	221	70	230	62	32

Table 2: Quality control during the prototyping phase.

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