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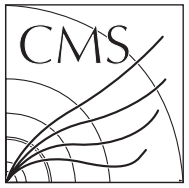

The Compact Muon Solenoid Experiment

Conference Report

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Electronics for the far-forward CMS muon detector upgrade, ME0

Joseph Carlson for the CMS Collaboration

Abstract

With the High Luminosity upgrade of the Large Hadron Collider (LHC) we expect increased instantaneous luminosities up to $5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$, or five times more than the original values. In order to maintain performance of the Compact Muon Solenoid (CMS) experiment under these conditions, ME0 is one of three new muon sub-detectors being added, along with GE1/1 and GE2/1, which use the triple Gas Electron Multiplier (GEM) technology. ME0 is designed to cover the forward region of $2.0 < |\eta| < 2.8$, thus improving muon reconstruction at high background rates by supplementing other overlapping muon subsystems up to $|\eta| = 2.4$, while also extending the acceptance for the first time to $|\eta| = 2.8$. The readout electronics for ME0 must be designed to accommodate high data rates and be sufficiently radiation hard to operate close to the beamline. The Optohybrid (OH) board for ME0, which reads out data from the front-end VFAT3b ASICs, has therefore been designed to operate without an FPGA (unlike GE1/1 and GE2/1) to ensure radiation hardness. The ME0 OH uses the radiation-hard CERN-designed lpGBT ASIC and VTRx+ optical transceiver module for high bandwidth optical links up to 10.24 Gb/s. The backend system is based on the ATCA standard. The design and development status of the readout electronics for ME0 is presented, along with recent results from integration tests performed using the first prototypes.

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Electronics for the far-forward CMS muon detector upgrade, ME0

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Abstract: With the High Luminosity upgrade of the Large Hadron Collider (LHC) we expect increased instantaneous luminosities up to $5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$, or five times more than the original values. In order to maintain performance of the Compact Muon Solenoid (CMS) experiment under these conditions, ME0 is one of three new muon sub-detectors being added, along with GE1/1 and GE2/1, which use the triple Gas Electron Multiplier (GEM) technology. ME0 is designed to cover the forward region of $2.0 < |\eta| < 2.8$, thus improving muon reconstruction at high background rates by supplementing other overlapping muon subsystems up to $|\eta| = 2.4$, while also extending the acceptance for the first time to $|\eta| = 2.8$. The readout electronics for ME0 must be designed to accommodate high data rates and be sufficiently radiation hard to operate close to the beamline. The Optohybrid (OH) board for ME0, which reads out data from the front-end VFAT3b ASICs, has therefore been designed to operate without an FPGA (unlike GE1/1 and GE2/1) to ensure radiation hardness. The ME0 OH uses the radiation-hard CERN-designed lpGBT ASIC and VTRx+ optical transceiver module for high bandwidth optical links up to 10.24 Gb/s. The backend system is based on the ATCA standard. The design and development status of the readout electronics for ME0 is presented, along with recent results from integration tests performed using the first prototypes.

Contents

1 Introduction

ME0 is a new muon endcap detector, to be installed in CMS during the Phase-2 upgrade for the High Luminosity LHC (HL-LHC) [1]. ME0 is based on GEM detector technology [2], also used for GE1/1 and GE2/1, and covers the far forward region of $2.0 < |\eta| < 2.8$. In collaboration with the detectors GE1/1 and GE2/1, ME0 will help to improve muon reconstruction by supplementing other muon subsystems until $|\eta| = 2.4$, and also extend the acceptance region to $|\eta| = 2.8$. The ME0 detector system will consist of 6-layer triple GEM stacks arranged in each endcap in a wide planar ring with inner radius ≈ 0.6 m and outer radius ≈ 1.5 m, centered on beamline. Each endcap holds 18 stacks in a ring, making 32 6-layer stacks in total for CMS. Each ME0 chamber covers in the azimuthal direction, $\Delta\varphi = 20°$, and in the polar direction $\Delta\eta = 0.8$. This $\Delta\eta$ is split into 8 partitions in η, and further divided into 384 readout strips.

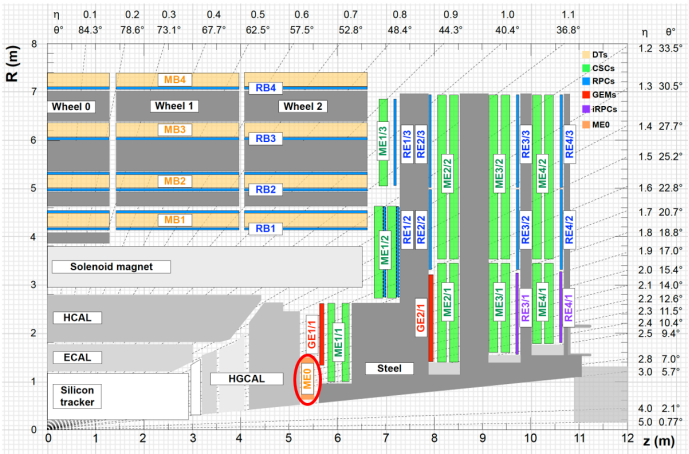

Figure 1: Quadrant of the CMS experiment highlighting ME0 ($2.0 < |\eta| < 2.8$). [2]

2 ME0 Electronics Overview

Being so close to the beamline means ME0 requires the use of only radiation-tolerant electronics. Also, due to the high luminosity, ME0 is required to operate at high data rates. The readout electronics (Fig. 2) is connected to the electrodes of the GEM chamber through the readout board. The VFAT is mounted on the GEM Electronics Board (GEB) and is connected to the readout board through a flex PCB connector. The GEB distributes power to all boards mounted on it, provided by the bPOL12V DC-DC converters. The GEB also hosts the Optohyrbid (OH), which further reads out the data from the VFATs, and converts the electrical signals to an optical signal, driven by the VTRx+, and finally sends this to the back-end ATCA card.

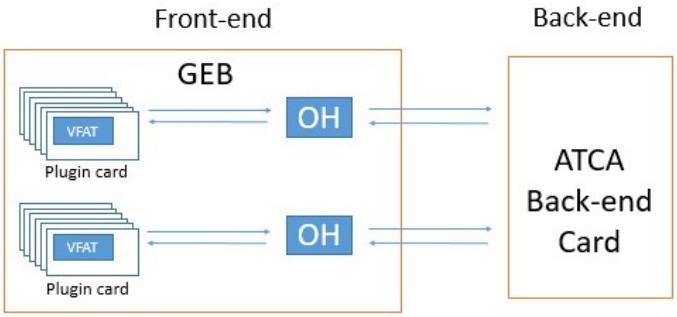

Figure 2: Block diagram for readout electronics of ME0.

The GEB (Fig. 3), designed by Peking University (PKU), distributes power and provides the interface for all front-end electronics on ME0. This board is radiation-tolerant and magnetic-tolerant by design. The GEB is split into two parts per layer, narrow and wide. Each GEB, narrow and wide, hosts 3 bPOL DC-DC converters, 12 VFATs, and 2 OHs. The GEB is fixed to the readout board. The GEB also provides current and temperature monitoring of the DC-DC converters, read out through the OH.

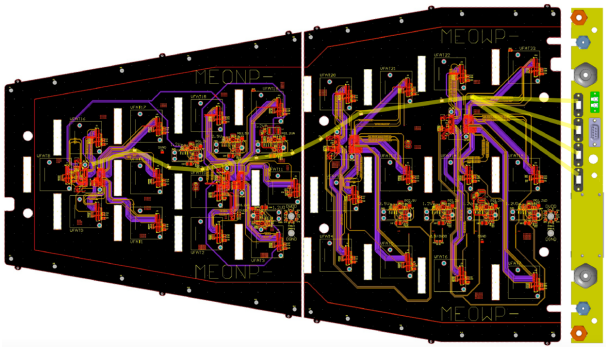

Figure 3: PCB layout of ME0 GEB, with fiber route in yellow.

The bPOL12V is a radiation-tolerant and magnetic-tolerant DC-DC converter ASIC, designed by CERN . The carrier board for bPOL12V has been designed for ME0 by CERN, based off the carrier board for the previous FEAST DC-DC converter which is pin-for-pin compatible with the

bPOL12V. 3 bPOLs provide voltages 1.2V (digital), 1.2V (analog), and 2.5V to the GEB and mounted electronics.

The VFAT3b (Fig. 4), designed by INFN Bari and CERN, is a radiation-tolerant and magnetic-tolerant front-end chip which reads out the strips on ME0 (also used in GE1/1 and GE2/1). One chip takes in the analog signals (charge) from 128 strips, and converts this to a digital signal, sent to the OH as tracking and trigger data. The VFAT3b has a charge sensitive preamplifier and shaper, followed by a constant fraction discriminator to reduce the background on each channel. The ASIC is packaged and mounted on a "plug-in card" with a protection circuit on the inputs.

The OH (Fig. 4), designed by UCLA, is a radiation-tolerant and magnetic-tolerant board which provides the readout interface for six VFATs. Each OH has two low power Gigabit Transceiver (lpGBT) ASICs (by CERN). The OH also has a connector for a VTRx+ transceiver to be mounted to the board, which provides the optical interface with the backend. The OH receives and transmits data to the VFAT over electrical links as 320 Mbps. The optical downlink, received by the OH is at 2.56 Gbps, and the uplink data from the OH to the back-end is at 10.24 Gbps. The ME0 OH does not use an FPGA in order to ensure radiation tolerance. Instead, all data compression and triggering is done in the back-end.

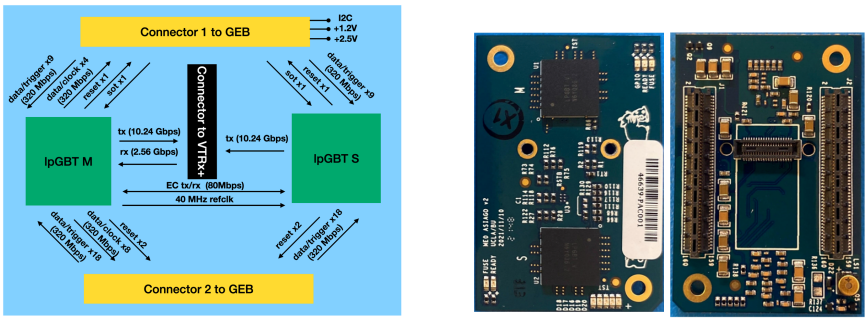

Figure 4: Block diagram for OH (left). Photo of OH top and bottom (right)

The ATCA-based back-end system will be used for all ME0, GE1/1, GE2/1, and Cathode Strip Chamber (CSC) detectors. The ATCA card is far from the front-end and does not require radiation tolerance. The back-end card will use an FPGA for triggering and online computation, and uses QSFP transceivers to interface with VTRx+. Each ATCA card will interface with two ME0 stacks, requiring 18 cards in total. The card supports high DAQ data rate of 700 Gb/s, accounting for all raw trigger hits from OH.

3 Electronics Testing

Pre-production boards have been produced and tested for all ME0 electronics. For the back-end ATCA card, initial testing with front-end electronics has been done, and more boards are being produced for use at various teststands.

For the GEB, both narrow and wide prototypes have been produced and distributed to various test stands. The final version will be made with halogen-free PCB, will optimize the fiber routing for the OHs, and will optimize the powering scheme. For the VFAT3b, all wafers have been produced for ME0, packaging expected in 2022.

For the OH, pre-production boards have been produced. All optical and electrical links are shown to be reliable, with a bit error ratio $< 10^{-12}$. For the full production run of ME0 OHs, there will be a tester board, QUESO (Fig. 5) by UCLA, which will test all inputs and outputs of all the OHs. QUESO stands for the QUalification of Electrical Signals and Optics. A pseudo-random bit sequence (PRBS) is generated in the back-end, sent to the OH, and the looped back through FPGAs (working in lieu of the VFATs), and sent through the uplink, finally being verified in the back-end. The PRBS has a unique bitmask applied on each electrical link to differentiate between links. The prototype of this board has been produced and is undergoing testing.

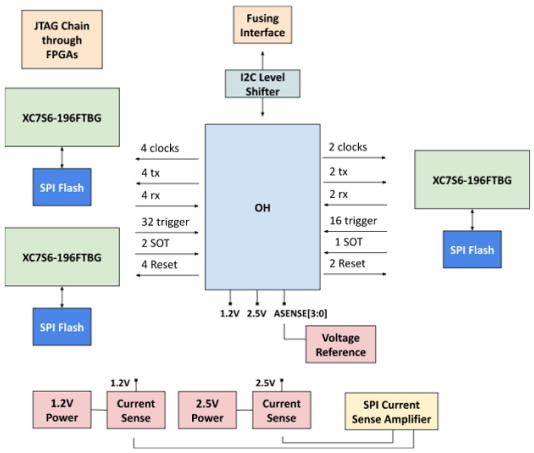

Figure 5: Block diagram for QUESO tester board.

4 Latest Status and Results from ME0 Integration

A multi-layer stack for ME0 (Fig. 6) is being integrated at CERN currently. The stack is using all the latest ME0 electronics available, and is the first test with using multiple layers of ME0 simultaneously. These layers are also connected to the full GEM chamber, allowing testing of the full ME0 system. This testing will be important for firmware and software development. The stack is currently composed of two layers, each layer being only half populated with electronics (due to availability), with more layers to be added in the future.

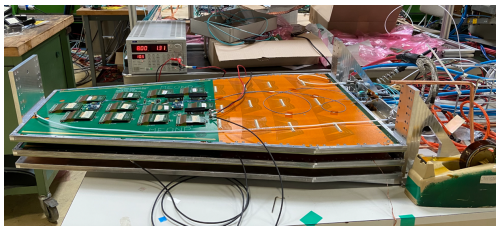

Figure 6: Picture of ME0 stack at CERN.

Equivalent noise charge (ENC) measurements have been taken for the data links of the VFATs using S-Curves (Fig. 7). The VFAT generates a calibration pulse of various magnitudes, and injects this into the channels, which are then read out through the ME0 electronics. The ENC is measured

from the width of the turn-on band near the threshold. The ENC was measured for all 128 channels on all 12 VFATs of one ME0 layer (Fig. 7). The average ENC is shown to be lower than 0.5 fC, indicating acceptable performance of the system.

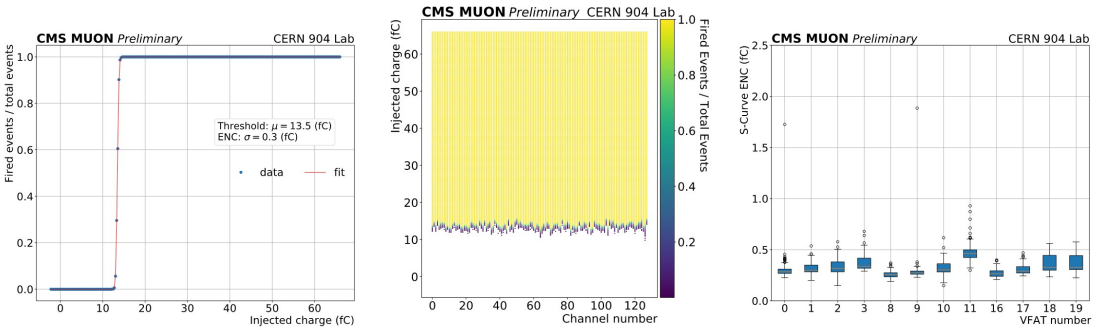

Figure 7: S-Curve for one channel with data and fit results (left). S-Curve for all 128 channels of one VFAT (middle). S-Curve ENC distribution for all 128 channels of 12 VFATs on an ME0 detector (right).

The electronic background noise rate on the VFAT3b trigger links (S-bits) was measured by scanning over the threshold setting. As expected, there is a quick fall off in noise rate as the threshold is increased. The same test is done with the high voltage supply to the GEM chamber turned on (Fig. 8). This results in a non-zero hit rate of cosmic muons in the tail of the falling noise rate, as the threshold is increased and background noise is suppressed.

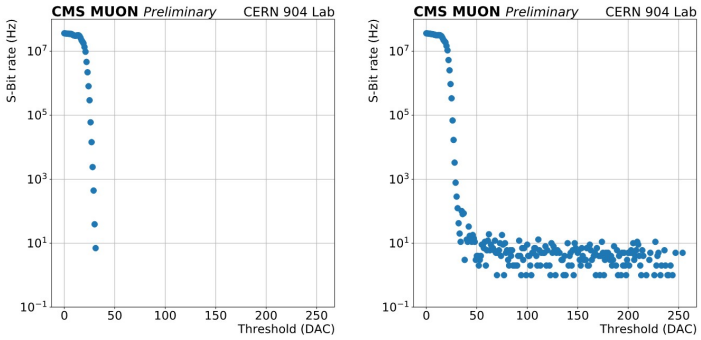

Figure 8: S-bit noise rate vs. threshold from all 128 channels on one VFAT on an ME0 detector without (left) and with (right) application of high voltage across GEM foils.

5 Summary and Outlook

The development of electronics for the far-forward CMS muon detector upgrade, ME0, is progressing well. Design is completed, and either GEB prototypes or pre-production ATCA and OH boards have been produced and successfully tested. Integration of the electronics system with the GEM detector is also progressing well. The project will soon move to a collaboration-wide review of the electronics system before starting the final production.

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