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Electrical performances of pre-productions staves for the ATLAS ITk Strip Detector Upgrade

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Abstract: The ATLAS experiment is currently preparing for an upgrade of the inner tracking detector for High-Luminosity LHC. The new tracker, ITk, employs an all-silicon detector with outer Strip layers. The building block of the ITk Strip barrel is the stave which consists of a low-mass support structure hosting the common electrical, optical and cooling services as well as 28 silicon modules. In this contribution, we outline the challenging aspects of the stave pre-production testing phase at Brookhaven National Laboratory. The electrical characterization of these staves, hosting the final design of both front-end electronics and ASICs, will be discussed in detail.

Keywords: Radiation-hard detectors, Si microstrip and pad detectors, Electronic detector readout concepts (solid-state), Front-end electronics for detector readout,Performance of High Energy Physics Detectors

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1 Introduction

To face the higher radiation levels foreseen at the HL-LHC, the inner tracker of the ATLAS detector will be replaced by an all-silicon Inner Tracker (ITk) consisting of an innermost Pixel and an outer Strips Detector. This outer Strip tracker consists of a four-layer barrel, assembled with silicon-strip staves. A stave consists of 14 micro-strip silicon modules mounted on either side of a carbon composite support structure, which provides mechanical support and houses the necessary electrical, optical, and cooling components.
Half of the ITk Barrel Strip Detector will be assembled at Brookhaven National Laboratory (BNL) between 2023 and 2026. The ITk production is preceded by two preproduction phases, PP-A and PP-B. In the PPB phase the final layout and design of all parts are adopted. This paper shows the electrical characterization measurements of pre-production staves built in 2022.

2 ITk Stave Schematics

An ITk Strip Stave comprises a support structure made of carbon fiber and foam into which a cooling pipe is integrated. A copper/kapton bus tape is co-cured on both external faces of this support structure to route electrical services between the End of Substructure (EoS) card and the detector modules. The EoS represents the interface between the stave and the off-detector electronics [1, 2]. It hosts a radiation hard low power GigaBit Transceiver (lpGBT [3]) and a Versatile link (VTRx+ [4]) fibre optics driver for high speed optical transmission. The EoS distributes CCR (Clock, Control, Reject) signals to the front-end ASIC chips via the corresponding bus on the bus-tape. These are segmented, multidrop CCR signals at 160 MHz. Moreover, each module returns a point to point event data at 640 Mbit/s.
To ensure power is delivered to the modules without increasing the cable density, a DC-DC powering

scheme has been adopted. Each stave has a common low-voltage power bus at 11 V, which is further step-down to the 1.5 V needed by the front-end ASICs by using on-module DC-DC buck converters (bPol12V [5]). Similarly, the number of high voltage buses used to provide sensor bias to the fourteen modules on each stave side are reduced to four. Both high-voltage and low-voltage buses route along one edge of the stave together with the Detector Control System (DCS) signals [1].
A module [6] consists of a silicon sensor, one or two polyimide pcbs called hybrids and a powerboard. For the barrel area, two sensors variant are used: long strip (LS) sensors and short strip (SS) sensors, having the same geometry but different strip lengths. The hybrid hosts the readout ASICs: 10 ABCStar chips (for barrel modules) and a controller chip called HCCStar. Each ABCStar has a binary architecture, with 256 channels of trimmable preamplifier, discriminator and control logic. Each ABCStar has also a point-to-point 160 Mbit/s data path to the HCCStar, enabling fast readout. The Power Board is responsible to deliver both LV and HV power to the module. It hosts a DC-DC buck converter [5] meant to step down the input LV power to the 1.5 V needed by the front-end ASICs and an Autonomous Monitor and Control (AMAC) chip which provides on-module environmental monitor and control functions.

3 Pre-production Staves

The ITk production is preceded by two pre-production phases, PP-A and PP-B. While in first one some prototype components have still been used, in the PP-B phase the final layout and design of all parts are adopted. During 2022, two pre-production staves have been assembled and tested at BNL: one PP-A LS stave which has the final version of the ABCStar chips, but prototype versions of the HCCStar and AMAC chips and one PP-B stave which has the final version of the all chip-sets.

3.0.1 PPA Electrical results

Fig 1 shows the gain profile for all 14 modules on one side of the stave at -400 V bias voltage and for different temperatures: $22^{\circ}C$(in red), and $-35^{\circ}C$ (in blue). The plots confirm the ABCStar gain dependence upon temperature, with the gain decreasing linearly as the temperature increases. Despite the temperature dependence, the gain response is kept uniform within a chip, with small variations observed on a chip to chip basis. The input noise profile at the same temperatures and bias voltage is shown in Fig 2. Overall good performance are observed for all the modules. An increased noise due to EMI emission of the DC-DC converter coil is observed in strip channels located centrally [6].

3.1 PPB Electrical results

The 28 SS module PPB stave hosts the final version of ABCStar, HCCStar and AMACStar chipset. Thermal cycles of the stave have shown a uniform gain response both at cold and room temperature. Fig 3 shows the input noise profile for all the modules on one side of the stave. Good noise performance are observed at room and cold temperatures except for some modules that at cold temperature feature some noise peaks, which we refer to as Cold Noise. This Cold Noise, observed also during thermal cycles of single modules, has been mainly observed on the rows of strips having the hybrid and powerboard glued on top without a well-defined pattern. As this Cold Noise requires more deep investigation, further studies are on-going at module level.

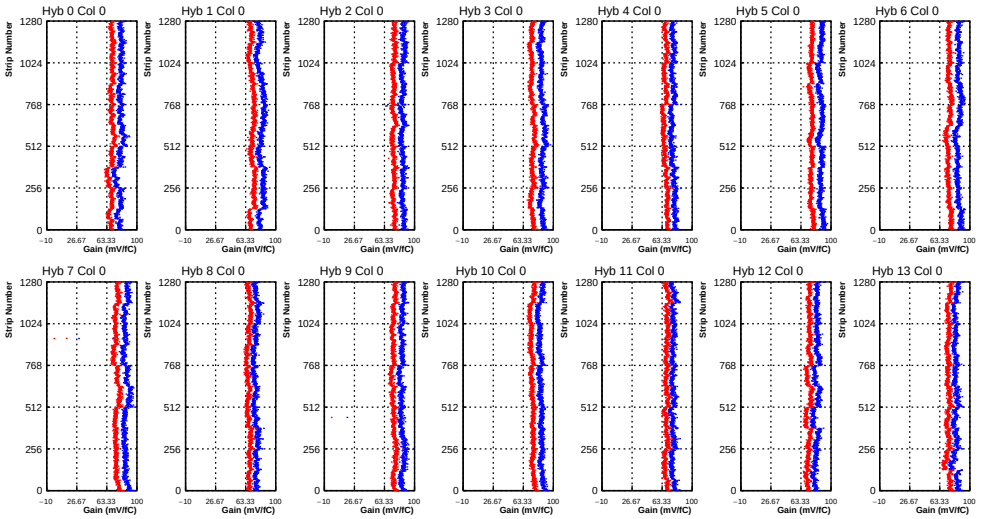

Figure 1. Gain profile for the fourteen modules on one side of the PPA stave at $V_{bias} = -400V$. Modules are ordered from 0 to 13. The curves refer to two different testing temperatures: $22°C$(in red), and $-35°C$ (in blue).

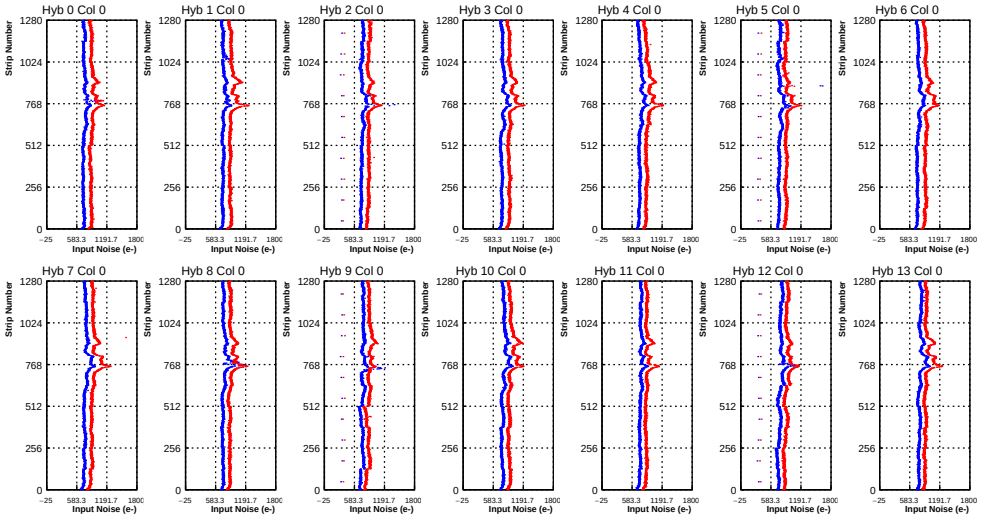

Figure 2. Noise profile for the fourteen modules on one side of the PPA stave at $V_{bias} = -400V$. Modules are ordered from 0 to 13. The curves refer to two different testing temperatures: $22°C$(in red), and $-35°C$ (in blue).

3.1.1 PPB Stave signals

As the PPB stave hosts the final version of the HCCStar, it represents the first stave where the signal integrity at the designed data rate of 640 Mbit/s could be tested. Fig 4 shows the eye diagram for the HCCStar 0 data respectively at the Hybrid and at the EoS side. Good signal communication is established between the two ends, confirmed also by no BER error at 640 Mbit/s.

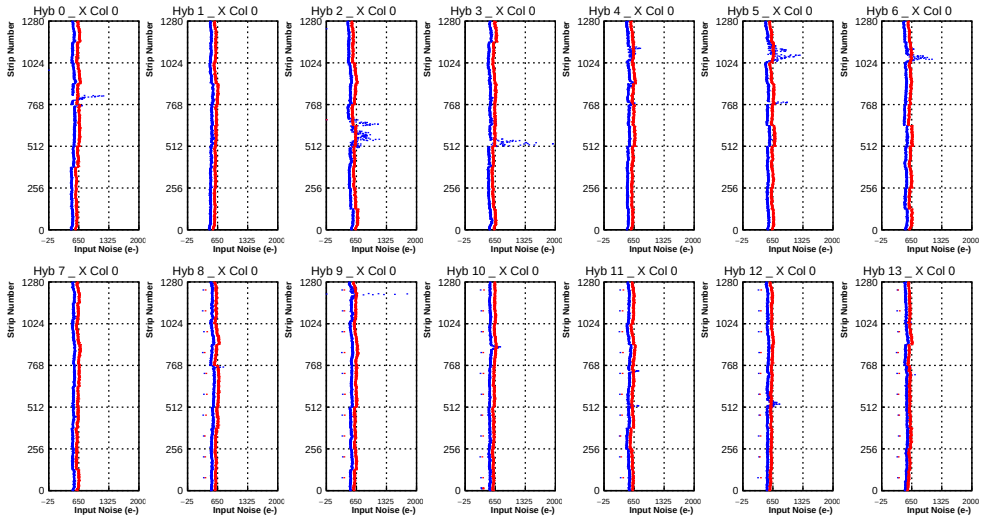

Figure 3. Noise profile for the fourteen modules on one side of the PPB stave at $V_{bias} = -400V$. Modules are ordered from 0 to 13. The curves refer to two different testing temperatures: $22°C$(in red), and $-35°C$ (in blue).

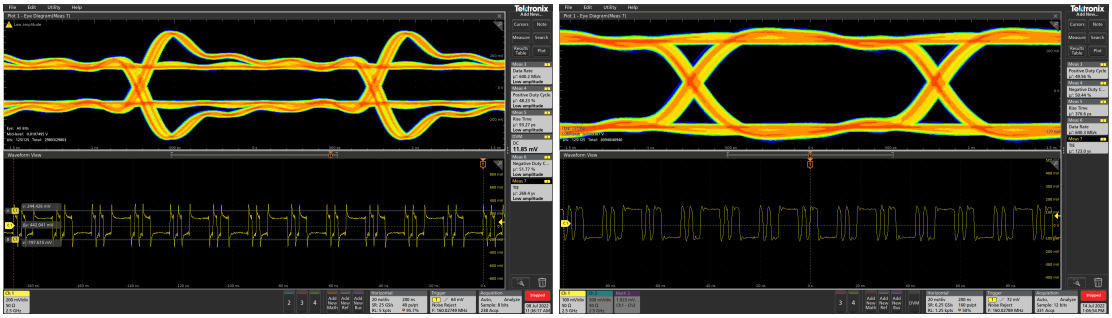

Figure 4. Eye Diagrams for the HCCStar 0 data at 640 Mbit/s. The HCCStar 0 is the farthest from the EoS, and then characterized by the longest data trace. The eye diagram are reported for both the driver side - Hybrid (left) and for the receiver side -EoS (right).

3.1.2 PPB Stave monitoring

The AMAC chip on the powerboard allows on-module monitoring and control functions. Among those, the possibility to monitor the HV return current, a function that will become significant during detector operation when higher current is expected due to the radiation damage. Fig 5 shows the HV return current measurements for all the 14 modules on the PPB stave as a function of the HV bias voltage. Good resolution is achieved with the final version of the AMAC chip (AMACStar). In addition, these measurements of the HV return current made using the AMACStar have shown to be greatly improved from the prototype version of AMAC, mainly due to the removal of AC coupling capacitors between HV return line and hybrid ground which had previously shown to introduce additional noise.

On-module temperature monitoring is also accessible through the AMAC by using the 10K NTCs on hybrids and powerboard and the proportional to absolute temperature (PTAT) channel which

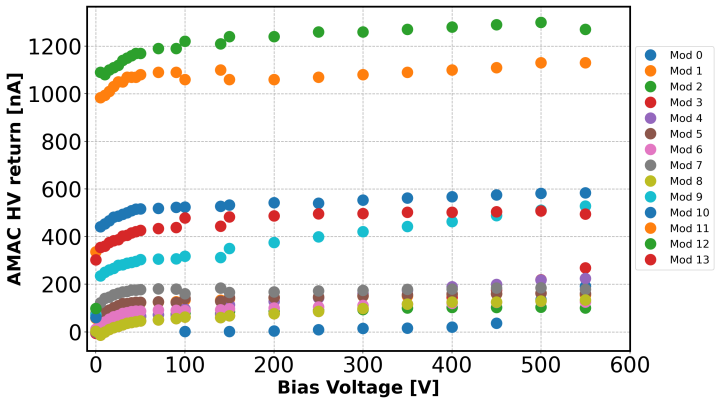

Figure 5. HV return current measurements for all the 14 modules on one side of the PPB stave as a function of the HV bias voltage. Modules 11 and 12 which are close to the EoS are characterized by higher current, most likely due to the light from the VTRx+. Chip-to-chip offset can be corrected by measuring the current at $V_{bias} = 0$.

allows to estimate the bPOL12V temperature. Fig 5 shows the temperatures for all the module on the stave. A module-to-module variation is observed, with the bPOL12V being the hottest part of a module, as expected. These temperature variations can be correlated to differences in the module assembly procedure.

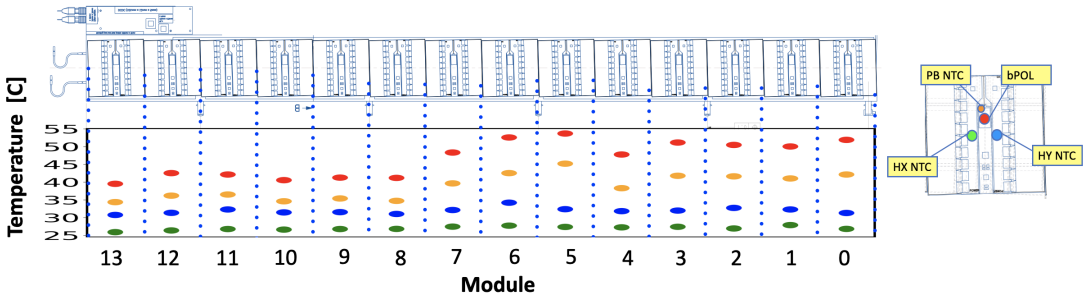

Figure 6. Stave temperature monitoring through the AMACStar by using the 10K NTCs on the hybrids (green and blue), and on the powerboard (orange) and the PTAT channel (red) which allows to estimate the bPOL temperature.

4 Conclusions

Meeting the requirements imposed by the HL-LHC operational conditions presents a unique challenge for the ITk Strip detector. This important study wanted to show the results from pre-production staves in terms of electrical performance and signal integrity at the designed data rate of 640 Mbit/s. Moreover, the good performance of the AMACStar chip which allows on-stave monitoring of temperatures and currents have also been investigated.

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