

Detecting the position of the sealring and the edge on the sensor chip

G R Panjaitan¹, K M Lhaksana², E Prakasa³ and L Musa⁴

^{1,2}School of Computing, Telkom University, Jalan Telekomunikasi No. 1 Terusan Buah Batu, Bandung 40257, Indonesia.

³Research Center for Informatics, Indonesian Institute of Science (LIPI), Bandung, Indonesia.

⁴ALICE – A Large Ion Collider Experiment, The European Organization for Nuclear Research (CERN), Geneva, Switzerland.

¹gandarain@students.telkomuniversity.ac.id, ²kemasmuslim@telkomuniversity.ac.id,

³esa.prakasa@lipi.go.id

Abstract. ALICE (A Large Ion Collider Experiment) is one of the physics projects developed by CERN. The project aims to observe the results of collisions between proton and proton, proton and nucleus, and nucleus with nucleus. Thousands of sensor chips are used to record the collision trajectory. Visual inspection with digital image processing has been developed to analyze the conditions of cutting the sensor chip, using the Hough Transform, Edge Detection, and Template Matching methods. The distance from the edge to the sealring chip will be used as a reference to determine how the condition of chip cutting. The results obtained are quite good and give a support for the next research process.

1. Introduction

ALICE (A Large Ion Collider Experiment) is one of the projects in physics at CERN (Conseil Européen pour la Recherche Nucléaire), Switzerland. The project aims to observe how the physical characteristics if proton-proton, proton-nucleus, and nucleus-nucleus are collided. The two particles are accelerated on a long path, when the speed is correct or it is near the speed of light, the two particles are directed in the opposite directed and crashing each other using a Large Hadron Collider (LHC) [1].

Observations were made at the LHC, and the particles crashed were in the Inner Tracking System (ITS). ITS is at the center of the LHC which has seven concentric sensor cylinders. Cylinders with the smallest diameter (46 mm), namely Layer 0, are located in the innermost part of the ITS system. The largest cylinder, Layer 7, is designed with a diameter of 786 mm. Thousands of sensor chips with size (30 × 15 mm²) are mounted on the cylinder surface to record the track [1].



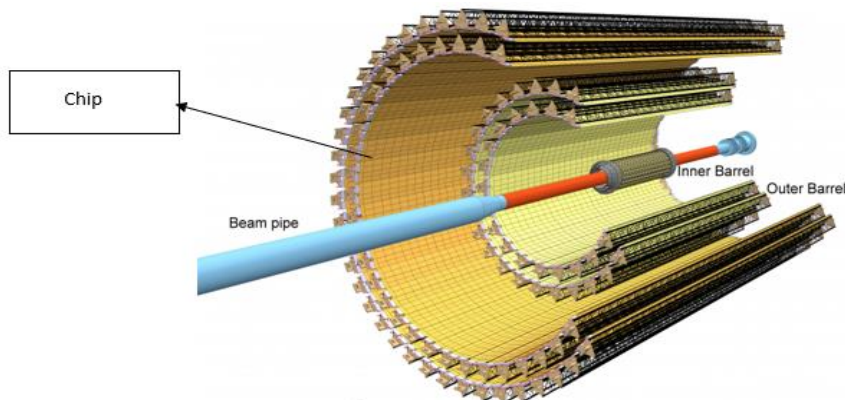


Figure 1. Inner Tracking System (ITS). [2]

Thousands of sensor chips are used to record tracks. In the manufacturing process, it is known as a wafer, which is made of pure silicon in the form of a circle. Wafers and chips are unity because wafers are a collection of similar chips. The wafer are cutted with laser or other cutting machine, according to a specified distance. So that if the chip cuts are not suitable it can damage the chip or other chips.

The cutting condition of the chip can be known by calculating the distance from the sealring to the edge of the chip. Therefore, we need an algorithm that is able to detect the position of the sealring and the edge of the chip. If the position of the sealring and edge of the chip is known, the process of determining the chip cutting condition can be done easily. Therefore, this algorithm is needed to help the process of determining the quality of chip cutting.

This paper is organized as follows. In part 2 there are several methods and research that has been previously developed. In part 3 there are the explanation of the algorithm to be developed. The results of the developed algorithm are explained in section 4. And in the last section there is a conclusion.

2. Related Works and Discussion

2.1. Visual Inspection in Electronic Components

Visual inspection using image processing methods has been widely applied to check the condition of electronic components. The Hough Transform, Edge Detection and Template Matching methods are used to develop a visual inspection algorithm on electronic components. Usually this methods are used to detect position and check for damage to electronic components.

A hybrid algorithm has been developed to check the damage to the chip wafer. The method uses Hough Transform and Canny Edge Detection to find the end of the chip. In the development process, this algorithm uses 14 training images and 137 testing. Accuracy obtained are 92.8% for training images and 86.0% for testing [3]. In addition, there is a Line Extraction algorithm that was developed to analyze the damage to the IC, by utilizing a sound device SEM (Scanning Electron Microscopy) to take the image from the IC. The algorithm uses the Hough Transform method to detect the edge of the IC [4].

Besides of detecting edge lines and chip ends, the image processing method is also used to create template images of electronic components. As in the Defect Detection algorithm, it uses the Canny Edge Detection method to create template from wafers. This template will be used to analyze damage from wafers [5].

A *real time* or *live* algorithm for visual inspection has also been developed, one of which is the FPGA. The algorithm uses the Template Matching method to detect the location of electronic components. This algorithm can help the inspection process on chips, ICs and other semiconductor components. FPGA speed is 13 times and 80 times faster than PC [6].

Visual inspection is also applied to check LCD, as in Defect Inspection algorithm developed to improve the quality of LCD display and results. The algorithm uses the Hough Transform method to accumulate scratches on the LCD. [7].

2.2. Visual Inspection in Industry

In addition to the field of electronic components, visual inspection are often applied in industrial fields too, to check the products they produce. Image Processing methods used are generally the same as the electronic components, such as Hough Transform, Template Matching and Edge Detection.

The Automated Visual Inspection (AVI) algorithm has been developed to examine the results of metal products produced in real time, the Canny Edge Detection method is used to detect metal edges and Hough Transform to calculate the diameter of the metal. The results is the algorithm are able to calculate the diameter of the metal despite the difference in pixel intensity in the metal image [8]. Besides metal, there is an Improved Canny Edge Detector algorithm that is used to check ceramics. The algorithm uses the Canny Edge Detection method to detect cracks in ceramics. The algorithm developed are capable to process 20 images and the accuracy obtained are 98% [9].

The combination of Edge Detection and Template Matching can also assist the inspection process, as in the Automated Crack Detection algorithm using the Edge Detection method to create a template from the bridge bolt then uses Template Matching to detect the position of the bolt. The goal is to create a machine in real-time that can detect damage or cracks on the bridge [10].

In the Automated visual inspection algorithm, it were developed to check the condition of BBB (Break Beam Bolt) on the railroad tracks. Template Matching method is used to detect the position of the bolt, after that SVM (Support Vector Machine) is used to classify the condition of the railroad tracks based on the position of the bolt. The accuracy obtained from this algorithm are 100% for the first set of data, 99.21% for the second data set and 99.64% for the third data set. [11].

3. Research Methodology

The data used are the image of the chip. Derived from a machine developed by CERN namely ALICIA. In the image retrieval process, ALICIA scans the edges of chips, starting from the top, left, bottom, and right edges. So that one chip has 84 images. The image retrieval process greatly determines the results that are obtained because if the image is blurry or not good, it is difficult to process. The following are sample and image scanning processes.

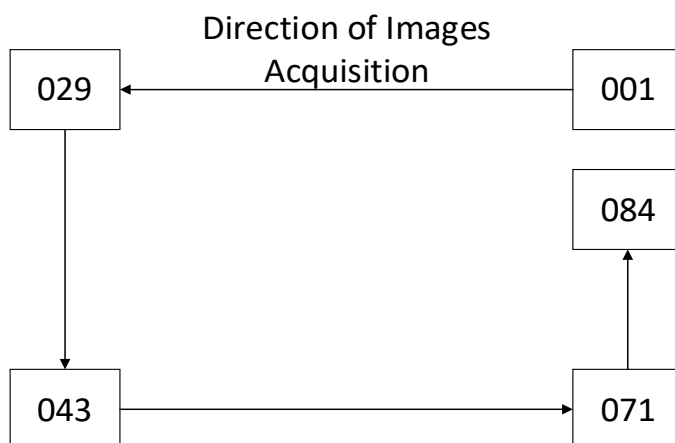


Figure 2. Direction of images acquisition with ALICIA.

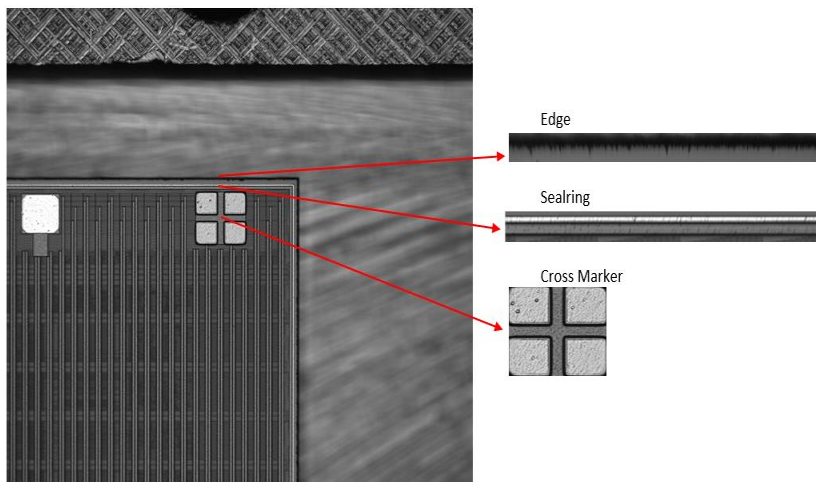


Figure 3. Examples of images from the chip and the parts to be observed.

The algorithm developed has two main processes, namely ROI Extraction and Dividing ROI. In the ROI Extraction process, the input image will be cut so that the resulting image focuses on the sealring and chip edges. This is needed to reduce interference from other chips, so that the algorithm is able to focus on the part of the image to be observed. The image results from the ROI Extraction will be used in the Dividing ROI process. In this process, the ROI image will be divided into 2 parts, the edges and sealring.

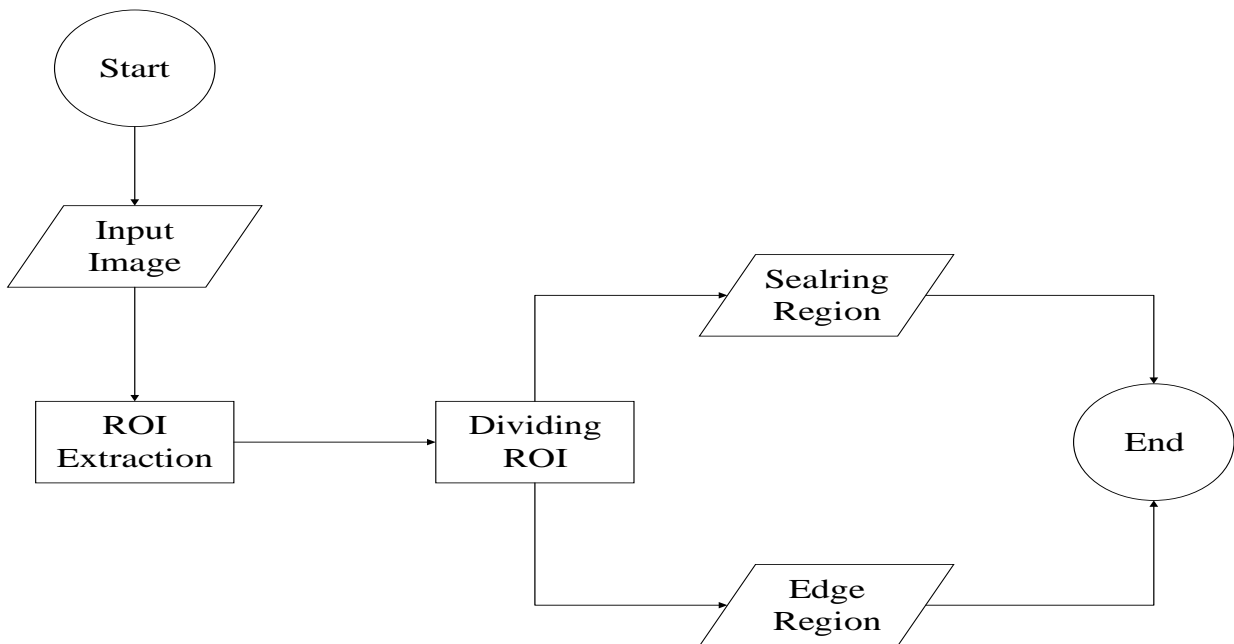


Figure 4. General description of the system.

In the image retrieval process, there are the possibility of the location of the slanted chip so that the resulting image are also tilted. This causes the image cutting process to require an algorithm to detect the slope of the image so that cutting can be done automatically. The slope value in each section may be different, the top and bottom may be different as well as left and right. Each sensor chip has four markers at the end, called cross markers. The marker can be used to determine the slope of the chip, because the position is fixed if the chip image is not tilted, and vice versa.

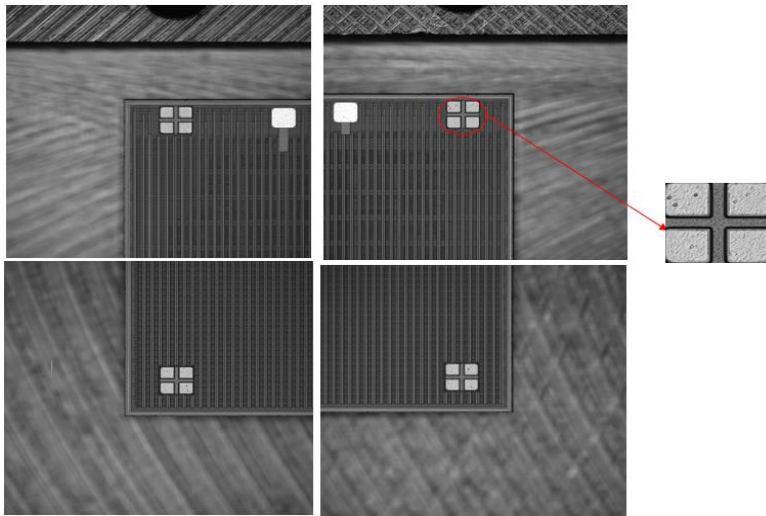


Figure 5. Cross Marker located on each corner of the chip.

The process of finding the position of the cross marker location begins with creating a template. The template will be used for the Template Matching method. Template Matching will detect where the object's position is similar to the input template, so that with this method, the cross marker position will automatically be known. Once the position are known, the midpoint of the cross marker can be searched by tracing each pixel in the section that matches the threshold value. Each pixel that matches the threshold value will be added then divided by the total of the amount.

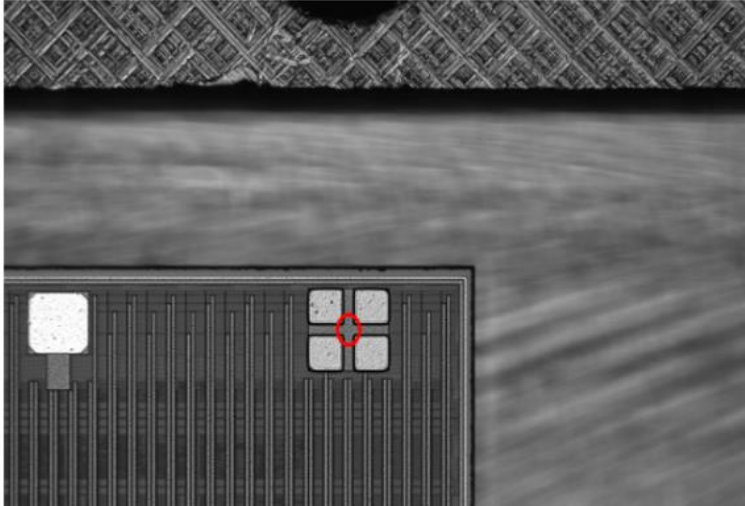


Figure 6. Detect the midpoint of Cross Marker in the right corner of the chip.

After the midpoint position of the cross marker is known, the value will be compared with the other cross markers on each chip section, the results of the comparison will be applied to a line equation that will represent the slope of a chip section. At the top of the chip, the horizontal point in the first and 28th image cross markers are considered as y_1 and y_2 . Whereas for Δx the sum of vertical points in the cross image of the first image and the 28th image, and the width of the upper image. The values of Δx and Δy will be used to find the equation of the line in the chip section. More details are shown in the following equation:

$$\Delta y = y_2 - y_1 \quad .(1)$$

$$\Delta x = x_1 + (\text{number of images} * \text{img. cols}) + (\text{img. cols} - x_2)$$

$$m = \frac{\Delta y}{\Delta x}$$

The level of the chip slope is known by looking for the gradient. Δx and Δy values The gradient value will be used to determine the equation in a chip section, where x is the width of the image and c is the horizontal point in the first image.

$$y = mx + c \tag{.2}$$

$$y = \frac{y2 - y1}{x1 + (\text{number of images} * \text{img. cols}) + (\text{img. cols} - x2)} x + y1$$

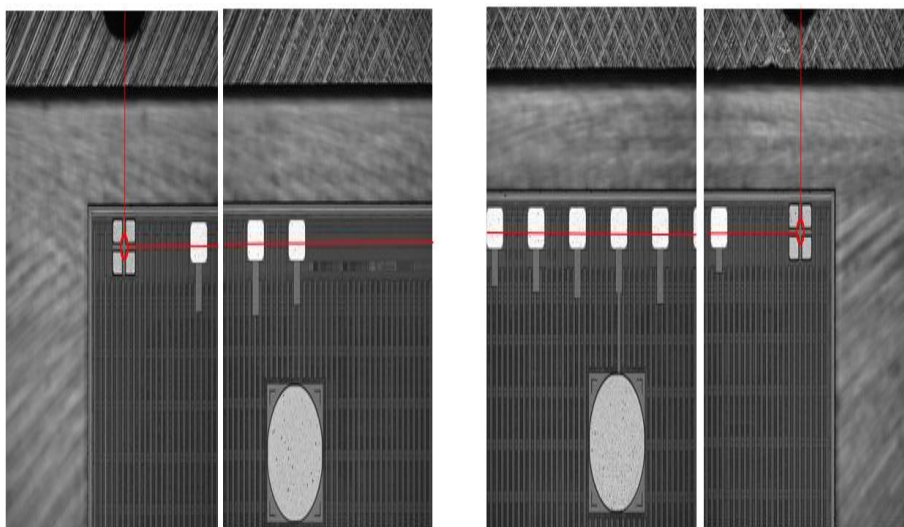


Figure 7. ROI Extraction Process.

By knowing the slope level, image cutting can be done automatically. Image cutting is done because the developed algorithm will focus on the edges and sealing chips, and to reduce noise or noise from other parts of the image. Image cutting results will be divided into two parts, namely sealing and chip edge, because the method used for sealing and chip edge are different.

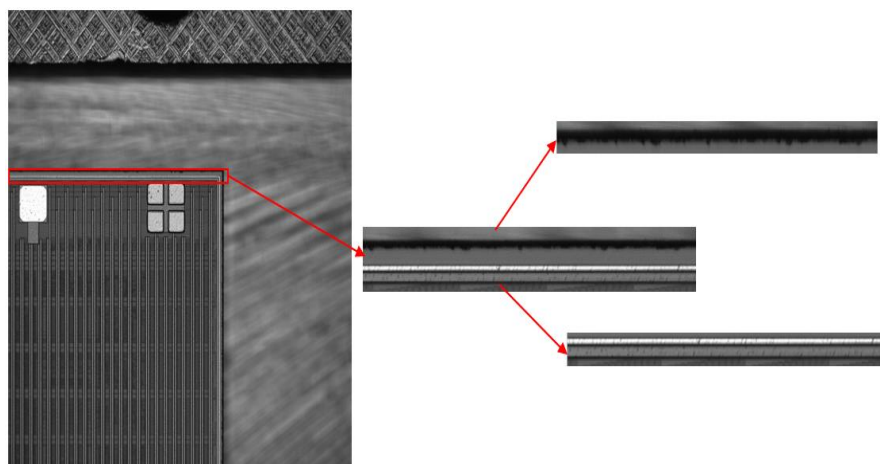


Figure 8. The process of detecting the sealing position and the edge of the chip on the ROI.

4. Result and discussion

This algorithm is applied to 2 chips, the first and second chips. The results that obtained, are the algorithm is able to detect the position of the sealring and edges of the first and second chips precisely and consistently. Although the image quality is different from the first and second chips, the algorithm still able to accurately detect sealring and chip edges.

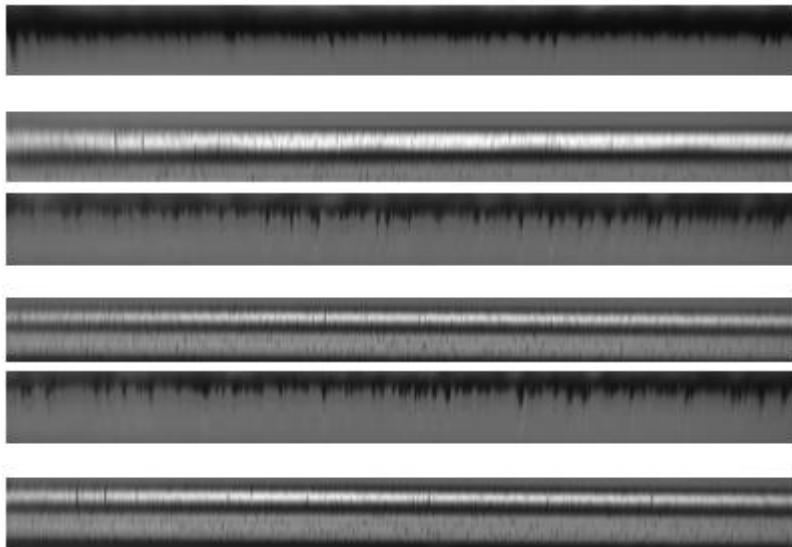


Figure 9. The algorithm is able to detect the position of the sealring and edges on the first chip.

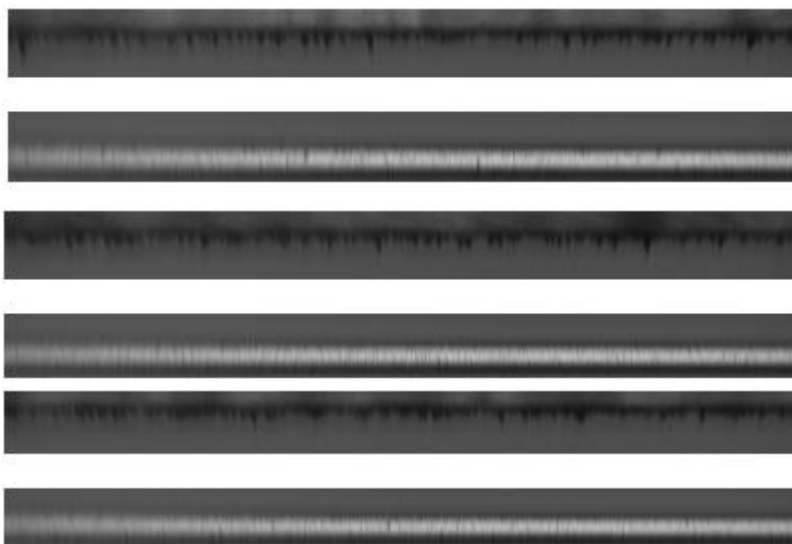


Figure 10. The algorithm is able to detect the position of the sealring and edges on the second chip

But in some images, the algorithm cannot detect the exact position of the chip's edge. This is caused by cutting the chip too deep so that the edges of the chip are considered as part of the sealring.

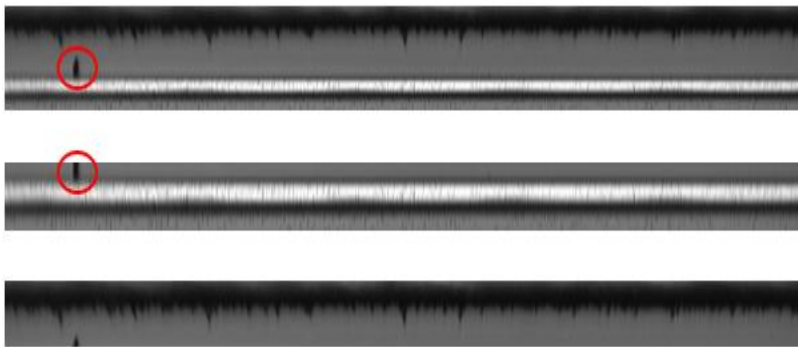


Figure 11. There is an error in second image of the first chip.

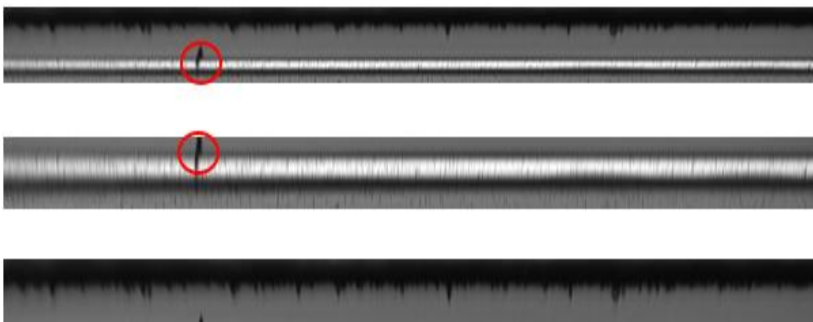


Figure 12. There is an error in sixth image of the second chip.

The algorithm error results are displayed in a table. The number of algorithm errors are less than the correct algorithm. This error generally occurs at the edges, where the algorithm detects the edge of the chip to be part of the sealring.

Table 1. Number of algorithm errors on the first and second chips.

	number of algorithm errors
The First Chip	5 images
The Second Chip	0 image

In the first table, there are number if algorithm error on the first and second chips. Number of algorithm error on first chip is 5 images dan 0 image for the second chip. The amount of images that has been processed are 168 images. Accuracy value is obtained by comparing the number of algorithm errors on the first and second chips with all images, so the accuracy value is 97%.

5. Conclusion

The developed algorithm data can detect the position of the cross marker, calculate the slope of the chip, detect the ROI that will be observed and detect the sealring and edge of the chip. Algorithm errors occur in several images, as in the first chip, there are 5 images. This is caused by cutting the chip too deep, so that the edges of the chip are considered as part of the sealring by the algorithm. Based on algorithm errors, the accuracy obtained by this algorithm is 97%. The algorithm developed is considered capable of correctly detecting sealring and edge of the chip even though in some cases an error occurs. Therefore, this algorithm is expected to help to determine the quality of chip cutting.

References

- [1] Prakasa, E., Kurniawan, E., Nurhadiyatna, A., Musa, L., & Reidler, P. (2015, November). Implementation on 3d surface algorithm for measuring thickness parameter of sensor chip. In *Intelligent Signal Processing and Communication Systems (ISPACS), 2015 International Symposium on* (pp. 199-203). IEEE.
- [2] Abelev, B., Real, J. S., Margotti, A., Contreras, J. G., Karavicheva, T., Arsene, I. C., ... & Shtejer, K. (2013). Technical design report for the upgrade of the ALICE inner tracking system. *J. Phys. G*, *41*(CERN-LHCC-2013-024), 087002.
- [3] Chang, C. F., Wu, J. L., & Wang, Y. C. (2013). A hybrid defect detection method for wafer level chip scale package images. *International Journal on Computer, Consumer and Control*, *2*(2).
- [4] Shu, D. B., Li, C. C., Mancuso, J. F., & Sun, Y. N. (1988). A line extraction method for automated SEM inspection of VLSI resist. *IEEE Transactions on Pattern Analysis & Machine Intelligence*, (1), 117-120.
- [5] Shankar, N. G., & Zhong, Z. W. (2005). Defect detection on semiconductor wafer surfaces. *Microelectronic engineering*, *77*(3-4), 337-346.
- [6] Chen, J. Y., Hung, K. F., Lin, H. Y., Chang, Y. C., Hwang, Y. T., Yu, C. K., ... & Chang, Y. J. (2012, July). Real-time FPGA-based template matching module for visual inspection application. In *Advanced Intelligent Mechatronics (AIM), 2012 IEEE/ASME International Conference on* (pp. 1072-1076). IEEE.
- [7] Tsai, D. M., Tseng, Y. H., & Fan, S. M. (2018). Defect Inspection of Liquid-Crystal-Display (LCD) Panels in Repetitive Pattern Images Using 2D Fourier Image Reconstruction. *ICAS 2018*, 21.
- [8] Akbar, H., & Prabuwo, A. S. (2008). Automated visual inspection (AVI) research for quality control in metal stamping manufacturing. In *Proc. the 4th International Conference on Information Technology and Multimedia (ICIMU'08)* (pp. 626-630).
- [9] Hocenski, Z., Vasilic, S., & Hocenski, V. (2006, November). Improved canny edge detector in ceramic tiles defect detection. In *IEEE Industrial Electronics, IECON 2006-32nd Annual Conference on* (pp. 3328-3331). IEEE.
- [10] Yeum, C. M., & Dyke, S. J. (2015). Vision-based automated crack detection for bridge inspection. *Computer-Aided Civil and Infrastructure Engineering*, *30*(10), 759-770.
- [11] Nan, G., & Gao, Y. (2018). Automated visual inspection of multipattern train components using gradient information and feature fusion under the illumination-variant condition. *Proceedings of the Institution of Mechanical Engineers, Part F: Journal of Rail and Rapid Transit*, *232*(5), 1500-1513.