Hardware Design and Testing of the Generic Rear Transition Module (GRM) for the Global Trigger Subsystem of ATLAS Phase-II Upgrade

Filiberto Bonini and Shaochun Tang
on behalf of the ATLAS TDAQ Collaboration

TWEPP 2022 Bergen
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Outline

- Global Trigger subsystem
- GRM Hardware Design
- GRM Hardware Testing
- Conclusions

Global Trigger subsystem

ATLAS TDAQ Phase-II Upgrade

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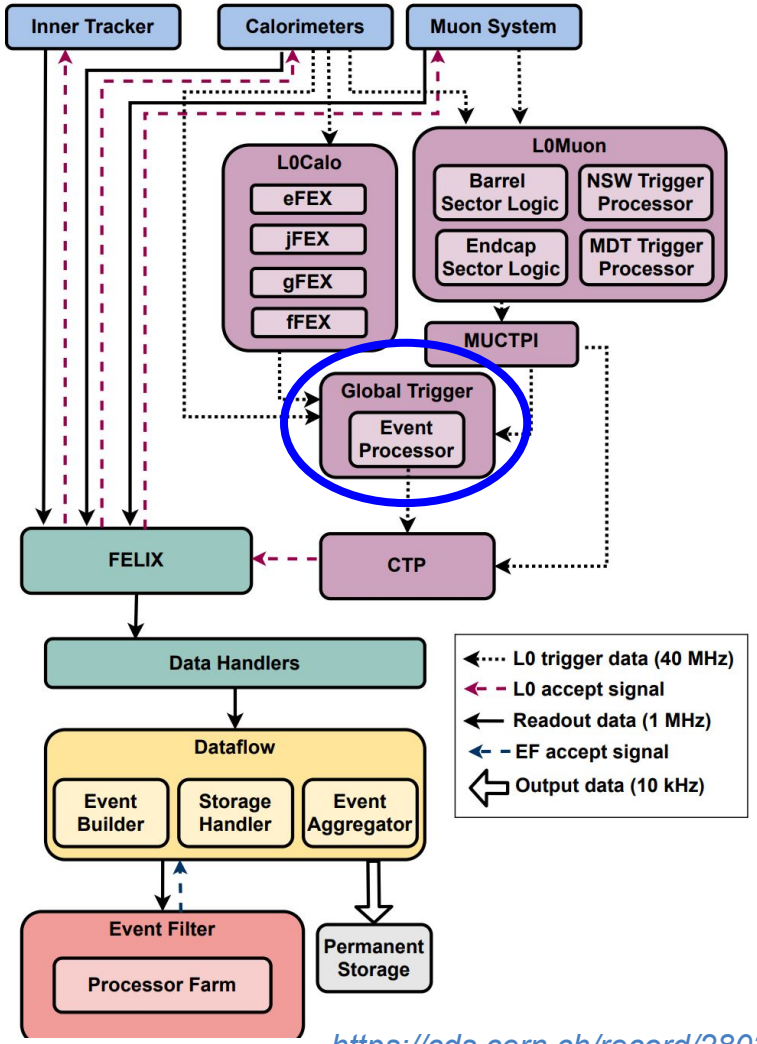
Global Trigger subsystem

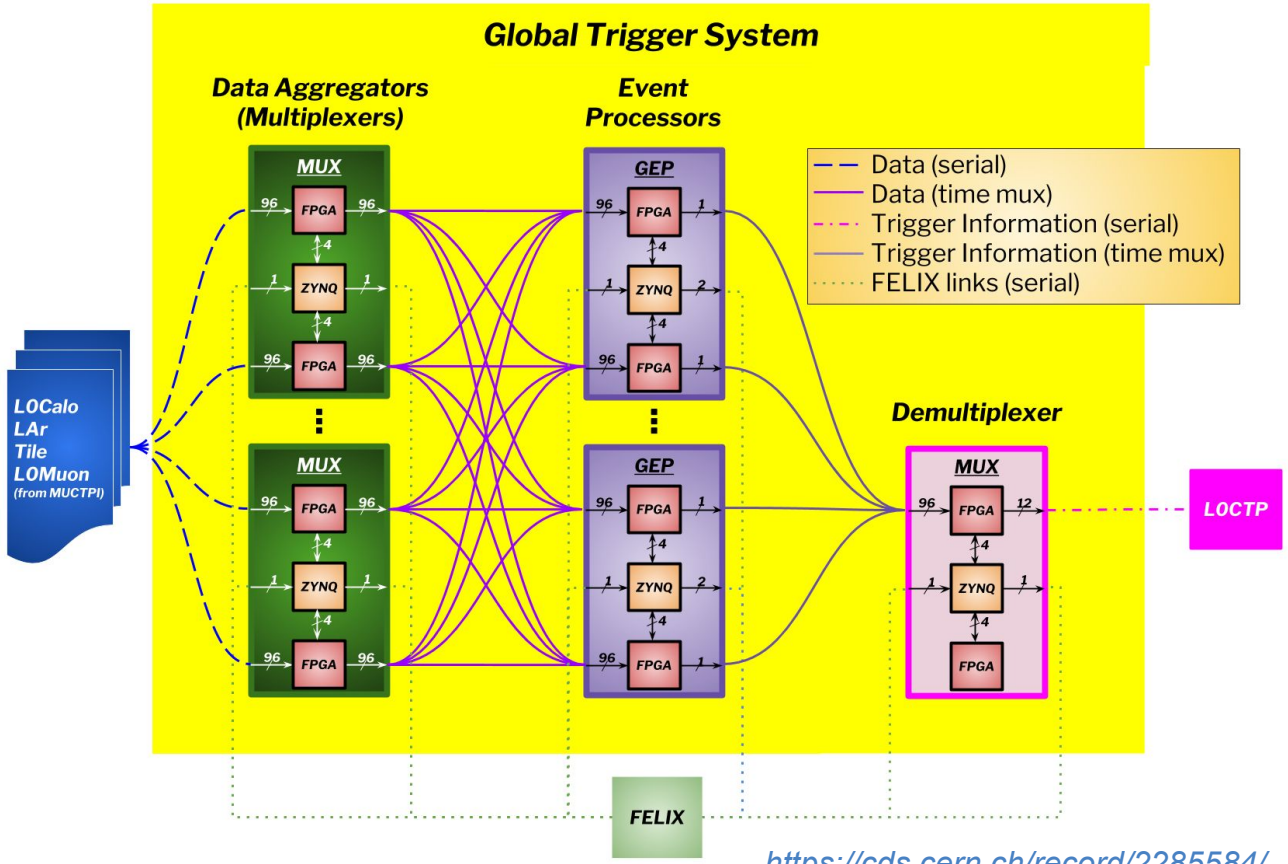


- Single-level **Trigger** in **Run 4** (HL-LHC)
  - Installation at Large Hadron Collider Long Shutdown 3 ~ 2026-8
- New **Global Trigger** subsystem
  - Receive all trigger information from legacy / new systems; Concentrate data for a full bunch-crossing (BC) event onto a single processor ~ MUX
  - Replace and extend functionality of the first stage of the Run-3 topological trigger; Identify topological signatures, perform offline-like (i.e. close to full reconstruction) algorithms on full-granularity calorimeter data ~ GEP
  - Send processed trigger information to Central Trigger Processor (CTP) for final decision ~ CTP-Interface

https://cds.cern.ch/record/2802799/files/ATLAS-TDR-029-ADD-1.pdf

Global Trigger hardware

- Firmware-based project
  - 3 layers (MUX, GEP, CTP-interface)
  - Several processing nodes
- Common hardware platform ~ 50x
  - Global Common Module (GCM) - cf. TWEPP-2021
  - Advanced Telecommunications Computing Architecture (ATCA) board
  - Simplify system design and long-term maintenance
- Generic Rear Transition Module (GRM)
  - Mitigate the risks of the complex design and power management



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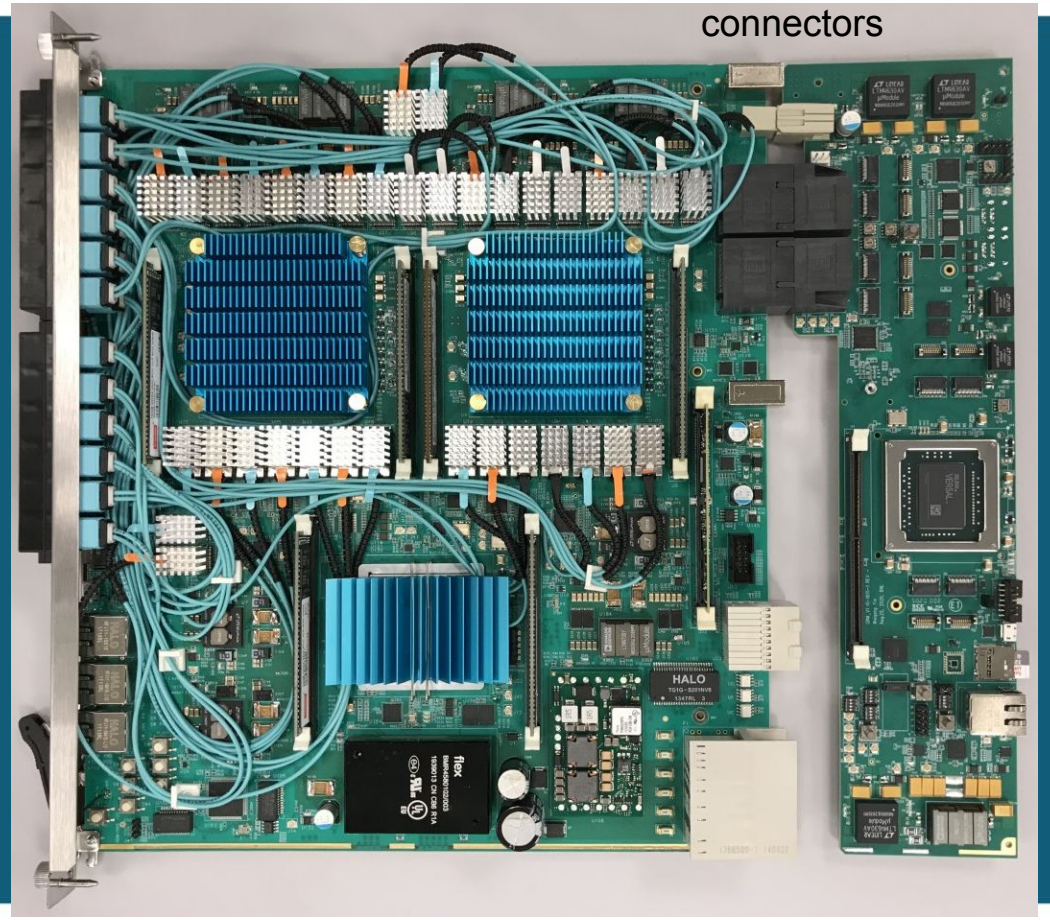
GRM Hardware Design



Generic Rear Transition Module (GRM)

2x **ADM1066** power mgmt.
sequencing and monitoring

Samtec ECUO FireFly
2x TxRx 25-Gb/s
12-ch pairs (6 GTY quads)

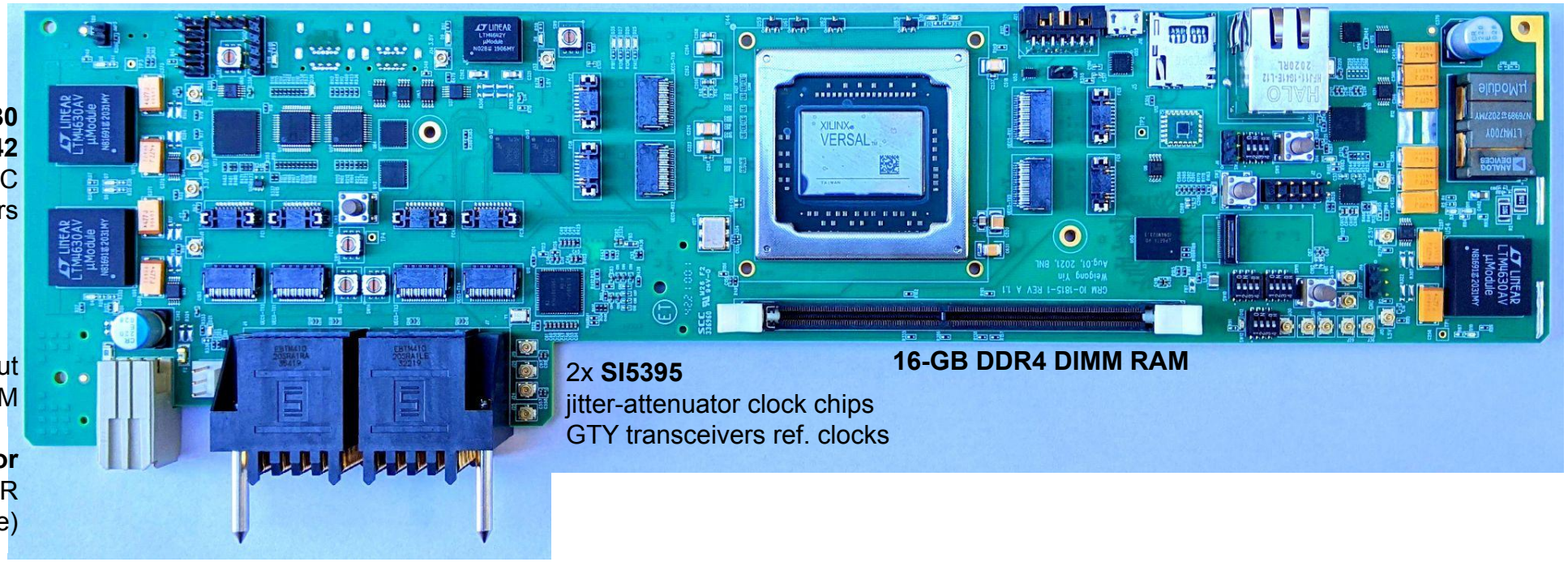
Samtec ECUO FireFly
4x Tx 25-Gb/s 12-ch modules from
GCM MGTs via Zone-3 conn.

QSPI
2x 2Gb
flash

Versal Prime
Xilinx VM1802
ACAP FPGA

CERN MMC

JTAG, UART, SD 3.0, GbE RJ45, PHY



3x **LTM4630**
LTM4642
dual-rail DC/DC
regulators

12V power input
from GCM

Zone-3 connector
Samtec EBTM L/R
2*(40-diff, 10-single)

2x **SI5395**
jitter-attenuator clock chips
GTY transceivers ref. clocks

16-GB DDR4 DIMM RAM

LTM4700 VCCINT
DC/DC regulator

lpGBT
+ VTRx+

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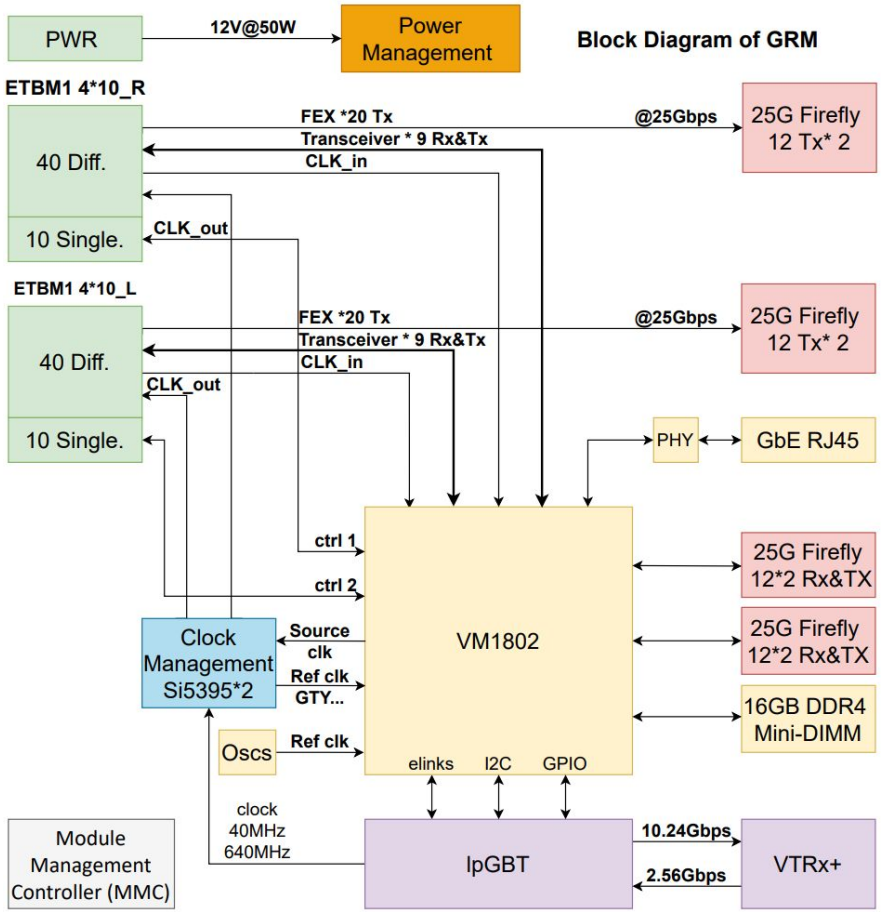
Generic Rear Transition Module (GRM)

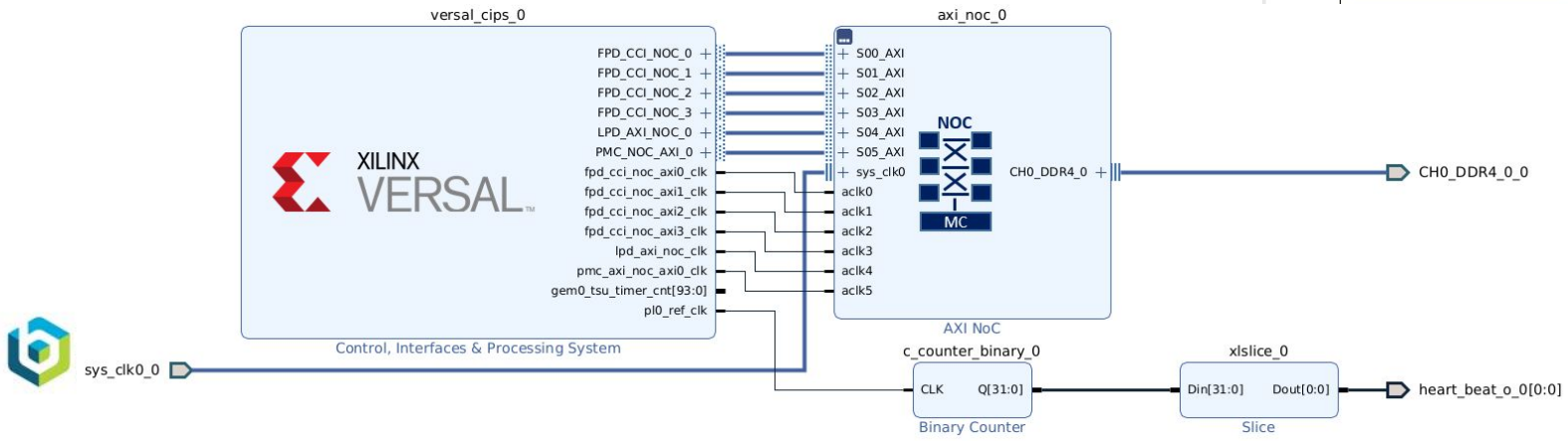
- 82x **25.8 Gb/s MGT links**
  - GRM VM1802 : 2 TxRx 12-ch FireFly pairs, 24 GTY MGTs ~ Communication with FELIX subsystem
  - GCM readout : 4 Tx-only 12-ch FireFly, 40 GTY MGTs
  - GCM control : 2*9x TxRx GTY MGTs pairs for 2 XCVU13P processing-FPGAs on GCM front board through the Zone-3 connector
- MGT ref. clocks by 2x Skyworks SI5395 jitter-attenuator clock chips
- Emulate LAr sRTM, compatible with LASP
  - **lpGBT** chip enables emulation of detector front-ends (FEB2→LASP) for initial integration tests

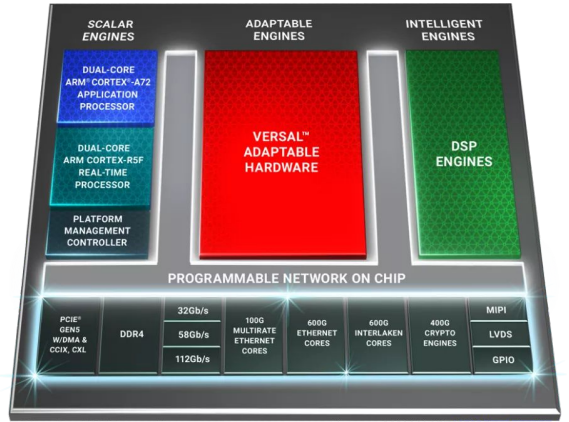


GRM Hardware Testing

Versal bring-up CIPS, NoC, DDRMC

- New ACAP 7nm het. computing (PL, PS/OS)
  - New Versal flow, IPs
- CIPS: Control, Interfaces & Processing System
- NoC & DDRMC
  - AXI-based interfacing, saves resources & power, P&R runtime, CDC, SLRs xing: easier switch-based routing
  - 1080 MHz * 128b = 17.28 GB/s
  - DDR4-MC 2400 MT/s: tests, margins > ±120ps





I2C devices configuring and monitoring

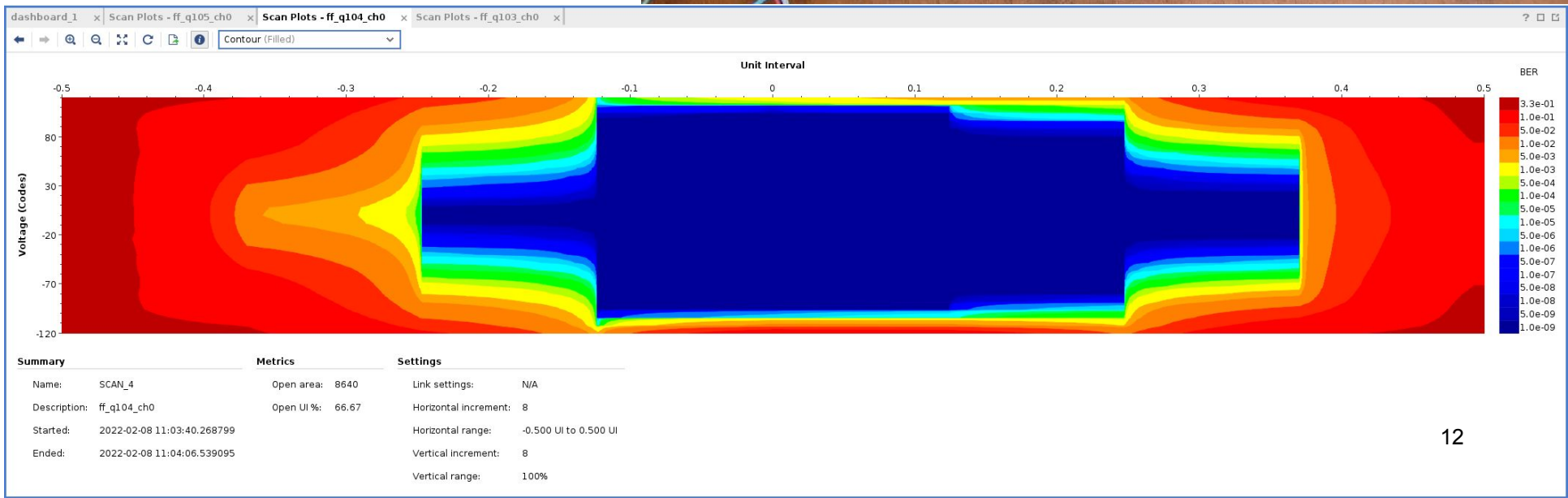
- 3x TMP435
  - Board and Versal die temperatures
- 11x INA226
  - Power rails
- 2x TCA6424 GPIO expander
  - FireFly's un-reset
- 4x SI570
- 2x SI5395
  - 390.625 MHz GTY ref. clocks
- LTM4700 DC/DC regulator VCCINT
- lpGBT ASIC

- Scripts for I2C:
  - Devices configuration
  - Power consumption
  - Thermal performances
- Vitis C bare-metal ARM Cortex-A72 apps
  - UART, DDR4, GbE
- PetaLinux 2021.2 → OS → Python3
  - modules
  - ssh server

14-Gb/s FireFly modules

- 24 loopback optical links (12 Tx + 12 Rx)
- 12.8 Gb/s, PRBS-31, BER < 1E-9 for IBERT EyeScan
- GTY quads 103-104-105, 106-205-206
- All links up and running error-free
  - BER < 1E-13

Link	Open area
q104_ch0	8640
q105_ch0	8640
q106_ch0	6848
q205_ch0	7360
q206_ch0	8000
AVG	7900



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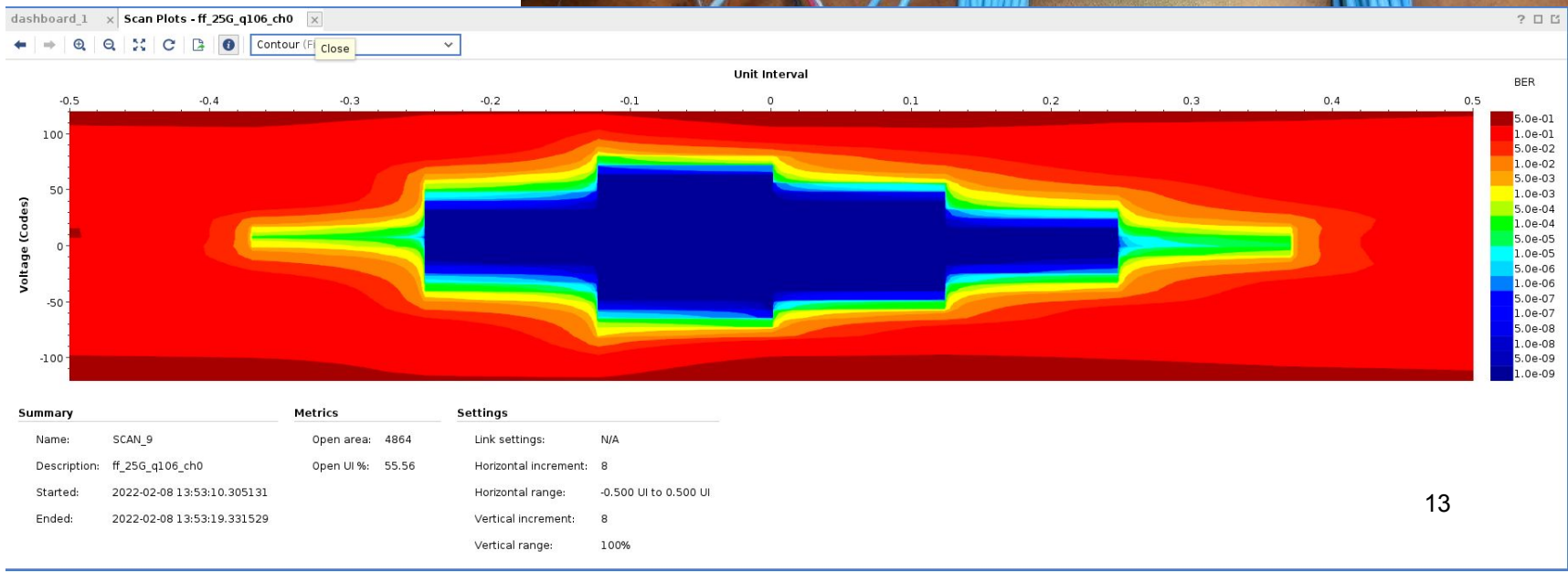
25-Gb/s FireFly modules

- Used 20-meter fiber loopback (no loopback module available)
- 25.8 Gb/s, PRBS-31, BER < 1E-9 for IBERT EyeScan
- All links up and running error-free
  - BER < 1E-13

Link	Open area
q106_ch0	4864
q205_ch0	5184
q206_ch0	6080
AVG	5380



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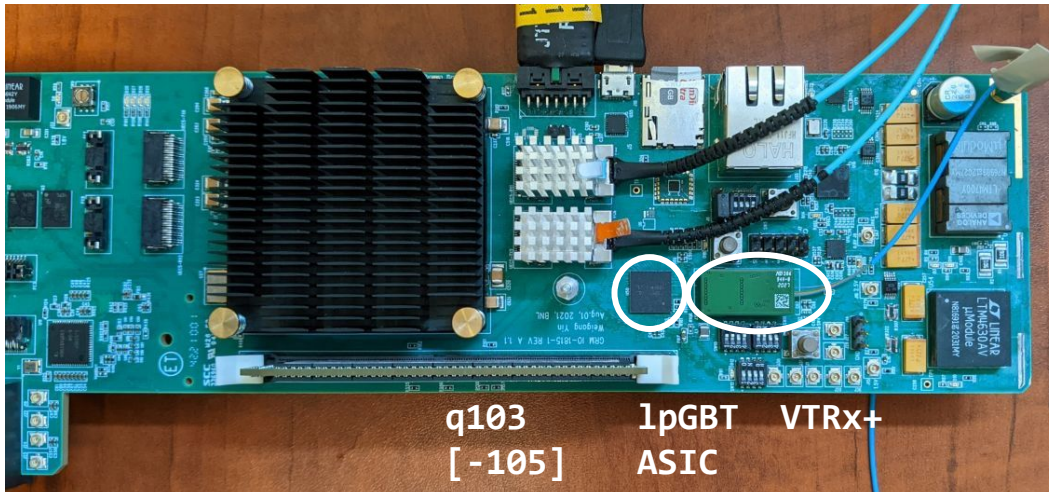
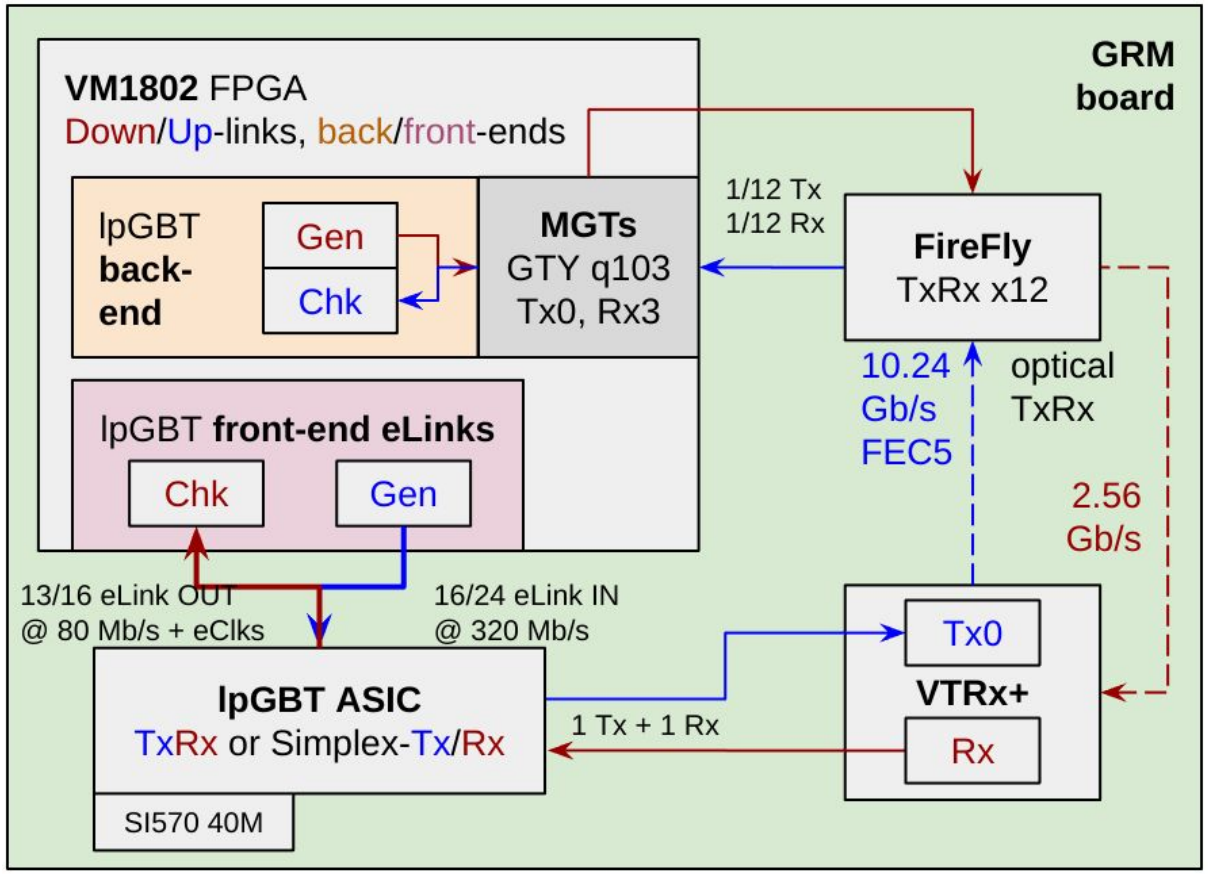
GRM lpGBT test-bench

- lpGBT
  - Low-Power Giga-Bit Transceiver for Emulation of detector front-end on GRM
  - Radiation-hard ASIC, protocols for front-end readout
- lpGBT configuration via I2C (VM1802 master) or IC/optics (FELIX)
- Send/Check lpGBT data on VM1802, through both uplink and downlink loopback via electrical links (eLinks) and optics on VTRx+/FireFly's
  - eLinks: lpGBT CLPS compatible with VM1802's LVDS
  - VTRx+ [Versatile Link PLUS, a radiation-hard optical transceiver]: high-speed asymmetrical (uplink Tx 10.24, downlink Rx 2.56 Gb/s) bidirectional optical links between the VTRx+ and FireFly



Testing lpGBT Uplink and Downlink

- Down-link
  - VM1802 PRBS data generated, encoded, scrambled
  - GTY → FireFly optical module @ 2.56 Gb/s
  - VTRx+ → lpGBT ASIC, decodes
  - Distributed to output eLinks (CLPS) → VM1802
  - VM1802 data is checked (with eClk).
- Up-link
  - VM1802 raw data generated
  - Sent to input eLinks (LVDS) → lpGBT, encodes
  - VTRx+ → FireFly optical looped-back @ 10.24 Gb/s
  - VM1802 decodes, descrambles and checks (with adaptation lpGBT-FPGA repo to Versal).



Conclusions

Conclusions

- ATLAS Global Trigger is a new firmware-focused project designed to meet new trigger requirements for the High-Luminosity runs of the Large Hadron Collider
- Global Trigger common hardware: GCM + GRM. Board design, fabrication, bring-up and testing is completed successfully for all functionalities
- Demonstrated Versal-lpGBT communication; both devices will play crucial roles in ATLAS TDAQ for a long time, so experience on GRM will be also valuable to other projects (e.g. upcoming GCMv3 and FELIX FLX-18* Phase-II hardware - poster)
  - Lessons learned in new Xilinx Versal family, several bugs reported and resolved 2022.1

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Backup

GRM bring-up completed

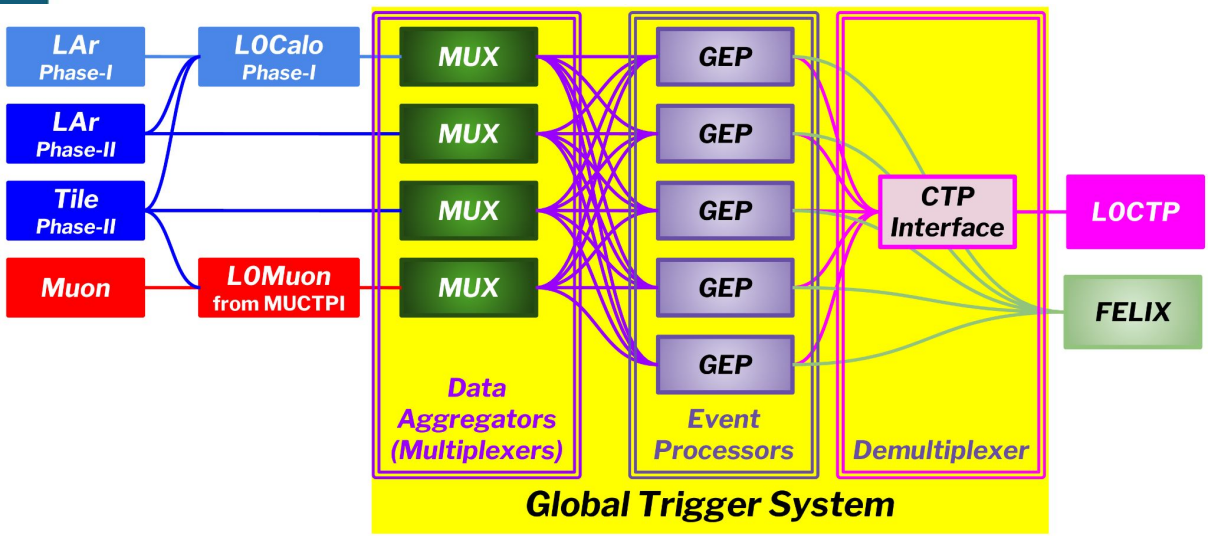
- **Power**
  - LTM DC/DC regulators and power rails
  - Ripple measures (Tektronix TPR4000)
  - Managing and sequencing (ADM1066)
  - MMC verification with ATCA IPMC (GCM via Zone3 conn.), hot-swap, [de]activation
- **Versal & interfaces**
  - PL, CIPS, NoC, DDRMC
  - PetaLinux build, OS boot
  - PS, I2C devices configuring and monitoring (bare-metal ARM-A72 C apps, Python3, kernel drivers devtree)
  - JTAG, UART, SD 3.0, GbE
- **Transceivers, FireFly's**
  - GTY transceivers
  - FireFly's 14-Gb/s
  - FireFly's 25-Gb/s (alpha)
  - IBERT 12.8 Gb/s, 25.78125 Gb/s
- **lpGBT**
  - I2C and IC regmap configuration
  - eLinks CLPS ⇔ LVDS
  - Up-link VM1802 loopback
  - Down-link VM1802 loopback
  - Clocks and Decoders locked correctly

Versal - Bugs / Lessons learned

- Vitis
  - Versal example application issues (GbE Echo server C source, missing libraries lwip, DDRMC not ready, …)
- Vivado
  - Versal design flow
    - IBERT integrated in GTY MGT wizard
  - Removed dynamic LPM/DFE switching
  - Multi-rate MGT IBERT
  - Glitches (menus, importing CIPS/NoC block design resets clocks, < 2400 MT/s Complex patterns in margin analysis absent, NoC IP instantiated as RTL component allowed, but should not - BD only)
- PetaLinux
  - PetaLinux does not mount full rootfs when boot INITRD images
  - Linux won’t boot if Inter Processor Interrupts are not enabled to A72

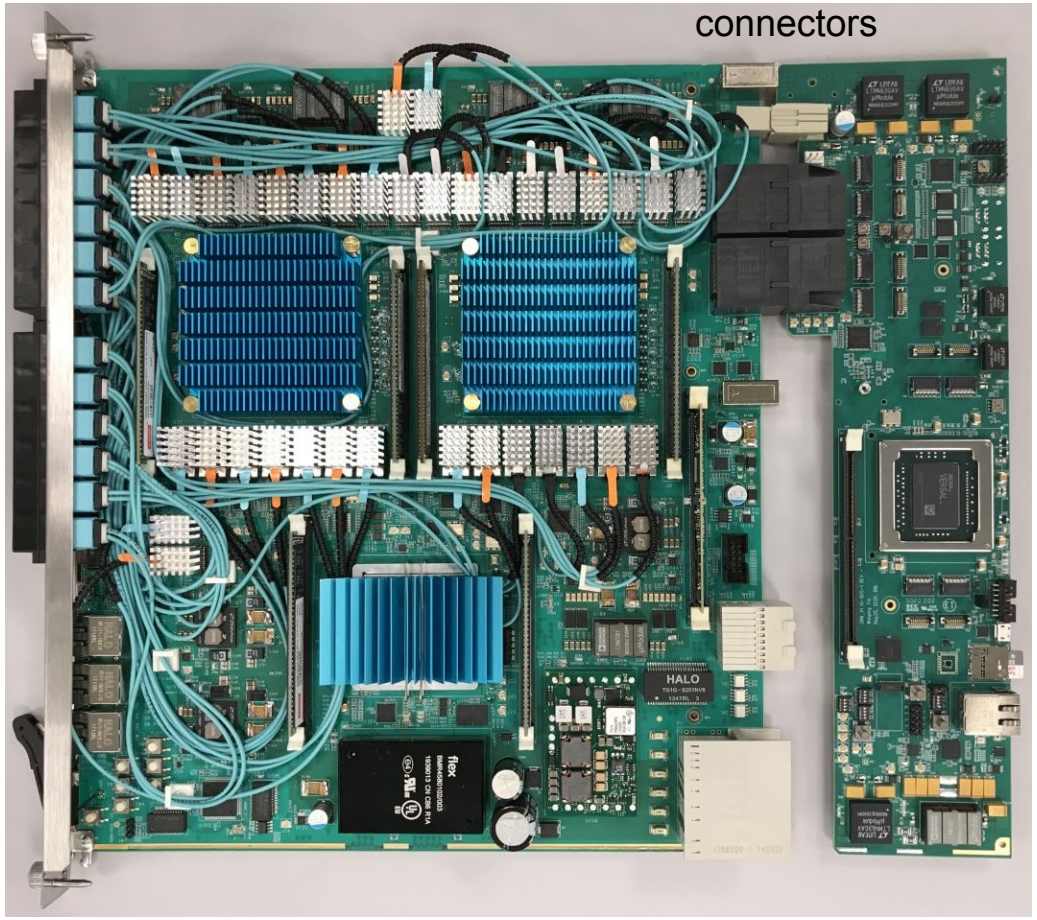
- Early Versal experience
  - Versal design flow
  - Versal-lpGBT interfacing

GCM ⇔ GRM



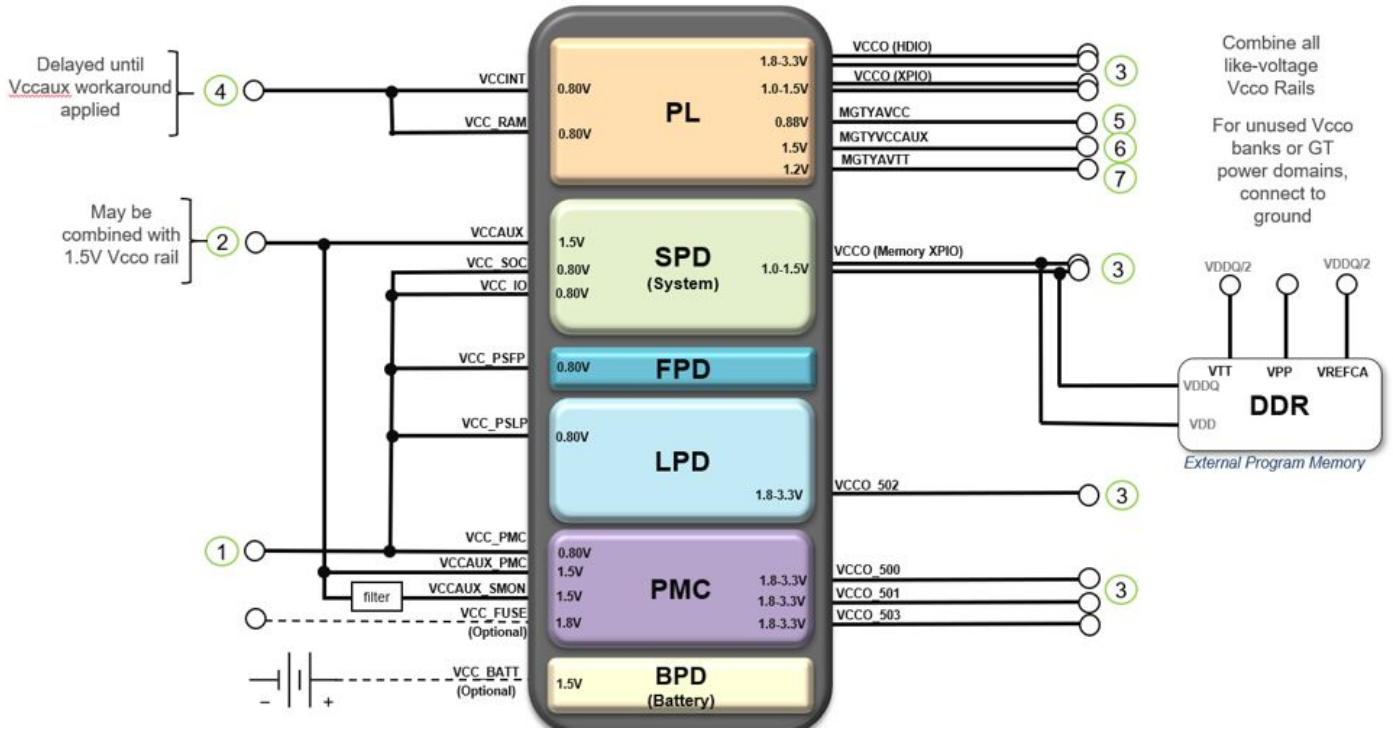
Zone3
connectors

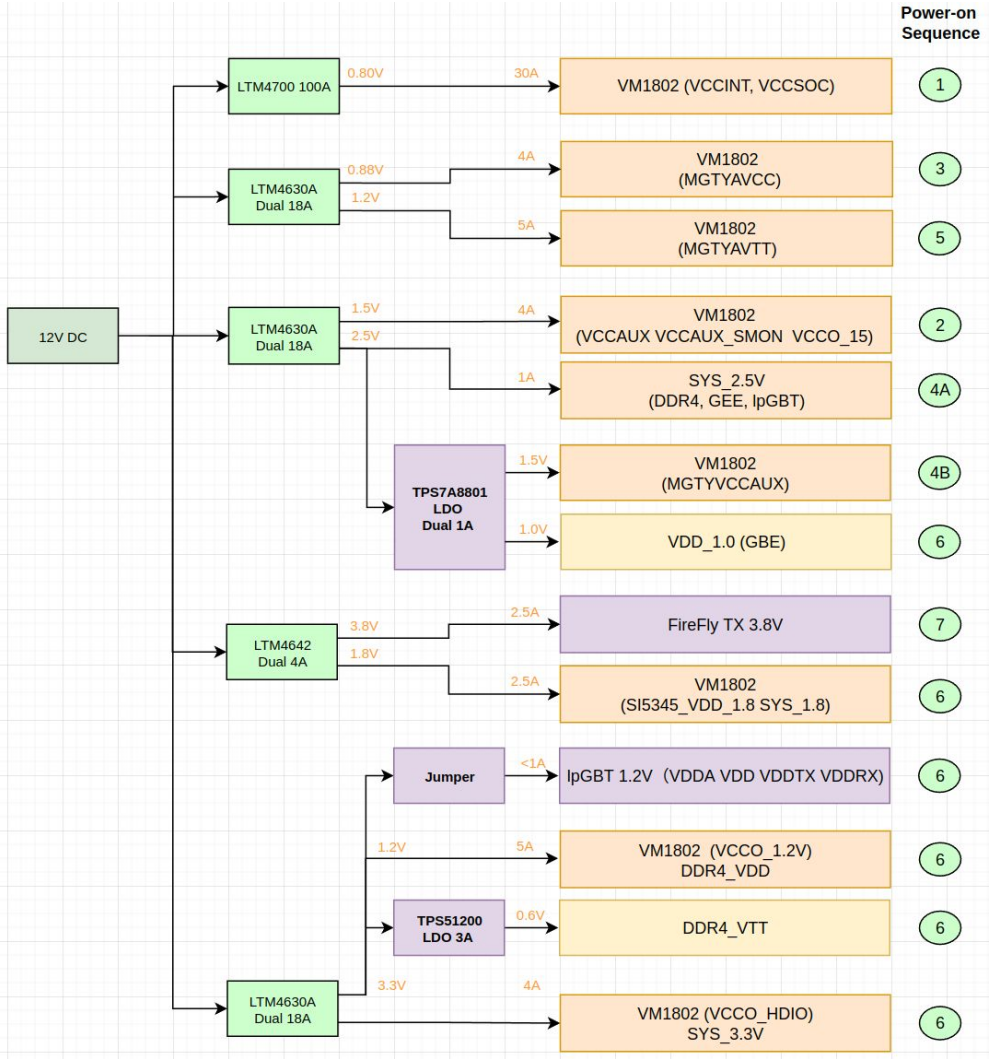
G
C
M



G
R
M

Versal power rails and sequencing





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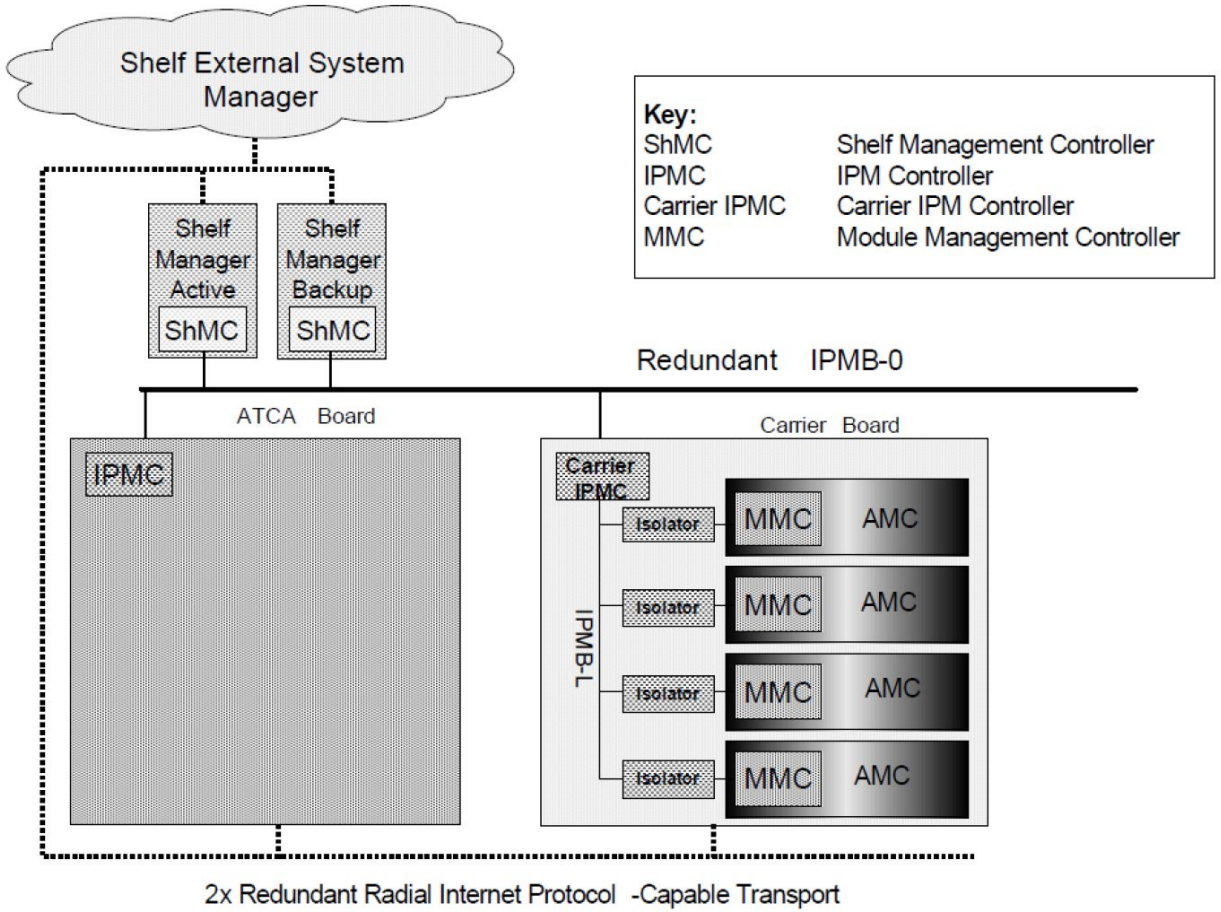
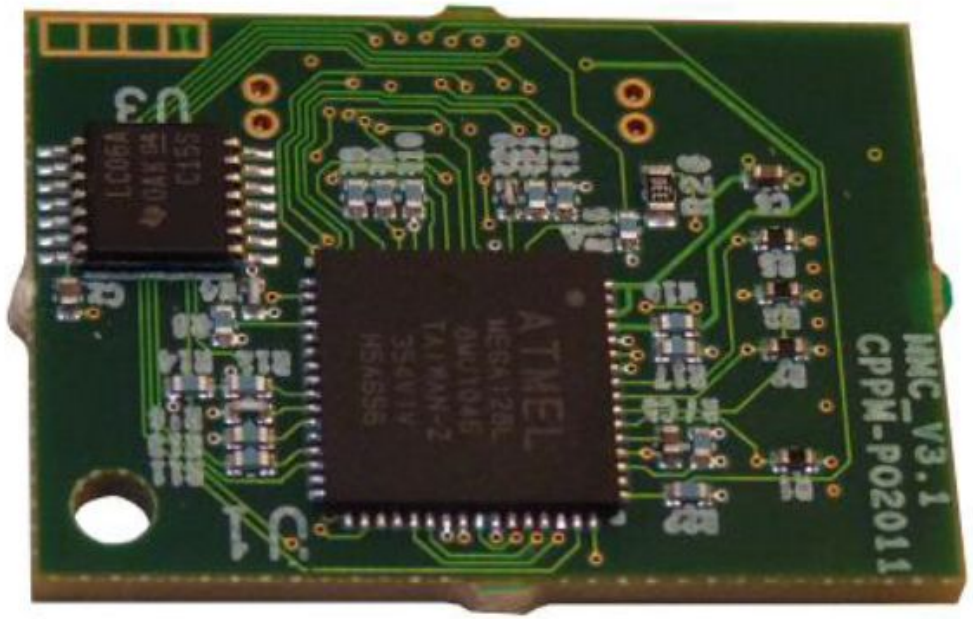
Voltage/V	Current Demand/A	Power/W	Description	Source
0.8	39.8	31.8	VCCINT	LTM4700
0.8	1.5	1.2	VCC_PMC	LTM4642
0.8	0.3	0.2	VCC_RAM	LTM4642
0.8	2.7	2.2	VCC_SOC	LTM4642
1.5	1.9	2.9	VCCAUX	LTM4642
0.88	3.7	3.3	MGTYAVCC	LTM4630A
1.2	4.2	5.0	MGTYAVTT	LTM4630A
1.2	5	6.0	SYS_1V2	LTM4630A
1.8	0.6	1.1	SYS_1V8	LTM4642
2.5	0.2	0.5	SYS_2V5	LTM4642
3.3	3.6	11.9	SYS_3V3	LTM4630A
0.6	0.75	1.0	DDR4_VTT	TPS51200 from SYS_1V2
1	0.1	0.1	VDD_1V0	TPS7A8801 from SYS_2V5
1.5	0.01	0.0	MGTYVCCAUX	TPS7A8801 from SYS_2V5

MMC: Module Management Controller

https://espace.cern.ch/ph-dep-ESE-BE-uTCAEvaluationProject/MMC_project/default.aspx





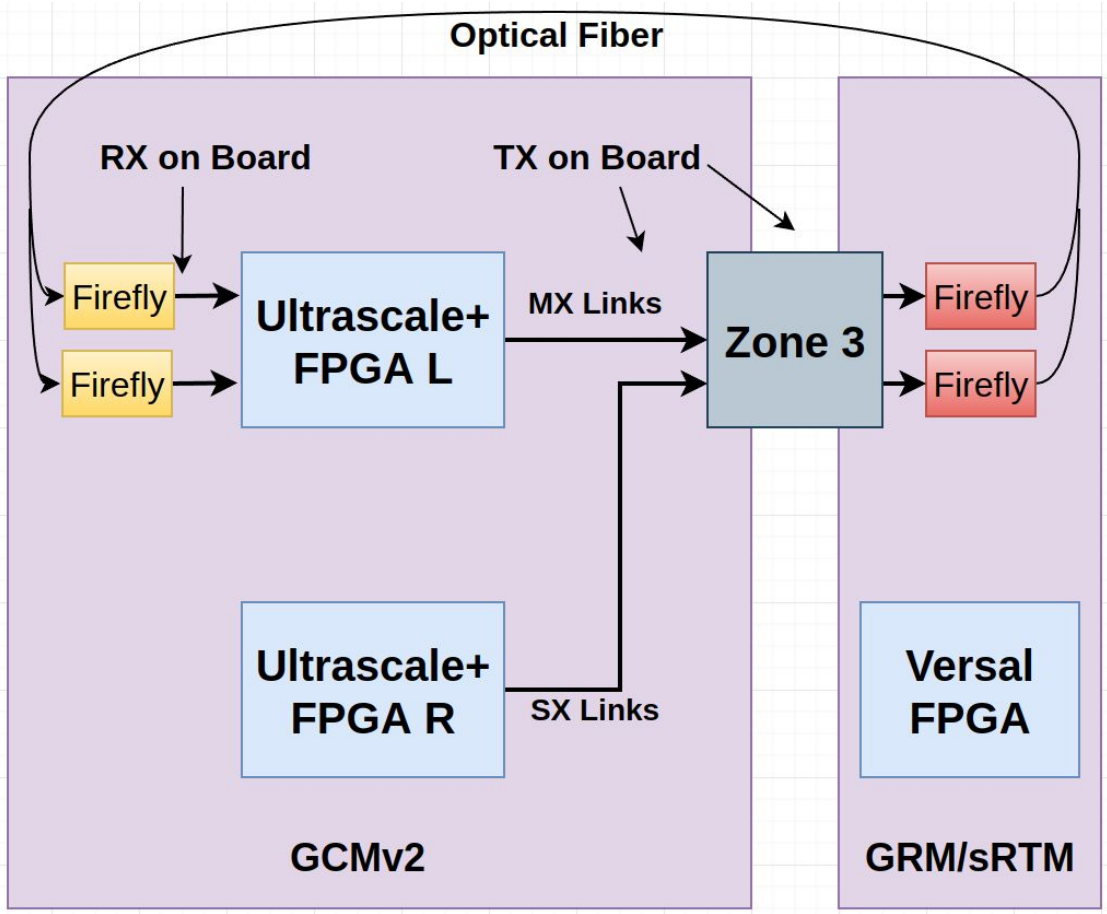
CERN MMC Mezzanine

- Sensor management by IPMC in GCM

Hardware Setup of IBERT Test GCM-GRM [Weigang]

- ***16 GTY TX links between GCM and GRM***
  - ❑ Source: Two big processor Ultrascale+ FPGAs on GCM (each FPGA has 8 links in bank 128 and 129) .
  - ❑ Path: Two Zone3 connectors between two boards.
  - ❑ Destination: TX FireFly modules on GRM
- ***RX side on GCM***
  - ❑ Optical fibers from GRM to GCM
  - ❑ Transceiver data is received by GCM FPGA via RX FireFly modules

- Links OK with 14-Gb/s modules IF custom emphasis/swing settings used
- Verify with 25-Gb/s FF modules?
- Now evaluate the performance of different electrical trace lengths at 25.8 Gb/s => high speed for RTMs!



Bare-metal and OS

- Vitis C bare-metal ARM Cortex-A72 apps
  - UART - “Hello world”
  - DDR4 - Memory tests
  - GbE - Echo server

    GRM⇔router⇔workstation

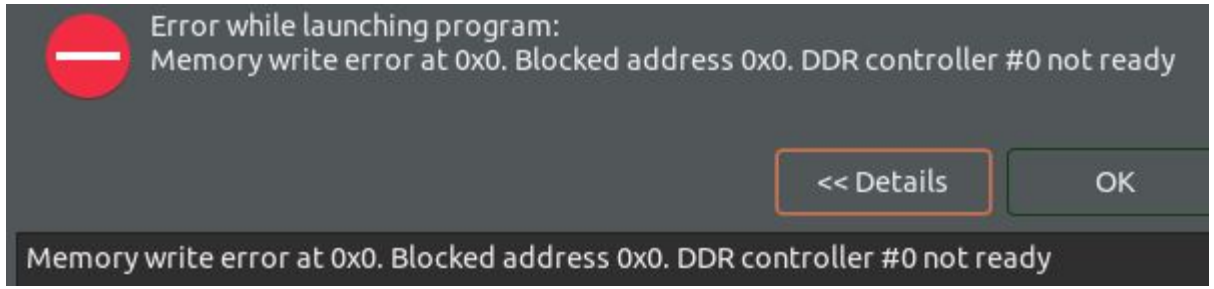
```
-----lwIP TCP echo server ------
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
link speed for phy address 1: 1000
Board IP: 192.168.1.101
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7
```

- Linux OS
  - PetaLinux 2021.2 → 2022.1
  - Device tree (GbE PHY, INA226, SI570 kernel drivers)
  - SSH server
  - python3 modules (e.g. periphery)
  - ntp, git, i2c-tools, …

```
root@2021:~# cat /sys/bus/iio/devices/iio\:device0/name
xlnx,versal-sysmon
root@2021:~# cat /sys/bus/iio/devices/iio\:device0/in_temp160_temp_input
41.546875000
root@2021:~# cat /sys/bus/iio/devices/iio\:device1/name
ina226
root@2021:~# cat /sys/bus/iio/devices/iio\:device1/in_voltage*_scale
0.002500000
1.250000000
root@2021:~# cat /sys/bus/iio/devices/iio\:device1/in_shunt_resistor
0.000500000
root@2021:~#
```

DDRMC-NoC Config. 72-bit (ECC)

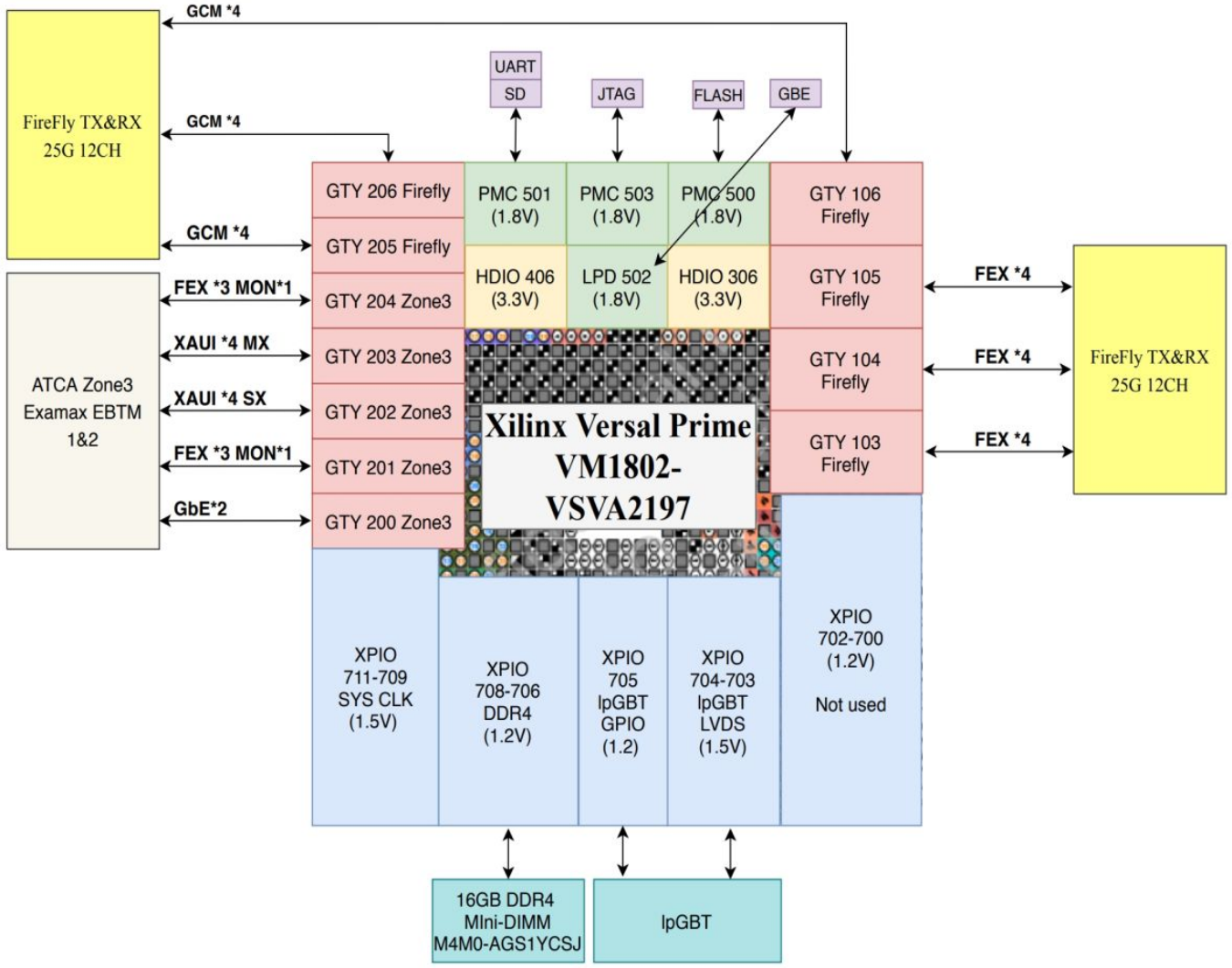
- Device type == UDIMM, 2-ranks 16GB
- Vivado HW Manager - DDRMC
  - PASS, GOOD
- Vitis DDR Memory Test Example Application
  - Successful, LOW0,1




```
[1972.808]Total PLM Boot Time
--Starting Memory Test Application--
NOTE: This application runs with D-Cache disabled.
As a result, cacheline requests will not be generated
Testing memory region: axi_noc_0_C0_DDR_LOW0
    Memory Controller: axi_noc_0
          Base Address: 0x0
                  Size: 0x80000000 bytes
           32-bit test: PASSED!
           16-bit test: PASSED!
            8-bit test: PASSED!
[...]
Testing memory region: axi_noc_0_C0_DDR_LOW1
    Memory Controller: axi_noc_0
          Base Address: 0x800000000
                  Size: 0x80000000 bytes
           32-bit test: PASSED!
           16-bit test: PASSED!
            8-bit test: PASSED!
[...]
Testing memory region: axi_noc_0_C3_DDR_LOW1
    Memory Controller: axi_noc_0
          Base Address: 0x800000000
                  Size: 0x80000000 bytes
           32-bit test: PASSED!
           16-bit test: PASSED!
            8-bit test: PASSED!
Testing memory region: versal_cips_0_pspmc_0_psv_pmc_ram_psv_pmc_ram
    Memory Controller: versal_cips_0_pspmc_0_psv_pmc_ram
          Base Address: 0xF2000000
                  Size: 0x20000 bytes
           32-bit test: PASSED!
           16-bit test: PASSED!
            8-bit test: PASSED!
--Memory Test Application Complete--
Successfully ran Memory Test Application
```

Internal loopback (Near-End PMA)

- All links up and running error-free for >10’
  - `GTY_q103_q104_q105`, REFCLK0
  - `GTY_q106_q206_q205`, REFCLK1
  - `GTY_q200_q201_q204`, REFCLK1
  - `GTY_q202_q203`, REFCLK0
    - 1.21A, 43 degC



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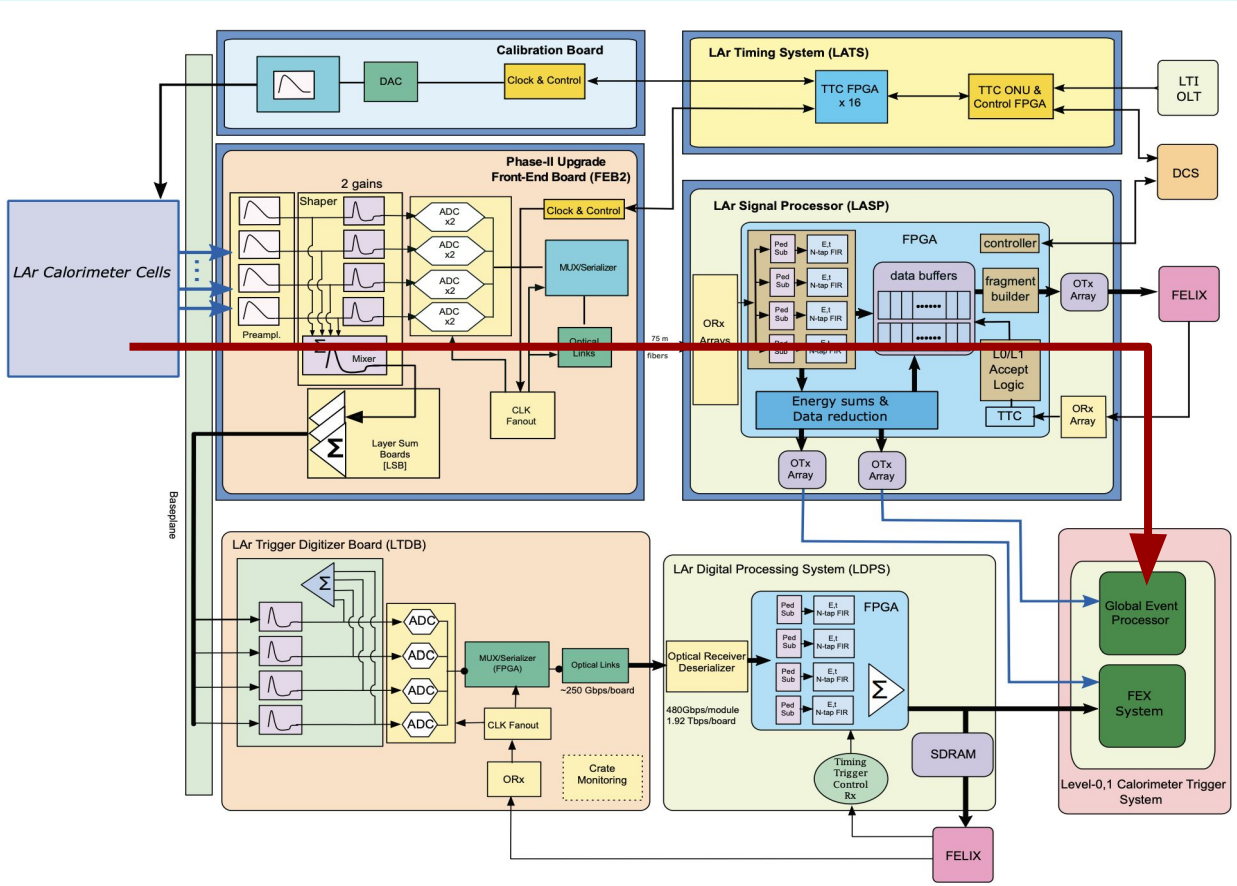
lpGBT

Low-Power Giga-Bit Transceiver

for detector front-end emulation



CLPS / LVDS [Weigang]

- CLPS's driving current and Amplitude are compatible with LVDS
  - Up to 1.28Gbps, Vcm=600mV, Vcco=1.2V
  - Driving current: 1 to 4 mA in 0.5 mA steps
- Vcm of CLPS and LVDS are not same
  - **CLPS's TX to LVDS's RX**
    - CLPS's Vcm TX 0.6V (0.43-0.77V)
    - LVDS's Vcm RX = 1.2V (DC 0.3-1.425V) from DS923
    - CLPS's TX can be connected to LVDS's RX directly
  - **LVDS's TX to CLPS's RX**
    - LVDS Vcm TX = 1.2V (1.0-1.425V) from DS923
    - CLPS's Vcm RX 0.6V (0.07-1.2V)
    - LVDS's TX should be compatible with CLPS's RX

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF}[2]	Differential output voltage: (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}[2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}[3]	Differential input voltage: (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High		100	350	600[3]	mV
V_{ICM_DC}[4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V
V_{ICM_AC}[5]	Input common-mode voltage (AC coupling)		0.600	–	1.100	V

eRX differential receiver

Parameter	Description	Min	Nom	Max	Units
V_{DD}	Supply voltage range	1.08	1.2	1.32	V
I_{DD}	Average current consumption		850		µA
V_{CMRX}	Common-mode voltage range[A]	70	600	1200	mV
V_{CM}	Common-mode set voltage[B]		V_{DD}/2		
$\|V_{ID}\|$	Differential voltage[C]	140	200	450[E]	mV
V_{IDTH}	Differential input[C] high threshold			70	mV
V_{IDTL}	Differential input[C] low threshold	-70			mV
V_{IH}	Single-ended input high voltage		700	V_{DD}+200	mV
V_{IL}	Single-ended input low voltage	-40	500		mV
Z_{ID}	Differential input impedance	80	100	125	Ω
J_R	Random noise jitter			10[F]	ps rms
J_{PW}	Pattern or pulse width dependent jitter[D]			10[F]	ps
$T_{R/F}$	Output rise/fall time		30		ps
PSR	Power supply rejection			10[F]	ps/100mV
CMR	Common mode rejection			10[F]	ps/100mV

eTX differential driver

Parameter	Description	Min	Nom	Max	Units
V_{DD}	Supply voltage range	1.08	1.2	1.32	V
V_{CMTX}	Common-mode voltage[A,B]	430	600	770	mV
$\|\Delta_{VCMTX(1,0)}\|$	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV
$\|V_{OD}\|$	Differential voltage[B,C]	140	200	270	mV
$\|\Delta V_{OD}\|$	VOD mismatch when output is Differential-1 or Differential-0			10	mV
V_{OH}	Single-ended output high voltage[B]		700	900	mV
V_{OL}	Single-ended output low voltage[B]	300	500		mV
I_{MOD}	Modulation output current [D]	0.7	1 to 4	5.4	mA
I_{PRE}	Pre-emphasis output current [D]	0.7	1 to 4	5.4	mA
Z_L	Load impedance		100		Ω

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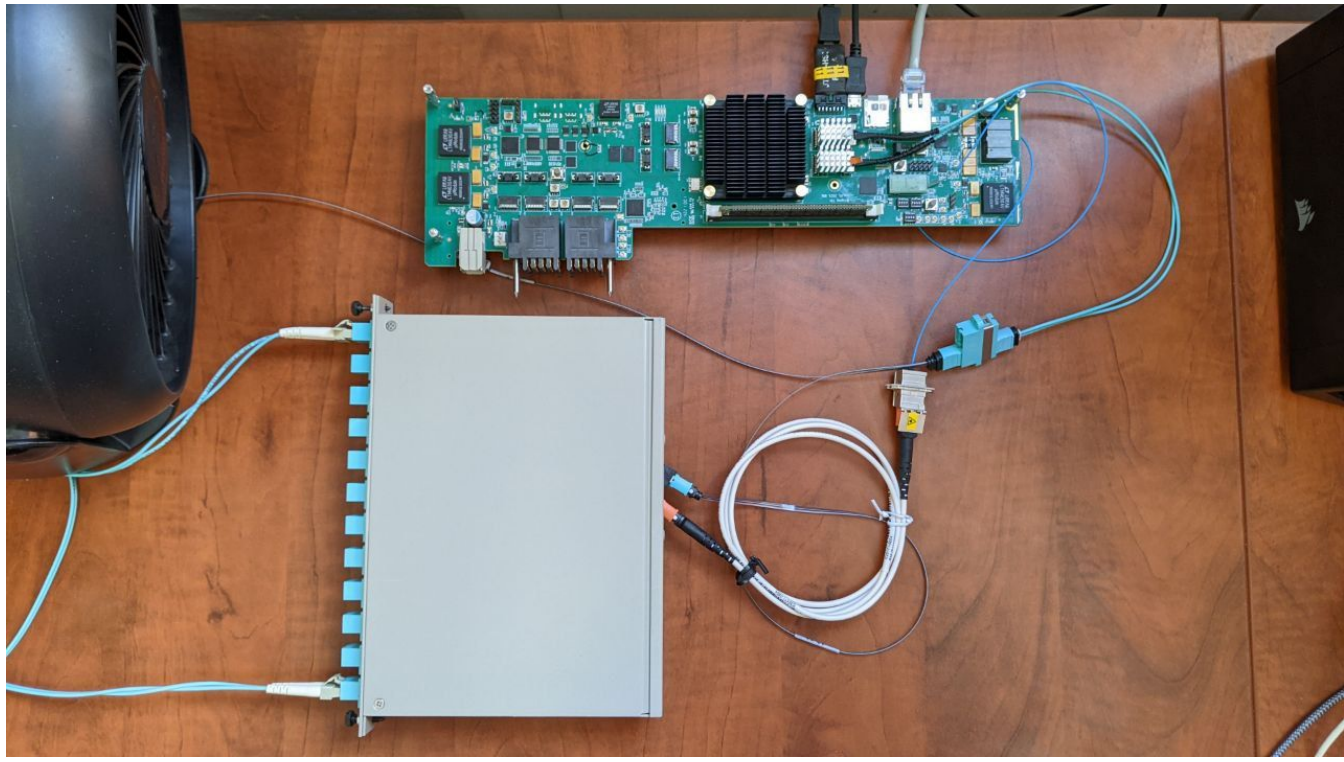
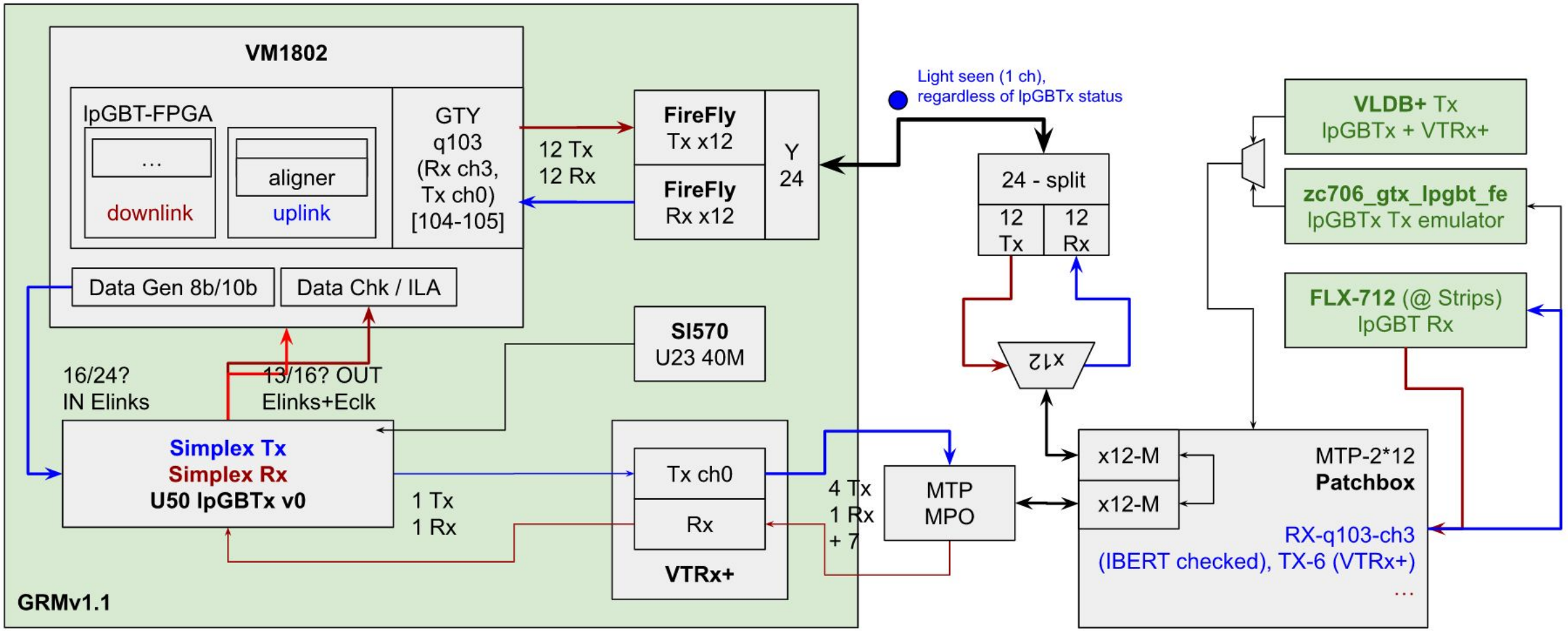
Configuration: Registers

Generate and export register file from pigbt.web.cern.ch

- EP-RX-160M: # EDIN [5.12 Gb/s, FEC12] = 16 (connected)/24 @ 160 Mb/s (320 Mb/s for 10.24 Gb/s)
- EP-TX-80M: # EDOUT = 13/16 @ 80 Mb/s
- ECLK: 40 MHz, 2.5 mA
- TxRx-EC on (No need IC/EC for now)
- TxSwapP/N (schematics)
- GPIO (testing)
- Elinks IN phase adj.



Test-bench: Uplink / Downlink



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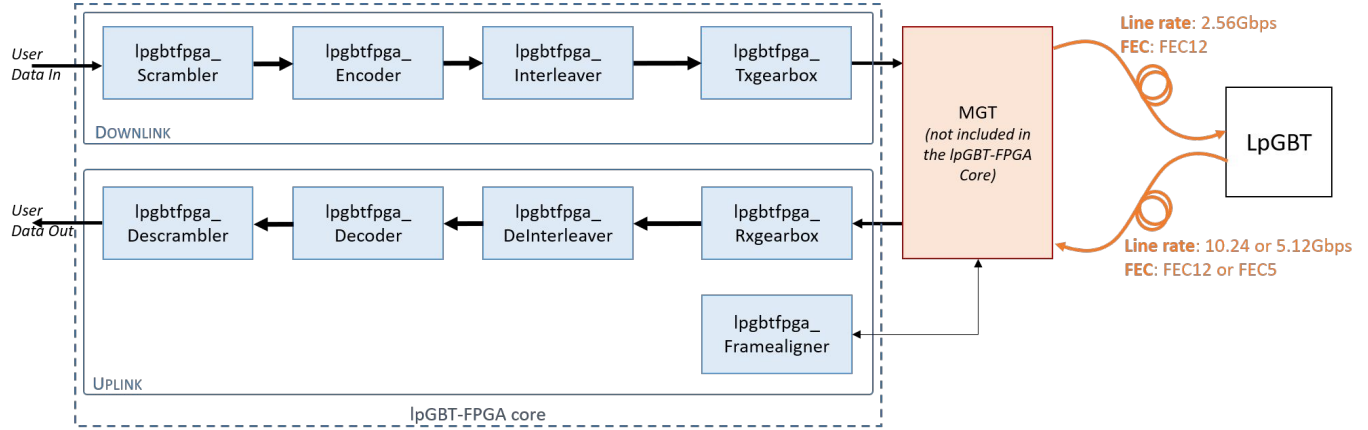
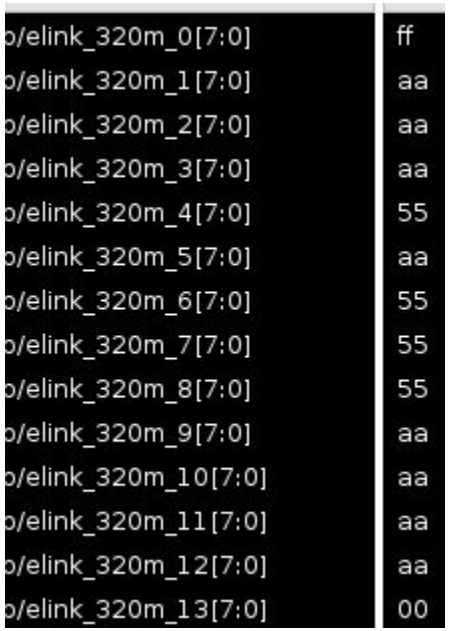
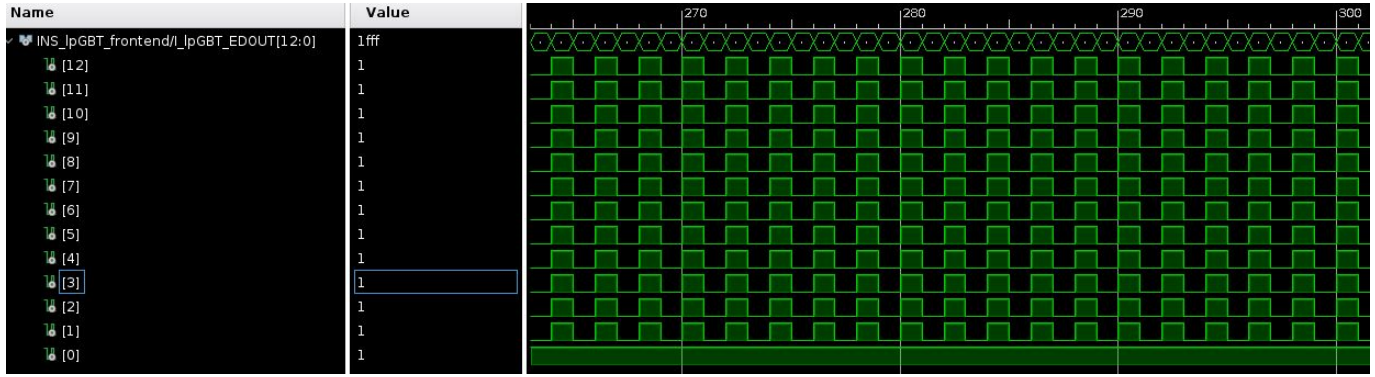
- eLink Data IN
- eLink Data OUT
- lpGBT-FPGA top-level







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