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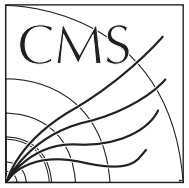

The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

27 July 2022 (v4, 29 July 2022)

The DAQPATH readout system of the Serenity boards for the CMS Phase-II Upgrade

Paolo Prosperi and Guido Magazzú for the CMS Collaboration

Abstract

The Serenity boards are ATCA custom boards used in the readout of the Phase-II CMS detector. Each board can handle up to 144 optical serial links (up to 25Gb/s each) and supports up to two high-performance FPGAs. In several applications the Serenity board is required to aggregate raw events (FE data) from the detector at every L1 accept and route this event fragment to the central DAQ system. The architecture and behavior of the DAQPATH firmware that collects and merges FE data and manages their transmission to the DAQ system over 25Gb/s output optical links are here described.

Presented at *15th Pisa Meeting 2022 15th Pisa Meeting on Advanced Detectors*

The DAQPATH readout system of the Serenity boards for the CMS Phase-II Upgrade

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Abstract

The Serenity boards are ATCA custom boards used in the readout of the Phase-II CMS detector. Each board can handle up to 144 optical serial links (up to 25Gb/s each) and supports up to two high-performance FPGAs. In several applications the Serenity board is required to aggregate raw events (FE data) from the detector at every L1 accept and route this event fragment to the central DAQ system. The architecture and behavior of the DAQPATH firmware that collects and merges FE data and manages their transmission to the DAQ system over 25Gb/s output optical links are here described.

Keywords: ATCA, CMS, DAQ, FPGA, FW, FSM

1. DAQPATH firmware application

The Serenity board (Figure 1) has been developed for the Phase-II upgrade of the CMS experiment at the CERN LHC. It is a carrier board that can house either one or two mezzanine cards with high performance FPGAs (Xilinx Virtex or Kintex Ultrascale+ devices) and that can handle up to 144 serial optical links (up to 25Gb/s each). It can be seen as a data engine that allows high data throughput (up to 5TBps per carrier board) and suitable for different sub-detectors by design. The firmware developed for the Serenity FPGAs is compatible with a flexible firmware framework, the Extensible Modular data Processor (EMP), which allows for algorithm development that does not depend on the underlying infrastructure and FPGA type .[1]

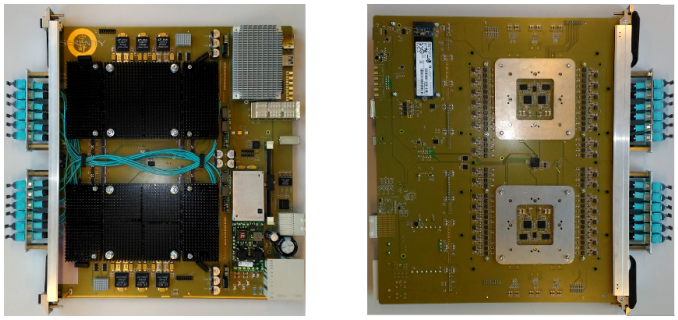

Figure 1: Serenity carrier card.

For detector-facing Serenity boards, DAQ data from the FE links are received upon every L1 accept and decoded by FE interface blocks. DAQ data packets and associated information are temporarily stored into input channels' buffers. The goal of the DAQPATH is to collect and merge these FE data and to manage their transmission to the DAQ system (see Figure 2). In certain applications, the DAQPATH is also used to collect, merge and transmit trigger data which is associated to the incoming L1 trigger and temporarily stored into local latency buffers. These data are used for monitoring and data quality purposes. The DAQPATH firmware has to be a very flexible and modular block in order to be used for the transmission to DAQ system of several types of event data packets from a given number of input channels to a different (lower) number of output channels.

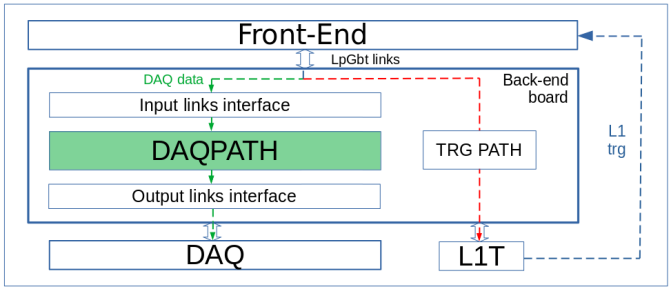

Figure 2: FE data management in BE boards.

2. DAQPATH firmware description

The architecture of the DAQPATH firmware is based on a main Finite State Machine (FSM) that controls a "token" ring chain of N channel blocks (N is the number of the input channels). The main FSM starts the sequential readout of the channels when all of the input buffers of all channels, containing data for transmission to DAQ and associated information as packet ID and length, are not-empty. In each channel block, the effective readout of the input buffers is performed by a specific FSM, and a multiplexing logic selects the output data in order to propagate data in the channels' chain and merge data from all the channels into packets feeding the 25 Gb/s output link interface. In Figure 3, additional details are provided in

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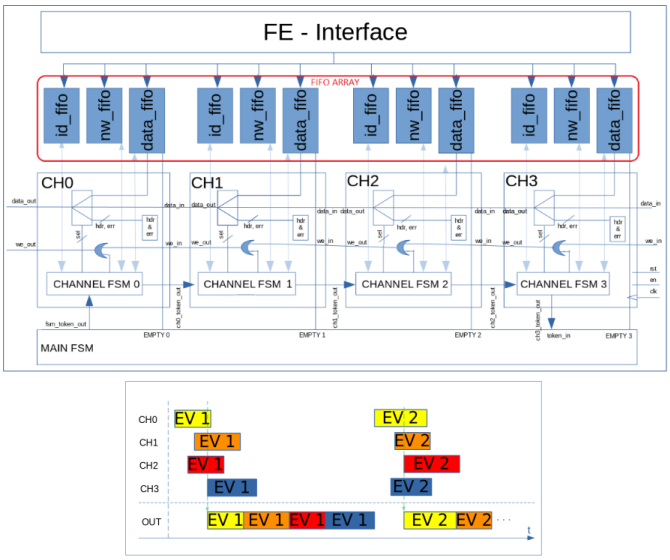

Figure 3: DAQPATH firmware architecture and data timing. id_fifo stores the ID information, nw_fifo the number of words and data_fifo the data words of incoming event.

the case of a a simplified architecture with four input channels. The timing diagram shows how output data packets are created from input ones.

The DAQPATH system has a modular and parametric structure: each DAQPATH module feeds one output link with data, from a programmable number of input channels with a programmable words' width. As a result, there may be as many DAQPATH modules as output links to DAQ. Due to the high number of input channels and their distribution on the FPGA floor-plan the channels' chain is pipelined to meet timing requirements.

3. DAQPATH firmware tests and results

A first version of the DAQPATH firmware (v1.0) has been validated with functional simulations in Vivado (Figure 4, panel A) and with hardware tests on Serenity boards Xilinx Ultrascale+ FPGAs. The core logic, including the DAQPATH, runs at a 360MHz target clock frequency.

Hardware tests used IPBus buffers (i.e FIFOs accessible via IPBus protocol - Figure 4, panel B) to be able to interact with the firmware by loading some specific data pattern with specific timing into input IPBus buffers and by reading data directly from output IPBus buffers. Tests with input data from FE modules to IPBus output buffers and with data from IPBus input buffers to DAQ boards (Figure 4, panel C) are on-going. Full chain tests (i.e. data from FE to DAQ system - Figure 4, panel D) are foreseen in the near future.

In Figure 5, the FPGA floor-plan of two different projects including DAQPATH and targeting two different numbers of input channels (4 and 32) are shown. The utilisation of Configurable Logic Blocks (CLBs) in the DAQPATH module obviously depends on the number of channels and scales up with it, but the main logic blocks of the DAQPATH are very inexpensive in

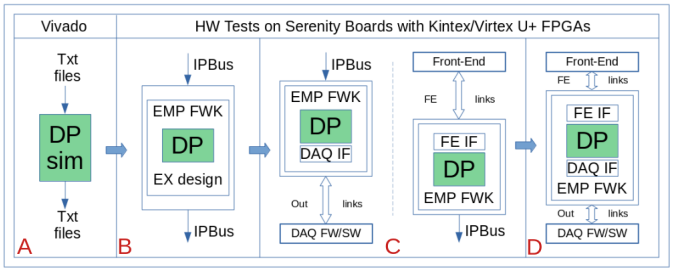

Figure 4: Design validation and development flow: test structures.

utilised resources and the major contribution to the utilisation is given by RAMs and buffers.

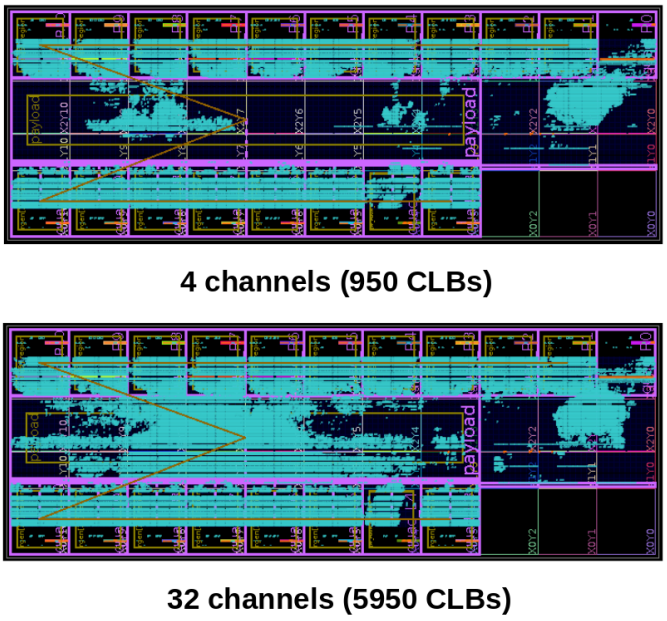

Figure 5: Floor-plans including DAQPATH on a KU15P Kintex Ultrascale+ device.

4. Conclusions

The DAQPATH firmware that collects and merges FE data on detector-facing serenity boards and manages their transmission to the DAQ system over output optical 25Gb/s links has been developed and tested in its first (v1.0) version. A pipelined token ring architecture with a main control logic FSM has been chosen for the DAQPATH firmware module. The version v1.0 will be available soon as a tool-kit for users within EMP framework official repository and a second version, with several upgrades and added features to improve flexibility and reliability has been already preliminary tested.

References

[1] Serenity CERN site at https://serenity.web.cern.ch/serenity (Last accessed 23rd Jul 2022).