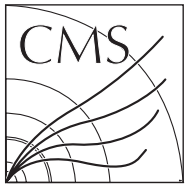
Available on CMS information server

CMS CR -2022/088



The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

22 June 2022 (v3, 10 August 2022)

The front-end electronics upgrade of the CMS ECAL barrel

Fabio Cossio for the CMS Collaboration

Abstract

The barrel part of the CMS electromagnetic calorimeter (ECAL) consists of 61200 $PbWO_4$ crystals coupled to avalanche photodiodes (APDs). A decrease of the ECAL operating temperature from 18° C to 9° C is needed to mitigate the increase in APD noise from radiation-induced dark current in the conditions of the high luminosity upgrade of the LHC. Moreover, a full re-design of the front-end electronics has been undertaken in order to deal with the increase of pileup events and to improve the rejection of anomalous signals generated from direct interaction with the APDs. The VFE (very front-end) card will be equipped with two new ASICs: a fast trans-impedance amplifier named CATIA as well as a data conversion and compression ASIC named LiTE-DTU. The VFE will interface with the radiation tolerant LpGBT transceiver and the VTRx+ optical board, while trigger primitive generation will be moved off-detector to FPGA-based processors. The CATIA ASIC has a single input and two differential outputs with different gains in order to have better resolution for low energy signals. CATIA is designed in commercial CMOS 130 nm technology and can be controlled via an I2C interface. The LiTE-DTU ASIC embeds two 12-bit 160 MS/s ADCs, a sample selection logic, a lossless compression digital logic, and a 1.28 Gb/s serializer that will directly interface with the LpGBT e-links. LiTE-DTU is designed in commercial CMOS 65 nm technology. It embeds a PLL for the generation of the low jitter 1.28 GHz clock required by the ADCs and the serializer. Both ASICs have been extensively tested in lab and beam tests. This new system has been verified to fulfill the requirements of the experiment in terms of performance and radiation tolerance. The ASICs are now in the pre-production phase.

Presented at *15th Pisa Meeting on Advanced Detectors (22-28 May 2022)*

The front-end electronics upgrade of the CMS ECAL barrel

Fabio Cossio*

Istituto Nazionale di Fisica Nucleare, Sez. di Torino, Via P. Giuria 1, 10125 Torino, TO, Italy

For the CMS Collaboration

Abstract

The barrel part of the CMS electromagnetic calorimeter (ECAL) consists of 61200 $PbWO_4$ crystals coupled to avalanche photodiodes (APDs). A decrease of the ECAL operating temperature from 18°C to 9°C is needed to mitigate the increase in APD noise from radiation-induced dark current in the conditions of the high luminosity upgrade of the LHC. Moreover, a full re-design of the front-end electronics has been undertaken in order to deal with the increase of pileup events and to improve the rejection of anomalous signals generated from direct interaction with the APDs. The VFE (very front-end) card will be equipped with two new ASICs: a fast trans-impedance amplifier named CATIA as well as a data conversion and compression ASIC named LiTE-DTU. The VFE will interface with the radiation tolerant LpGBT transceiver and the VTRx+ optical board, while trigger primitive generation will be moved off-detector to FPGA-based processors. The CATIA ASIC has a single input and two differential outputs with different gains in order to have better resolution for low energy signals. CATIA is designed in commercial CMOS 130 nm technology and can be controlled via an I2C interface. The LiTE-DTU ASIC embeds two 12-bit 160 MS/s ADCs, a sample selection logic, a lossless compression digital logic, and a 1.28 Gb/s serializer that will directly interface with the LpGBT e-links. LiTE-DTU is designed in commercial CMOS 65 nm technology. It embeds a PLL for the generation of the low jitter 1.28 GHz clock required by the ADCs and the serializer. Both ASICs have been extensively tested in lab and beam tests. This new system has been verified to fulfill the requirements of the experiment in terms of performance and radiation tolerance. The ASICs are now in the pre-production phase.

Keywords: HL-LHC, CMS, Calorimetry, LHC upgrades, Phase-2 upgrade, Front-end electronics

1. Introduction

The electromagnetic calorimeter (ECAL) of the Compact Muon Solenoid (CMS, [1]) detector plays an important role in the physics program of the experiment for the identification and reconstruction of photons and electrons. The ECAL is a compact, hermetic, homogeneous, high-granularity electromagnetic calorimeter, made of 75,848 $PbWO_4$ scintillating crystals, distributed in a central cylindrical barrel (EB) and two endcap disks (EE). The EB covers the central rapidity region, up to $|\eta| = 1.48$, and it is read out by avalanche photo-diodes (APDs), while the EE allows the detection of incident particles up to $|\eta| = 3.0$ and is read out by vacuum photo-triodes (VPTs).

The upcoming LHC upgrade to High Luminosity LHC (HL–LHC) foresees to operate the accelerator at an instantaneous luminosity as high as $7.5{\times}10^{34}$ $cm^{-2}s^{-1}$ from 2029, delivering an integrated luminosity up to 4500 fb^{-1} over about 12 years of operations, with up to 200 concurrent interactions per LHC bunch crossing (pileup) [2]. In order to maintain the present performance of ECAL in the harsh radiation environment of LHC Phase-2, several upgrades are required [3].

*Corresponding author

Email address: fcossio@to.infn.it (Fabio Cossio)

2. The ECAL upgrade for HL-LHC

The HL-LHC conditions pose a significant challenge to both detector and electronics performance. On the one hand, the currently installed crystals, APDs and motherboards of the EB will be retained. The aging of the crystals, which causes a loss of their transparency as well as increased leakage currents in the APDs, will be mitigated by lowering the operating temperature from 18°C to 9°C. On the other hand, the transparency loss in the EE is expected to be sufficiently large that they will be replaced with a completely new and different detector, the high-granularity calorimeter (HGCAL, [4]).

The Phase-2 trigger requirements are the main reason for the EB electronics upgrade: this includes an increased trigger latency from about 4.5 μs to a maximum of 12.5 μs and a Level-1 (L1) trigger rate of about 750 kHz compared to the current 100 kHz [5]. In addition, the L1 trigger granularity has been enhanced from 5x5 crystal sums to using the single crystal information.

3. The new ECAL front-end electronics

Fig. 1 shows a block diagram of the new readout electronics. The upgraded front-end includes an analog ASIC, called

CATIA (CAlorimeter Trans-Impedance Amplifier), comprising a dual-gain TIA with 35 MHz bandwidth, and a digital ASIC, called LiTE-DTU (LIsbon-Turin Ecal Data Transmission Unit), featuring two 12-bit ADCs sampling at 160 MHz, with gain selection, data compression and transmission.

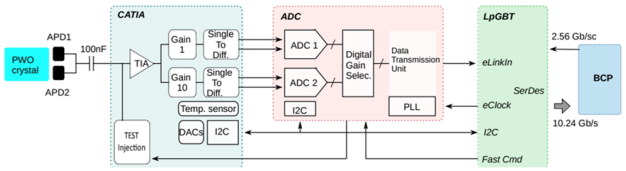


Figure 1: Scheme of the new ECAL readout electronics for the Phase 2 upgrade.

The TIA choice preserves the fast pulse shape of the APD signals and it is thus more resilient to noise increases due to the radiation-induced APD leakage current. This improvement will also provide better capability in rejecting signals generated by particles hitting the APD directly (spikes), which have a faster rise time and shorter duration compared to the scintillation light signals. CATIA is designed in a 130nm CMOS process and features two differential outputs, with x1 and x10 gain, to ensure a good energy and time resolution for the whole dynamic range of signals up to 2 TeV [6].

To take full advantage from the improved preamplifier performance, its output signals are sampled at 160 MS/s (i.e. four times the current sampling rate) with two 12-bit ADCs which have been designed by a commercial company and embedded in the LiTE-DTU chip. This ASIC includes also a time window based sample gain selection, to select and transmit only the highest non-saturated gain channel of CATIA, and a lossless data compression algorithm, to cope with the increased data rate [7]. An on-chip PLL provides the 1.28 GHz clock required by the ADCs and the serializers from the 160 MHz master clock. The LiTE-DTU has been designed in a commercial CMOS 65 nm technology and to be radiation tolerant to a dose up to 20 kGy and resistant to single event upsets.

The LiTE-DTU is connected to the lpGBT [8] optical transceiver to send single crystal data sampled at 160 MS/s to the off-detector electronics, where the L1 trigger primitives are generated with powerful, commercially available FPGAs. This new design, with faster analog electronics and increased sampling rate, will provide precision timing measurements, with a resolution of about 30 ps for photons and electrons above 50 GeV, while using the existing crystals and APDs. This will improve the overall CMS physics performance by disentangling pileup events.

A test beam, using prototype versions of CATIA and LiTE-DTU, was carried out in October 2021 at CERN with a 5x5 crystal matrix exposed to electron beams in the energy range between 25 and 250 GeV. The time resolution is extracted by comparing the time measurement over a single channel to that of an external timing reference detector placed along the beamline. The results are shown in Fig. 2 and meet the requirements for the Phase 2 design.

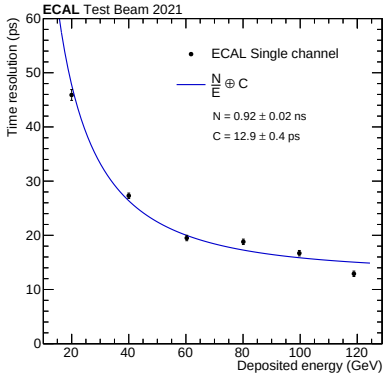


Figure 2: Time resolution as function of the deposited energy obtained in 2021 CERN test beam.

4. Conclusions

The challenging conditions of HL-LHC, with a 4-5 fold increase in occupancy with respect to LHC, require an extensive upgrade of the CMS electromagnetic calorimeter electronics. The ECAL barrel readout chain has been completely redesigned, while keeping the crystals and photo-sensors. The bandwidth of the analog readout has been increased by a factor of four, as well as the sampling frequency. This upgrade maintains the current energy resolution and provides an improved timing resolution to cope with the increased pileup. The trigger primitive generation has been moved off-detector for maximum flexibility. The pre-production versions of the ASICs have been tested and show excellent performance. At present, a larger scale test, with the electronics mounted on a fully assembled ECAL supermodule, is underway to measure the performance of the complete readout chain. The mass production and testing of the ASICs are foreseen in 2022 and 2023.

References

[1] The CMS Collaboration, The CMS experiment at the CERN LHC, Journal of Instrumentation 3 (08) (2008) S08004. doi:10.1088/1748-0221/3/08/s08004.

[2] I. Zurbano Fernandez, et al., High-Luminosity Large Hadron Collider (HL-LHC): Technical design report 10/2020 (12 2020). doi:10.23731/CYRM-2020-0010.

[3] The Phase-2 Upgrade of the CMS Barrel Calorimeters, Tech. rep., CERN, Geneva (Sep 2017).
URL https://cds.cern.ch/record/2283187

[4] The Phase-2 Upgrade of the CMS Endcap Calorimeter, Tech. rep., CERN, Geneva (Nov 2017). doi:10.17181/CERN.IV8M.1JY2.

[5] F. Thiant, Y. Geerebaert, F. Magniette, T. Romanteau, A. Zabi, A. Zghiche, New development in the CMS ECAL Level-1 trigger system to meet the challenges of LHC Run 2, PoS TWEPP2018 (2019) 052. doi:10.22323/1.343.0052.

[6] O. Gevin, P. Baron, M. Dejardin, F. Guilloux, CATIA: APD readout ASIC for the CMS phase 2 ECAL electronics upgrade, PoS TWEPP2019 (2020) 001. doi:10.22323/1.370.0001.

[7] S. Cometti, G. Mazza, LiTE-DTU: Online Data Selection, Compression, and Transmission ASIC for the Upgraded Front-End of the CMS Electromagnetic Calorimeter, in: 2019 8th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2019, pp. 1–4. doi:10.1109/MOCAST.2019.8741539.

[8] S. Biereigel, S. Kulis, R. Francisco, P. V. Leitao, P. Leroux, P. Moreira, J. Prinzie, The lpGBT PLL and CDR Architecture, Performance and SEE Robustness, PoS TWEPP2019 (2020) 034. doi:10.22323/1.370.0034.