The ITk interlock hardware protection system☆

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Abstract

For the upgrade of the Large Hadron Collider to the High-Luminosity Large Hadron Collider (HL-LHC) the ATLAS detector will install a new Inner Tracker (ITk), which consists completely of silicon detectors. Although different technologies were chosen for the inner and outer part, the major risk for all silicon detectors are heat-ups, which can cause irreparable damages. As detector elements are not accessible for several years or even for the lifetime of the detector, once the detector is installed, such damages must be avoided by all means. The ITk interlock system is a hardwired safety system, which acts as last line of defense and is designed to protect the sensitive detector elements against upcoming risks. The core of the interlock system consists of distributed FPGAs, housing the interlock matrix decision tables. They collect signals from interlock-protected devices and distribute signals onto interlock-controlled units (e.g. power supplies). Additionally, signals from external systems can be integrated. To keep the number of detector elements, which are out of operation, at a minimum, the power supplies are controlled with high granularity. The resulting large number of channels explains why no commercial solution was selected. We report from the concept to the realization.

Keywords: Interlock System, FPGA based safety system, DCS

1. The Concept

The interlock system is a hardware-based safety system to protect the sensitive detector elements of the ATLAS ITk (Inner Tracker) from the harsh conditions expected at the High-Luminosity Large Hadron Collider (HL-LHC)[1, 2, 3]. It acts between devices to be protected and units which can be a risk to the device. FPGAs house the interlock matrix decision tables. Figure 1 illustrates the concept [4]. A high segmentation is foreseen to keep the number of detector units low which are taken out of operation in case of an incidence. The resulting large number of channels, about 13000 channels, explains why a custom made solution was chosen.

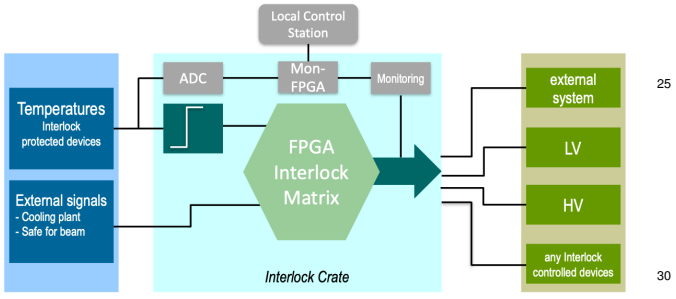

Figure 1: The concept of the interlock system[4].

2. LISSY

To fulfill the requirements of the ITk strip and the ITk pixel detector, a modular design was chosen. This allows the sub-detectors to combine the modules according to their needs. LISSY (Local Interlock Safety SYstem) is a 3U 19 inch crate. It houses three type of IO-modules, the ILK-FPGA, and the Mon-FPGA. The signals between the IO-Modules and the FPGAs are connected via separate IO-expanders and distributed via the backplane. Additionally, three pure hardwired signals are supported. Redundant power supplies ensure a reliable operation. One LISSY can handle up to 576 interlock signals.

3. The IO modules

Three types of IO-modules are available.

The T2I module. Main risk for all silicon detectors are heat ups. Therefore temperature sensors are mounted on the sensitive detector elements. The T2I (Temperature 2 Interlock) module transfers analogue signals from NTCs (Negative Temperature Coefficient) into a binary interlock signal. A discriminator creates the binary interlock signal T-HI. A second discriminator detects broken cables and sets the T-ERR signal. The thresholds can be defined by a plug-in. The T-HI and T-ERR signals are propagated to ILK-FPGA.

T-HI and T-ERR are separately propagated to the Mon-FPGA. In addition, an ADC allows for monitoring of the analogue temperature signals and test signals can be sent by the Mon-FPGA.

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The OUT module. The OUT module maps signals to the interlock-controlled devices. A fail safe logic is implemented, such that unplugged cables raise an interlock. Again, the Mon-FPGA spies onto the signals via separate IO-expanders.

The GSS module. The GSS (General Safety Signal) module receives signals from external systems. In the final system, when several LISSYs are required, the GSS modules of all LISSYs connect to the MIC (Main Interlock Crate), see Figure 2. Signals which are relevant for all LISSYs of a sub-detector, can be distributed by MIC.

4. The ILK-FPGA

The ILK-FPGA (Xilinx Artix-7 200T) is the central decision unit in the interlock system. It can handle up to 576 local IO signals and 120 inputs from remote crates via CAN (Controller Area Network). The I2C interfaces to the I/O modules are operated at 400 kHz. The CAN interface runs at 500 kBit/s. The update rate is typically 10-100 Hz.

To run the same firmware on all interlock crates, the user interlock logic is separated from the FPGA firmware. This allows for updating the user interlock logic separately, even during operation of the crate. A 10/100 Mbit/s ethernet interface is available for user access using the IPbus interface. Software tools allow for low level debugging and firmware updates. An interlock compiler enables the users to generate the user interlock logic program from boolean equations.

5. The Mon-FPGA

The Mon-FPGA reads 18 LISSY modules over 18 private I2C buses. These I2C buses are operated concurrently. The I2C readout sequence is automatically selected according to the module type. The LISSY module readout data is transfered to a backend device over private LVDS links. A non-solicited mode (periodic transmission) is default but the Mon-FPGA responds also to commands from the back-end.

The middleware is given by an OPC-UA server, which provides the data to the backend. In the backend the clients of WinCC collect the monitoring data and make them visible to the operator. The monitoring data allows for debugging the interlock system. Additionally, test signals can be given to verify the behaviour of LISSY and the implemented interlock matrix.

6. The Overall System

As several thousand interlock signals must be handled per sub-detector, several LISSYs must be combined to build the interlock system for a complete sub-detector. Figure 2 gives an overview on such system. Up to 16 LISSYs can be connected to one MIC (Main Interlock Crate). MIC receives signals from external systems and distributes these signals to the LISSYs of the sub-detector. The signals from the ATLAS wide DSS system are of main importance. They inform about failures in the cooling systems, high humidity, smoke in the experimental cavern or other global risks, which are relevant for the whole sub-detector. Further, a signal from the BIS (Beam Interfase System) can be integrated, which reports about dangerous beam conditions. The distribution of these global signals is hardwired, all logic decision is left to the LISSYs.

While the interlock signals are distributed via MIC to several LISSYs, the monitoring data of up to 16 LISSYs is concentrated onto one data stream by an EMP (Embedded Monitoring Processor) which is one of the standard ATLAS DCS components. It runs the OPC-UA server, which allows for integration of the monitoring data into the backend of ATLAS DCS. A first version of the OPC-UA server and an WinCC project allow for investigating the behaviour of the pre-production crates.

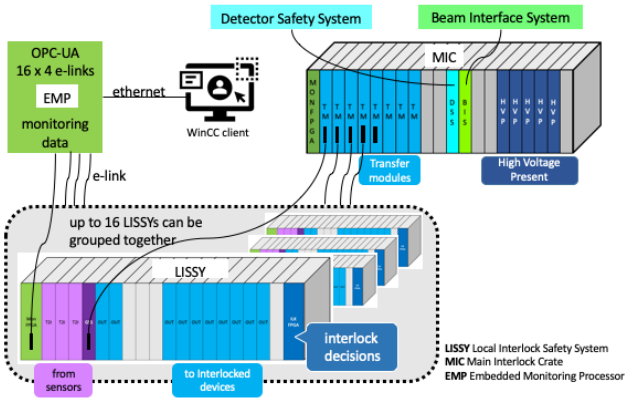

Figure 2: The components of the full interlock system.

7. Summary and Outlook

Heat-ups can cause irreparable damages to silicon detectors. The ITk Interlock system protects the sensitive silicon detector elements against potential risks from the harsh conditions expected at the HL-LHC. It acts between devices to be protected and units which can be a risk to the devices. FPGAs house the interlock matrix decision tables. In total about 13000 channels must be handled by the ITk interlock system. To fulfill the requirements of the different sub-dectors a modular system was selected. The users equip their interlock crates according to their needs. One LISSY crate can handle up to 576 channels. To build the interlock system for a complete sub-detector up to 16 LISSY crates can be combined. The ITk production system will consist of about 50 LISSY crates.

At present, the pre-production of the first LISSY crates is ongoing, the first crates are already delivered to the users.

References

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