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METHODOLOGY, CHARACTERISATION AND RESULTS FROM THE PROTOTYPE BEAM LOSS MONITORING ASIC AT CERN

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Abstract

The characterisation of novel beam loss monitoring front-end converters, based on radiation-hardened application-specific integrated circuits (ASIC), is undergoing at CERN. An effective performance analysis of the newly developed ASICs plays a key role in their candidacy for the future installation in the HL-LHC complex. This work introduces the latest test-bed architecture, used to characterise such a device, together with the variety of audits involved. Special focus is given on the verification methodology of data acquisition and measurements, in order to allow a detailed study of the conversion capabilities, the evaluation of the device resolution and the linearity response. Finally, the first results of post-irradiation measurements are also reported.

INTRODUCTION

The Beam Loss Monitoring (BLM)[1, 2] is an essential protection system of particle accelerators, since a variety of phenomena cause beam particles to escape from the desired trajectory. These produce secondary particle showers, which lead to unwanted energy deposition in the various machine elements. Thus, the BLM system is mandatory to prevent equipment activation, damage and, like in the case of the LHC, the quench of its superconductive magnets [3–6].

In view of the HL-LHC upgrade [7], a major renovation of the BLM electronics is on-going covering parts both within the accelerator tunnel and in the surface buildings. To cope with the new specifications, the BLM system will be required amongst others to enhance its radiation tolerance to reach 100 MRad of TID (was 50 kRad), and to provide a faster acquisition period of 10 µs in comparison to the currently installed system (was 40 µs) [8–11].

The high radiation tolerance requirements cannot be achieved using only commercial components, and a custom radiation hardened Application Specific Integrated Circuit (ASIC) was necessary to be designed.

The device is able to convert the analogue currents produced by the ionisation chamber detectors [12, 13] into digital data streams. These are serialised [14] and transmitted via optical fibres to the back-ends [15], where the data is further processed to obtain the beam loss measurements.

The measurements are compared in real-time with predefined thresholds [16, 17], unique by location, to decide whether the beam is permitted to circulate or its extraction must be triggered. Since the front-end conversion capabilities relies on the ASIC component, strict validation and performance characterisation on test-beds is required. Later, the post commissioning supervision will be carried on in conformity with the currently installed system [18–20].

In this report we will focus on the second version of the device, the BLMASIC, which implements similar concepts of current-to-frequency converter (CFC) as the currently operational system and an early prototype, studied in [21–24]. The validation has been performed using test-beds specifically designed to qualify the ASIC. In a previous paper [25], we presented a first version of the setup, which has since been significantly improved.

A brief description of the BLMASIC architecture and the methodology for the device validation are described in the following sections. Then, the test-bed assembly architecture, the batch data analysis software, as well as the first post-irradiation results are reported.

CONVERSION ARCHITECTURE

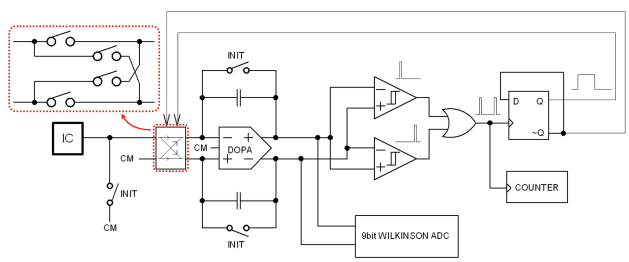

Figure 1: BLMASIC Conversion Architecture. "IC" represents the ionisation chamber detector (ideally modelled as an independent current source). "DOPA" is the input fully-differential amplifier configured as a current integrator. Quantisers and the toggling flip-flop are shown on the right.

The schematic architecture of the BLMASIC is shown in Fig. 1. The differential design of the circuit allows to double the internal signal swing and helps to improve the overall linearity response. Because of the configuration symmetry, it is possible to study its behaviour by splitting the complementary signal paths in two equivalent single-ended networks. Finally, the input current to measure is single-ended and the amplifier complementary input is connected to the circuit common-mode node, here considered as a neutral.

After the initialisation of the circuit, i.e. close the "INIT" switch, any charge injected by the ionisation chamber (IC) will be accumulated in the capacitors, producing a voltage

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swing at the amplifier outputs. Two quantisers compare the integrated charge with two fixed thresholds. They produce pulses indicating respectively whether an upper or a lower limit has been exceeded. To maximise the swing of the signal, the upper limit is set to a value close to the positive supply voltage and the lower one is close to the ground reference. The produced pulses are then combined with an OR gate and used to feed the clock of a toggling flip-flop. This allows to swap the input connections of the amplifier whenever a limit is reached using the switching circuitry, highlighted in red in Fig. 1.

For example, injecting a continuous current at the input of the circuit, the integrated current will cause a voltage ramp at the amplifier output. As soon as the voltage will reach one of the limits, the switching circuitry will toggle and consequently the ramp slope will be reversed. This mechanism generates an almost triangular waveform at the output of the integrating amplifier. Such an integrator output signal is hereafter referred to as the "primitive". The slope magnitude and the waveform frequency are proportional to the input current intensity and to the inverse of the integrating capacitance value. Therefore, knowing the circuit parameters, it is sufficient to track the number of generated pulses in-between the measurement period to obtain a measure of the current intensity.

Finally, at the integrator outputs an auxiliary 9-bit ADC designed following the Wilkinson architecture [26] is connected. It allows to keep track of the "instantaneous" values of the primitive signal, with a sampling frequency of 100 kHz. For input currents in the range of ~1 µA – 1 mA, the pulse rate (belonging to ~1 – 10 MHz) provides sufficient information to perform the measurements. Whereas, if the device has to measure low currents in the order of ~1 – 100 pA, a longer than 10 µs period would be required to carry out the same procedure, due to the low number of generated pulses. For such cases, the auxiliary ADC is exploited to directly estimate the slope magnitude. The information provided by both methods can be combined in the processing chain, with an algorithm similar to [27], to improve the resolution and reduce the system response time.

METHODOLOGY

Basic Device Functionality Tests

Basic electrical checks are required to prepare the brand new DUT for the characterisation. Initially, it is assembled on a test-bed PCB and connected only to the power supplies. To prevent permanent damages, the current limiter of each power-supply is set to twice the nominal current. Examining the PCB with a thermal camera helps also to detect and to locate excessive power dissipation spots and short circuits.

Three supply rails are used to power the device. The current consumption, measured after initialisation, resulted equal in all the DUTs. Their values were:

- 59 mA on the main (sum of digital & analog) rail (1.2 V)
- 1 mA on the common-mode reference rail (0.6 V)
- <1 mA on the low leakage input stage rail (1.7 V)

At the next step, the communication interfaces were tested. For redundancy, in the DUT both the internal registers access I^2C port and the output differential lane (80 Mbps), used for data transmission and configuration report, are duplicated. A programmable I^2C master terminal has been developed for the test-bed. In parallel, the use of a logic analyser with embeded protocol checker assisted debugging such an interface. Then, the differential lanes were connected to proper 100 Ω termination and probed with an oscilloscope. This includes an 8b/10b decoder that allowed to validate the data frame structure and to decode the first raw measurements. The DUT passed these tests successfully and no data integrity issues or erratic behaviours have been observed.

Finally, reset and power cycle events were tested, verifying the reliability of the device boot. An internal dead-lock state issue has been observed in the DUT for slow power-up ramps. This will be corrected in the next version of the ASIC.

Conversion Performance

The BLMASIC main purpose is the analogue to digital conversion of the input current. The analysis, similar to the one performed for commercial ADCs, characterises the device in terms of integral and differential non-linearity (INL and DNL respectively), conversion noise, settling time and compatibility with the source impedance.

The test-bed has been built to inject calibrated currents into the device and to monitor simultaneously its register contents. Due to the very high dynamic range (up to 180 dB), logarithmic current sweeps are used. The fast output interfaces are connected to an FPGA board, which provides the clock to the DUT and acquires the data. Only one of the lanes has been used during this study; the other lane, meant to provide redundancy, must be tested before the commissioning of the device. Also the two current inputs will be characterised independently.

The test procedure involves configuring the test current, waiting for about a second the output to stabilise and record the DUT memory contents. Such procedure is repeated for all the input current values of interest. The ability to store the entire device memory during the session allows to perform batch data processing directly on the raw values, monitoring the internal configuration. Such a method has the disadvantage of requiring larger storage, but this additional information becomes convenient when evaluating various signal processing methods. Therefore, once the optimal data treatment procedure is found, it can be implemented in the back-end cards to perform the computation in real-time.

During the characterisation of the BLMASIC, these measurement data sets have been collected:

- 50 measurements from 1 pA to 1 nA, of 10 s each
- 500 measurements from 1 nA to 1 mA, of 1 s each

DUT Irradiation

For HL-LHC operation, the BLMASIC must be radiation tolerant. Therefore, tests for the total ionisation dose (TID), the single event latch-up (SEL) and single event upset (SEU)

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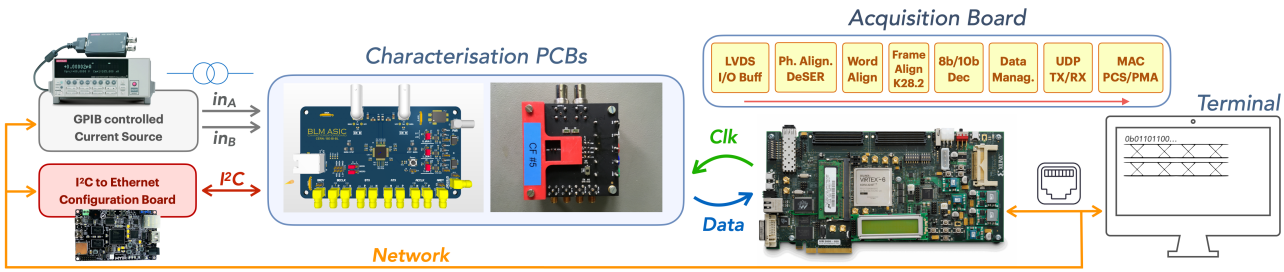

Figure 2: Characterisation Test-Bed Architecture.

must be performed, verifying the correct behaviour of the irradiated circuits and compliance with specifications.

In a preliminary study, a non-irradiated device against five other units irradiated with X-Rays was compared, to monitor any degradation of the conversion performance and validate the main operational functionality of the digital interface. Details of the irradiation sessions (performed at CERN) are reported in Table 1.

Table 1: BLMASIC X-Ray Irradiation Sessions

DUTs	Flux [MRad/h]	Time [h]	TID [MRad]
$CFC_{\#}1$	4.43	23	102
$CFC_{\#}2$	1.54	52	80
$CFC_{\#}3$	4.43	23	102
$CFC_{\#}4$	4.43	23	102
$CFC_{\#}5$	1.54	65	100

As soon as the next version of the device will be manufactured, devices will be subjected to additional irradiation campaigns, that more realistically emulate the final operational environment, such as with high-energy protons at Paul Scherrer Institut (PSI) and with mixed field radiation at CHARM, CERN.

TEST-BED ASSEMBLY

The test-bed makes use of a current source generator and a custom I^2C configuration card to provide the input current and control the device. Two printed circuit board variants, that can accept the DUT, have been developed to support the various activities. The first provided multiple access points and was used in [25]. Later, a more spartan version for the irradiation campaigns was realised. Finally, a supervision acquisition board decodes, collects the data, and transmits all information in real-time to a computer by UDP based packets over a gigabit Ethernet interface. A custom software was developed to perform the measurements and analyse the data. All the test-bed equipment is on the CERN network, allowing the remote control of the characterisation sessions. A block diagram of the test-bed components and connections can be seen in Fig. 2.

DATA ANALYSIS

Data Retrieval

Following the input current sweep runs and the extraction of the relative DUT memory storage, a first treatment was necessary to arrange the measurement registers and produce manageable numeric arrays. This process is computationally expensive because of the necessary bit addressing on the register map of the DUT. Although not usually efficient on CPUs, special functions have been used for bit data management. A possible alternative method would be to expand the results of interest directly on the acquisition board FPGA, but the dump of the entire DUT memory was preferred. Furthermore, to minimise the computation time of the data analysis, all the involved processing steps have been parallelised on separate threads, exploiting the performance of multi-core CPUs.

CFC Counter Data Analysis

The first analysis is focusing on the data provided by the CFC counters, incremented whenever the flip-flop toggles.

The BLMASIC must cover a large dynamic range, and different acquisition times are used for different input ranges, in order to obtain the desired measurement precision. Short times ($\leq$100 µs) are required while performing high losses measurements (currents >10 µA), because a fast response must be guaranteed to protect the accelerator. Response time constraints are further reduced ($\leq$20 µs) when reporting the instrument saturation or currents close to the full scale. On the other hand, longer integration times (up to tens of seconds) are allowed when high precision or low losses measurements (down to ~1 pA) are desired. Exploiting the overall acquired data, it is possible to test the conversion performance with a variety of averaging times. To this aim, a custom software procedure has been developed. For each specified averaging time it performs:

1. the partitioning of the full acquisition samples in clusters of the specified time window;
2. the averaging of the data within each of the cluster, representing an averaged measure;
3. the computation of the standard deviation amongst all averaged measures;
4. the computation of all samples average, representing a reference result.

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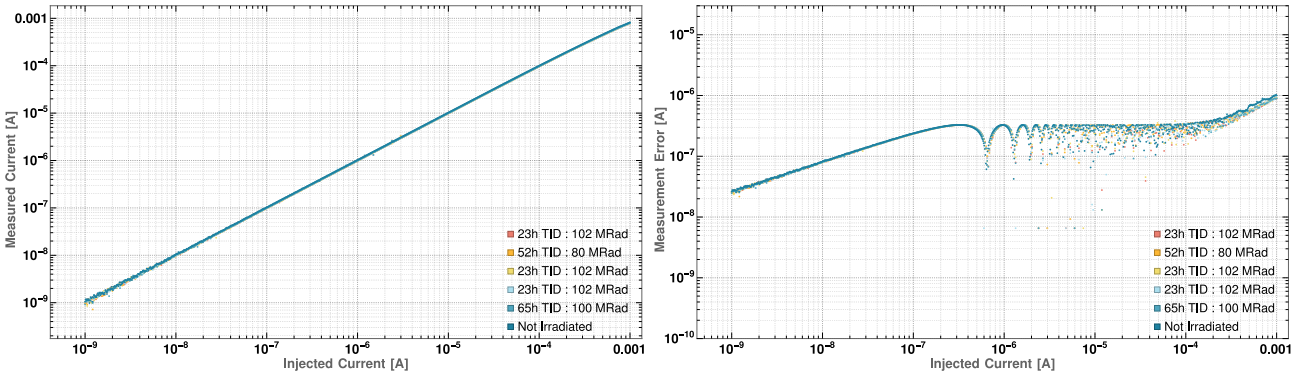

Figure 3: Conversion characteristic (left plot) and absolute errors (right plot) by a logarithmic current sweep of 500 values from 1 nA to 1 mA. The averaging time window is set to 100 µs.

Wilkinson ADC Data Analysis

The procedure used to analyse the Wilkinson ADC data follows similar steps to what was described before. However, a further computation is needed to estimate the slope magnitude of the primitive waveform. To this purpose, the linear regression has been applied on the samples of each cluster. In case this latter includes a slope direction change, detected on the basis of the CFC counter data, it will be discarded. Otherwise, the linear regression result will replace the averaged measures of the procedure step 2.

This analysis has allowed to achieve sub pA precisions for 1 s measurements of low currents (from 1 pA to 1 nA), in conformity with the design specifications. Hovewer, since its FPGA implementation can result resource-intensive, the exploitation of alternative but equally effective methods is under investigation.

POST-IRRADIATION RESULTS

In Fig. 3 it is shown a relevant result example obtained by the presented methodology. In particular, it reports the measured versus the injected current. Configured the test for high currents up to 1 mA, only the CFC counters have been exploited. The averaging time window has been set to 100 µs, corresponding to 10 samples.

No major performance drifts have been observed amongst the DUTs. The ripples in the error plot seem due to the data processing, not reflecting physical phenomena.

To study the conversion precision, relative errors have been computed. It turned out that an error smaller than 10 % is observed in measurements of currents greater than 3 µA, while it stays below the 1 % for currents above 35 µA. This is well inside the design specifications and it can be improved by advanced filtering techniques. Finally, a deviation from the linearity has been observed, which degrades the accuracy for currents in full-scale regime. This is due to a connection bug in the input stage clamping diodes, which has been solved in the third version upgrade. Thus, we will achieve the design value of 2.5 V for the related power rail.

CONCLUSIONS

The work reports on the test-bed architecture, the characterisation methodology and the data analysis aimed to perform the validation of the BLMASIC. Valuable results have been carried out during the tests, showing promising conversion performances and compliance with the design specifications.

The total dose irradiation session did not bring major drifts in the conversion behaviour. In every cases, the devices were able to perform high losses measurements with a precision below the 1% in a range from 35 µA to 1 mA and an integration time of 100 µs.

The presented method does not provide direct information about the INL / DNL factors of our converter, because its bit resolution is not strictly defined by the specifications and it depends on the chosen integration time. However, one could undertake a different approach, compiling a table that includes the equivalent conversion bits, the SNR and the non-linearity factors at various integration time windows. This will be helpful to optimise the device utilisation and eventually develop an auto-tuned methodology for the backends processing.

The consolidation of the gained experience, the procedures standardisation and the design improvement will be crucial for the test on the v3 device, which will begin by Fall 2021.

REFERENCES

[1] B. Dehning *et al.*, "The lhc beam loss measurement system," in *2007 IEEE Particle Accelerator Conference (PAC)*, 2007, pp. 4192–4194. doi:10.1109/PAC.2007.4439980

[2] B. Dehning *et al.*, "Overview of LHC beam loss measurements," Tech. Rep., 2011.

[3] C. Kurfuerst, B. Dehning, E. Holzer, A. Nordt, M. Sapinski, and C. Fabjan, "Quench Prevention of the LHC Quadrupole Magnets," 2010, https://cds.cern.ch/record/1265861

[4] A. Priebe *et al.*, "Beam-induced Quench Test of a LHC Main Quadrupole," in *Proc. IPAC'11*, San Sebastian, Spain, 2011, paper WEPC172, pp. 2388–2390, https://jacow.org/IPAC2011/papers/wepc172.pdf

ISBN: 978-3-95450-230-1 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2021-TUPP34

[5] A. Priebe, B. Dehning, M. Sapinski, M. Q. Tran, and A. Verweij, "Investigations of quench limits of the LHC superconducting magnets," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 3, p. 4 701 205, 2012. doi:10.1109/TASC.2012.2236378

[6] M. Sapinski *et al.*, "Beam induced quenches of LHC magnets," in *Proc. IPAC'13*, Shanghai, China, 2013, paper THPEA045, pp. 3243–3245, https://jacow.org/ipac2013/papers/THPEA045.pdf

[7] G. Apollinari, I. Béjar Alonso, O. Brüning, M. Lamont, and L. Rossi, "High-luminosity large hadron collider (hl-lhc): Preliminary design report," Fermi National Accelerator Lab.(FNAL), Batavia, IL (United States), Tech. Rep., 2015.

[8] C. Zamantzas, B. Dehning, E. Effinger, G. Ferioli, G. Guaglio, and R. Leitner, "The LHC beam loss monitoring system's real-time data analysis card," in *Proc. DIPAC'05*, Lyon, France, 2005, paper POW019, pp. 280–282, https://jacow.org/d05/PAPERS/POW019.PDF

[9] E. Effinger, C. Zamantzas, G. Ferioli, J. Emery, and B. Dehning, "Single gain radiation tolerant LHC beam loss acquisition card," paper WEPC06, pp. 319–321, 2007, https://jacow.org/d07/papers/wepc06.pdf

[10] C. Zamantzas, M. Alsdorf, B. Dehning, S. Jackson, M. Kwiatkowski, and W. Vigano, "System Architecture for measuring and monitoring Beam Losses in the Injector Complex at CERN," no. CERN-ACC-2013-0252, 2012, http://cds.cern.ch/record/1627308

[11] W. Vigano, M. Alsdorf, B. Dehning, M. Kwiatkowski, G. Venturini, and C. Zamantzas, "10 orders of magnitude current measurement digitisers for the CERN beam loss systems," *J. Instrum.*, vol. 9, no. 02, p. C02011, 2014. doi:10.1088/1748-0221/9/02/C02011

[12] M. Stockner, B. Dehning, C. Fabjan, G. Ferioli, and E. B. Holzer, "Measurements and Simulations of Ionization Chamber Signals in Mixed Radiation Fields for the LHC BLM System," in *2006 IEEE Nuclear Science Symposium Conference Record*, vol. 3, 2006, pp. 1342–1345. doi:10.1109/NSSMIC.2006.354151

[13] B. Dehning *et al.*, "Lhc beam loss detector design: Simulation and measurements," in *2007 IEEE Particle Accelerator Conference (PAC)*, IEEE, 2007, pp. 4198–4200.

[14] P. Moreira, "The lpgbt project status and overview," in *ACES*, 2016.

[15] A. Boccardi, M. Barros Marin, T. Levens, B. Szuk, W. Viganò, and C. Zamantzas, "A Modular Approach to Acquisition Systems for Future CERN Beam Instrumentation Developments," pp. 1103–1106, 2015. doi:10.18429/JACoW-ICALEPCS2015-THHB2002

[16] C. Zamantzas *et al.*, "Configuration and validation of the LHC beam loss monitoring system," in *Proc. DIPAC'09*, Basel, Switzerland, 2009, paper TUPB31, pp. 240–242, https://jacow.org/d09/papers/tupb31.pdf

[17] M. Kalliokoski *et al.*, "BLM threshold evolution and 2016 proposal," pp. 191–196, 2016, http://cds.cern.ch/record/2294668

[18] J. Emery, B. Dehning, E. Effinger, A. Nordt, M. Sapinski, and C. Zamantzas, "First experiences with the LHC BLM sanity checks," *J. Instrum.*, vol. 5, no. 12, p. C12044, 2010. doi:10.1088/1748-0221/5/12/C12044

[19] C. F. Hajdu, T. Dabóczi, and C. Zamantzas, "On-line system supervision of beam loss monitoring systems with sinusoidal excitation," in *XXI IMEKO World Congress*, 2015, pp. 1176–1180, https://www.imeko.org/publications/wc-2015/IMEKO-WC-2015-TC10-237.pdf

[20] C. Hajdu, T. Dabóczi, and C. Zamantzas, "Development of a Method for Continuous Functional Supervision of BLM Systems," in *Proc. IBIC'16*, Barcelona, Spain, 2017, paper MOPG21, pp. 90–93. doi:10.18429/JACoW-IBIC2016-MOPG21

[21] G. Venturini, B. Dehning, E. Effinger, and C. Zamantzas, "Design Specifications for a Radiation Tolerant Beam Loss Measurement ASIC," Tech. Rep., 2009.

[22] W. Vigano, E. Effinger, C. Zamantzas, G. Venturini, and B. Dehning, "Comparison of three different concepts of high dynamic range and dependability optimised current measurement digitisers for beam loss systems," 2012.

[23] G. Venturini, F. Anghinolfi, B. Dehning, and M. Kayal, "Characterization of a wide dynamic-range, radiation-tolerant charge-digitizer ASIC for monitoring of beam losses," no. 1, paper MOPA12, pp. 74–78, 2012, https://jacow.org/IBIC2012/papers/mopa12.pdf

[24] G. Venturini, F. Anghinolfi, B. Dehning, F. Krummenacher, and M. Kayal, "A 120db dynamic-range radiation-tolerant charge-to-digital converter for radiation monitoring," *Microelectronics Journal*, vol. 44, no. 12, pp. 1302–1308, 2013. doi:10.1016/j.mejo.2013.08.020

[25] F. Martina, L. Giangrande, J. Kaplon, P. V. Leitao, and C. Zamantzas, "Testbed Development for the Characterisation of an ASIC for Beam Loss Measurement Systems," in *Proc. IBIC'20*, Santos, Brazil, 2020, paper THPP04, pp. 215–217, doi:10.18429/JACoW-IBIC2020-THPP04

[26] T. Vergine, M. De Matteis, A. Baschirotto, and A. Marchioro, "A 32-channel 12-bits 65nm Wilkinson ADC for CMS Central Tracker," *IEEE Nucl. Sci. Symp. Conf. Rec.*, 1–4. 4 p, 2014. doi:10.1109/PRIME.2014.6872683

[27] M. Kwiatkowski, C. Zamantzas, M. Alsdorf, B. Dehning, and W. Viganò, "A Real-Time FPGA Based Algorithm for the Combination of Beam Loss Acquisition Methods Used for Measurement Dynamic Range Expansion," in *Proc. IBIC'12*, Tsukuba, Japan, 2012, paper TUPA31, pp. 419–423, https://jacow.org/IBIC2012/papers/tupa31.pdf