Timing performance of the Timepix4 front-end

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ABSTRACT: A characterisation of the Timepix4 pixel front-end with a strong focus on timing performance is presented. Externally generated test pulses were used to probe the per-pixel time-to-digital converter (TDC) and measure the time-bin sizes by precisely controlling the test-pulse arrival time in steps of 10 ps. The results indicate that the TDC can achieve a time resolution of 60 ps, provided that a calibration is performed to compensate for frequency variation in the voltage controlled oscillators of the pixel TDCs. The internal clock distribution system of Timepix4 was used to control the arrival time of internally generated analog test pulses in steps of about 20 ps. The analog test pulse mechanism injects a controlled amount of charge directly into the analog front-end (AFE) of the pixel, and was used to measure the time resolution as a function of signal charge, independently of the TDC. It was shown that for the default configuration, the AFE time resolution in the hole-collecting mode is limited to 105 ps. However, this can be improved up to about 60 ps by increasing the preamplifier bias-current at the cost of increased power dissipation. For the electron-collecting mode, an AFE time resolution of 47 ps was measured for a bare Timepix4 device at a signal charge of 21 ke. It was observed that additional input capacitance from a bonded sensor reduces this figure to 62 ps.

KEYWORDS: Front-end electronics for detector readout; Hybrid detectors; Timing detectors; Particle tracking detectors (Solid-state detectors)

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Contents

1 Introduction

The High Luminosity Large Hadron Collider (HL-LHC) [1] is an upgrade to the existing Large Hadron Collider that will increase the potential for new discoveries by increasing the integrated luminosity by a factor of ten. As a consequence, the number of concurrent collisions per bunch crossing (referred to as pile-up) will increase, making it more difficult for particle physics experiments to distinguish between collisions based on the spatial measurements of collision products by the detectors closest to the interaction point. To prevent large amounts of pile-up, the instantaneous luminosity will be kept at a constant level for the majority of the time during which collisions take place (a few hours typically); normally the instantaneous luminosity peaks at the start and decays over time, but luminosity levelling prevents the initial peak while keeping the average high enough to reach the desired integrated luminosity. Despite luminosity levelling, the tracking of decay products based on spatial measurements will likely be insufficient to assign them to the correct primary vertex because the reconstructed tracks will not have the required spatial resolution to distinguish between spatially overlapping vertices. A potential solution that is currently being pursued in the particle physics community is the incorporation of time measurements in the detectors to aid in the

reconstruction of tracks and primary vertices — a method typically referred to as 4D tracking [2, 3]. The time resolution that can be achieved with pixel detectors is therefore of great interest.

The time resolution of a pixel detector partly depends on the physical processes that happen in the sensor material in which charged particles deposit part of their energy, which generates a detectable electronic signal [4]. Another important contribution to the time resolution is from the front-end electronics that amplifies and discriminates the sensor signals. Lastly, the time at which the signal is discriminated is converted to a digital representation by a time-to-digital converter (TDC) which also contributes to the time resolution. New sensor technologies are being developed in order to achieve the time resolution required for 4D tracking at the HL-LHC, and the results are promising [5, 6]. However, there is currently no full-scale pixel readout ASIC with a front-end that is fast enough to benefit from the intrinsic time resolution provided by these new fast-sensor technologies. In a previous study [7] it has been shown that 3D [8] and thin planar detectors bonded to the Timepix3 pixel ASIC [9] have a time resolution that is limited by the pixel front-end.

Timepix4 [10] is the latest ASIC in the Medipix family [11]. It is the successor to Timepix3 and Timepix [12], which have been used across a wide range of applications, partly owing to their ability to do per-pixel time measurements.[1] In this study the timing performance of the new Timepix4 ASIC is characterised by means of test signals. The pixel TDC is studied by externally generated signals that are routed to the digital front-ends of pixels near the bottom and top peripheries, and the time resolution of the analog front-end is characterised by internally generated test pulses. The TDC measurements are performed using only bare ASICs (without a bonded sensor). The analog front-end measurements are performed also with devices that are bonded to $300\,\mu\text{m}$ planar silicon p-on-n sensors which provide a realistic input capacitance to the preamplifier. Two sequential revisions of the Timepix4 ASIC, versions 1 and 2, are tested.

This paper is structured as follows. Section 2 gives a general introduction of Timepix4 and explains its relevant features. Section 3 covers the timing performance of the digital front-end, and presents calibration measurements that are required in section 4, which present the analog front-end measurements and their results. Section 5 contains the conclusion.

2   The Timepix4 pixel ASIC

Timepix4 has been produced in a 65 nm CMOS technology. It has a matrix that consists of 448×512 pixels, which is a factor 3.5 bigger than Timepix3. Furthermore, the maximum hit rate has been improved by a factor 8 to a value of $358\,\text{Mhits/cm}^2/\text{s}$. Most importantly, concerning the subject of this paper, it offers an improved analog timing performance, and also has a more precise TDC featuring time bins of 195 ps compared to the 1.56 ns bin size in Timepix3. Like its predecessor, Timepix4 can measure the time of arrival (ToA) and time over threshold (ToT) of each hit simultaneously. The latter is a surrogate measure for the amount of charge in a signal, which

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[1]Chronologically, Timepix2 [13] was developed after Timepix3 as a successor to Timepix in order to meet a demand pertaining to applications that do not necessitate the added complexity of data-driven readout associated with Timepix3. The Timepix chips are named according to the collaboration by which they are developed: Timepix3 was developed by the Medipix3 collaboration that developed the Medipix3 ASIC. At the time, the Medipix2 collaboration did not develop a second version of Timepix alongside Medipix2.

can be used to measure particle energy. It can also be used to correct systematic errors in the time measurement that depend on signal size, as will be discussed in section 4.4.

2.1 Pixel front-end

Figure 1 shows a schematic diagram of the Timepix4 front-end. As in Timepix3 [14], the charge sensitive preamplifier in the analog front-end of Timepix4 is based on the Krummenacher scheme [15]. It compensates for leakage current and it can process positive as well as negative input signals to work with both hole- and electron-collecting sensors. The preamplifier has a roughly linear relationship between input charge and ToT because the feedback capacitor, onto which the signal current at the input pad is integrated, is discharged at a constant rate. The dynamic range of the ToT measurement can be increased by enabling the low-gain mode. This mode lowers the preamplifier gain by adding an extra capacitor in parallel to the main feedback capacitance. For hole-collecting sensors, the dynamic range can be increased further by the adaptive-gain mode, which adds a MOS gate capacitance to the feedback circuit. In this study only the default high-gain mode is considered.
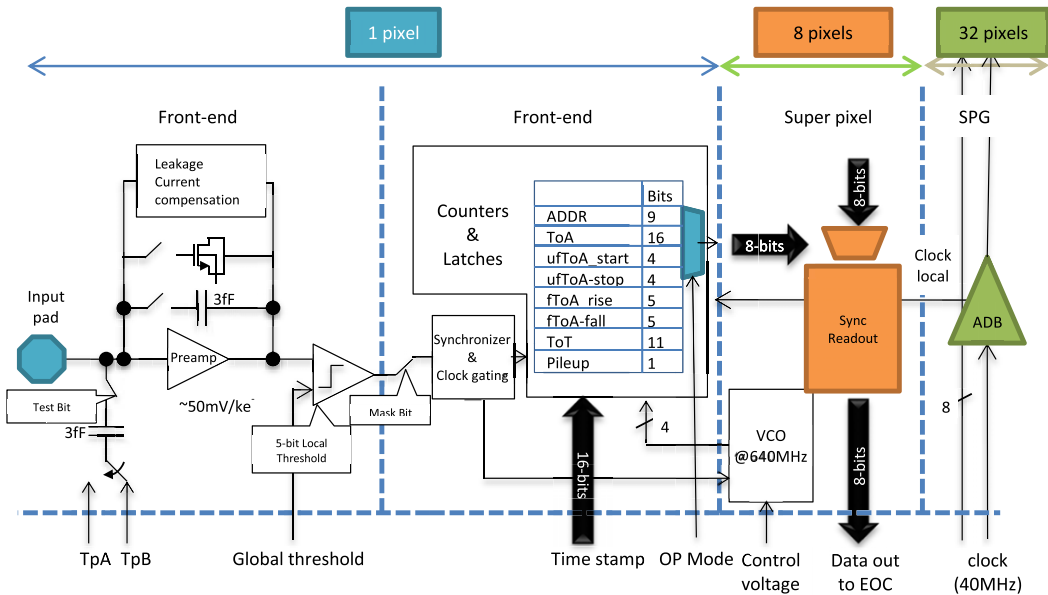

Figure 1. Schematic diagram of the Timepix4 front-end [10]. The front-end of a single pixel is divided into an analog and a digital part. A superpixel consists of two by four pixels and contains a 640 MHz oscillator which is used for precise time measurements. A superpixel group (SPG) consists of four superpixels and contains two adjustable delay buffers (ADBs) that distribute the system clock along columns of pixels (only one is shown).

Although the analog front-end can process positive as well as negative input signals, the time resolution is expected to be better for electron-collecting sensors. For hole-collecting sensors, at a certain amount of input charge, the analog front-end enters a slew-rate limited regime where a further increase in the input charge does not increase the slope of the preamplifier signal at the output anymore [16]. For positive polarity signals, there is an upper bound to the current with which the first amplifier stage can discharge the capacitive load at its output. As a consequence, the time resolution is inherently limited for hole-collecting sensors.

The test-pulse circuit at the preamplifier input allows for the injection of a controlled amount of charge. The input is connected to the voltage references TpA and TpB through a capacitor in an alternating manner; each time the voltage switches, a current pulse is injected into the front-end. The duration of this injected current signal is negligible compared to the rise time of the preamplifier, and the signal can therefore be regarded as having the shape of a delta function.

The discriminator after the preamplifier uses a global (chip-wide) threshold voltage. To compensate for pixel-to-pixel baseline variations, each pixel also has a five-bit local threshold setting, which is referred to as a trim DAC in this paper.

Figure 1 also contains a table listing the counters and latches involved in the various time measurements of each hit. In this figure, the ToA is the timestamp corresponding to the 40 MHz clock, which in this paper is more specifically referred to as the coarse ToA (cToA). Likewise, the ToT is the number of 40 MHz clock cycles that the preamplifier output is above the threshold value. The so-called fine time of arrival of the rising and falling edges of the preamplifier signal, fToA-rise and fToA-fall, correspond to measurements performed with a 640 MHz voltage-controlled oscillator (VCO) which is shared by a group of two by four pixels referred to as a superpixel. In this study only the fToA-rise counter is used, and it is simply referred to as the fToA. The even more precise ultra-fast time of arrival codes, ufToA-start and ufToA-stop, capture the phase of the VCO when the discriminator fires (start) and when the first subsequent 40 MHz clock edge arrives (stop). The ufToA-start code is only relevant for hits that arrive when the VCO has already been activated by another hit in the same superpixel, which cannot happen with the measurement method used in this study. Therefore, only the ufToA-stop code is used, and for brevity it is simply referred to as the ufToA code, or simply the ufToA when talking about its decoded value. The next section explains the time measurement and these variables in more detail.

In section 4.3 the test-pulse circuit is used to measure the time resolution of the analog front-end as a function of input charge. In this study the reference-clock distribution system (section 2.3) is used to control the clock phase with respect to the arrival time of the internally generated test pulses. As the clock is delayed, the time bin in which the test pulses arrive will change, and due to the noise in the analog front-end, this transition from one bin to another is not instantaneous: With each increment of the clock delay, the number of test pulses arriving in one time bin gradually decreases as they end up in the next adjacent time bin. The number of hits as a function of the clock delay therefore takes on the shape of an s-curve, which is the cumulative ToA distribution of the test pulses from which the time resolution of the analog front-end can be determined.

Timepix4 offers the possibility to use the digital front-end of certain pixels to timestamp external signals. This can be useful when working in conjunction with other detectors (to provide reference signals for example). In section 3.2 this feature is used to study the TDC (which is of the same type for all pixels) by generating external signals with a controlled arrival time with respect to the reference clock. In section 3.4 this feature is used to calibrate the reference-clock distribution, which is necessary for the analog test-pulse measurements in section 4.

2.2 Time measurement in Timepix4

The time-to-digital conversion in Timepix4 can be roughly divided into three parts, of which the first two are similar to Timepix3 (figure 2). First the coarse ToA is determined as the 40 MHz clock cycle in which the preamplifier output goes over threshold and activates the discriminator. Secondly,

the discriminator activates the VCO, and by counting its number of oscillations until the next rising edge of the 40 MHz clock, which defines the fine ToA, the timestamp granularity can be improved to 1.56 ns. In Timepix4 the VCO is also activated when the preamplifier goes below threshold in order to achieve a more precise ToT measurement. Normally, this feature is not necessary as the uncertainty in the ToT measurement is dominated by the voltage noise on the preamplifier output due to the shallow threshold crossing of the falling edge. However, if the discharge-current setting is increased, the threshold crossing improves, and the timestamp granularity due to the 40 MHz clock can become the dominating factor. This feature is mainly aimed at high flux applications, where it might be necessary to increase the discharge current of the feedback capacitor, and thereby shorten the preamplifier output signal to prevent signal pile-up.
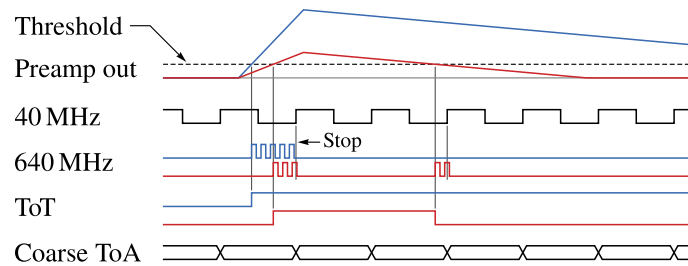

Figure 2. Diagram of the time measurement in Timepix4 for two hits with a different signal amplitude. In Timepix4 the 640 MHz clock is also activated on the falling edge of the discriminator in order to measure the ToT with a granularity of 1.56 ns. Figure adapted from [17].

Figure 3 shows the third part of the time-to-digital conversion in Timepix4. The ToA measurement is further refined by having four phase shifted copies of the 640 MHz clock. These phase shifted clocks define eight time bins within a single 1.56 ns period. The states of these four clocks are latched on the subsequent rising edge of the 40 MHz clock after the signal has crossed threshold. This defines the four-bit ultra-fine ToA code, which is used to refine the time measurement to 195 ps.
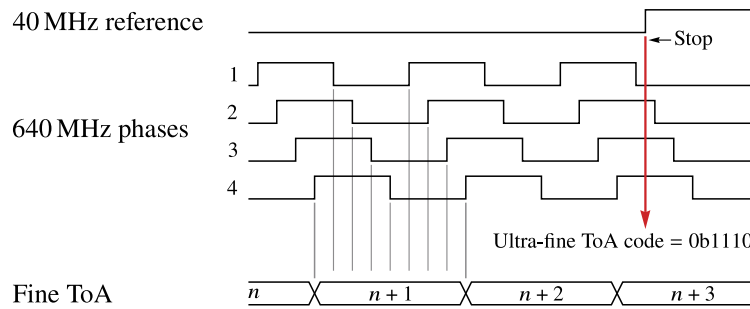

Figure 3. Diagram showing the ultra-fine ToA measurement in Timepix4. The four phase shifted 640 MHz clocks divide the 1.56 ns period into eight time bins of 195 ps.

The common control voltage of the VCOs, which determines their frequency, is normally generated in the centre periphery by a phase-locked loop (PLL) which is synchronised to the 40 MHz reference clock. However, the second iteration of the chip (Timepix4v1) suffers from a problem in the modelling of the control-voltage dependence of the VCO frequency, which has

led to a frequency that is too high.[2] The supply voltage of the periphery PLLs can be lowered independently to achieve the target frequency, which is necessary for the correct transmission of data. The supply voltage of the superpixel VCOs, however, cannot be set independently, and the control voltage that is generated by the periphery PLLs is too high. The control voltage is therefore configured to be taken from a dedicated DAC that is set to its lowest value to lower the frequency as much as possible. The resulting frequency is still too high, resulting in small time bins, but this does not negatively affect the front-end operation otherwise.

2.3 Reference-clock distribution

The 40 MHz reference clock is distributed along each double-column structure by means of a digital delay-locked loop (DLL) in order to achieve a well-defined clock phase at the pixels with a target skew of less than 100 ps [18]. A schematic of the DLL structure is shown in figure 4. The clock propagates away from the centre periphery along the columns to the outermost super-pixel groups and back. In each super-pixel group, the clock is buffered in both directions by an adjustable delay buffer (ADB). During normal operation, the controller, which is located in the centre periphery, regulates the delay of each of the 32 ADBs to 781 ps in order to achieve a total delay that is equal to one clock cycle of 25 ns. It is also possible, however, to override all controllers and set a chip-wide DLL control code to set the delay manually. Furthermore, all ADBs can be bypassed individually to prevent malfunctioning or completely defective ADBs from affecting entire double-columns. The manual control of the ADBs also allows for accurate control of the clock phase, which is demonstrated in section 3.4, and used in section 4.3 to measure the analog front-end time resolution.
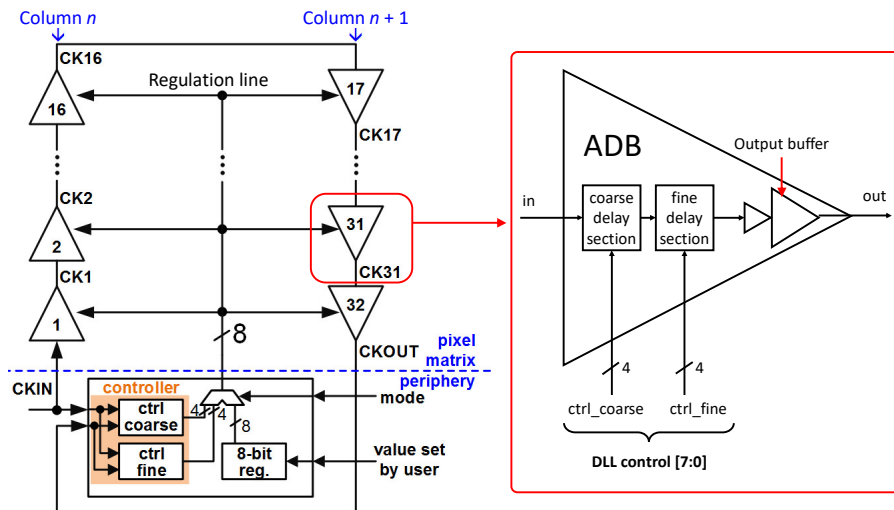

Figure 4. Schematic of the digital delay-locked loop that distributes the 40 MHz reference clock along a double-column. Figure adapted from [18].

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[2]The first iteration (Timepix4v0) suffers from the same problem.

3 Digital front-end measurements

In this section the superpixel TDC is characterised using a similar method that was used to determine the time-bin sizes of Timepix3 [7, 19]. Section 3.1 describes the measurement setup, and section 3.2 presents the results. In section 3.3 the expected TDC resolution is determined from the measurement results. In section 3.4 the clock distribution system is calibrated in preparation of the analog front-end characterisation described in the next section.

3.1 Measurement setup

The digital pixel inputs of Timepix4 can be used to timestamp up to four external signals. Each half of the chip has two digital pixel inputs, and each input is routed to a different set of double-column structures within that half. These double-column structures are typically referred to by their respective end-of-column (EoC) blocks. Within each half, one input is routed to all even-numbered EoCs, and the other input goes to all odd-numbered EoCs. The external signals are routed to the digital front-ends of all pixels in the first superpixel of each EoC. These signals can be enabled on a per-superpixel basis, and pixels can be masked to prevent receiving multiple hits per superpixel. The measurements described here are performed with a single non-masked pixel in each superpixel.

Figure 5 shows a diagram of the measurement setup that is used for the digital pixel measurements. The external test pulses are generated by two pulse generators:[3] The first pulse generator provides a 10 MHz clock and a synchronised 100 Hz trigger signal to a second pulse generator, which is used to generate square pulses with a width of 1 μs that are phase shifted by means of a configurable trigger delay. The signals are then fed into the Timepix4 readout system (SPIDR4, the successor of SPIDR3 [20, 21]) which generates a synchronised 40 MHz reference clock for Timepix4, and passes on the test pulses to one digital pixel input of each half of the chip. Figure 6 shows the SPIDR4 control board with a Timepix4 carrier board containing a Timepix4v1 bonded to a 300 μm p-on-n sensor. The setup allows for precise control of the test-pulse arrival time in steps of 10 ps within the 25 ns clock period of the reference clock.

3.2 Superpixel TDC characterisation

The TDC is characterised by scanning the test-pulse arrival time through the 25 ns reference-clock period in steps of 10 ps and recording the resulting timestamps. Figure 7 shows the measurement results from a single pixel for both the fine and ultra-fine time bins. It can be seen that the VCO frequency of Timepix4v1 is too high, resulting in 21 fine time bins. Timepix4v2 has a VCO frequency much closer to the design value, resulting in 17 fine bins. The first fine bins (fToA 0) of both devices are about half the size of the others by design: The fToA counter is incremented by the VCO clock with the largest phase delay as was illustrated in figure 3. The size of the last fine bin (fToA 20 for version 1 and fToA 16 for version 2) depends on the VCO frequency. The 17 ps jitter on the edges is dominated by the pulse generator. The difference between the ultra-fine bin sizes is clearly visible for both devices, especially for ufToA binary codes 0000 and 1111. The number of

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[3]The AT Pulse Rider was added after it was observed that the internal trigger of the Keysight is not sufficiently synchronised with its 10 MHz clock. The internal trigger suffers from a drift of about 0.1 ns per hour of elapsed real time (the exact value depends on the configuration) with respect to the 10 MHz clock.
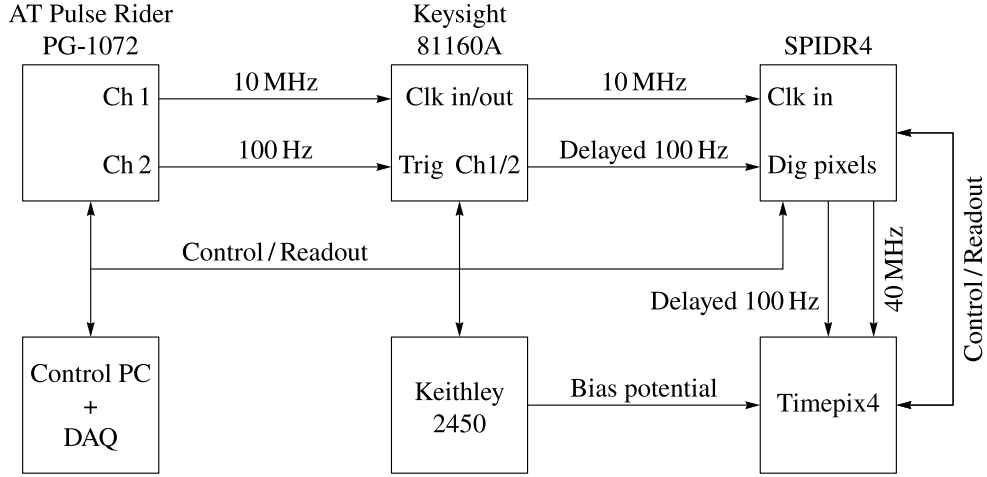
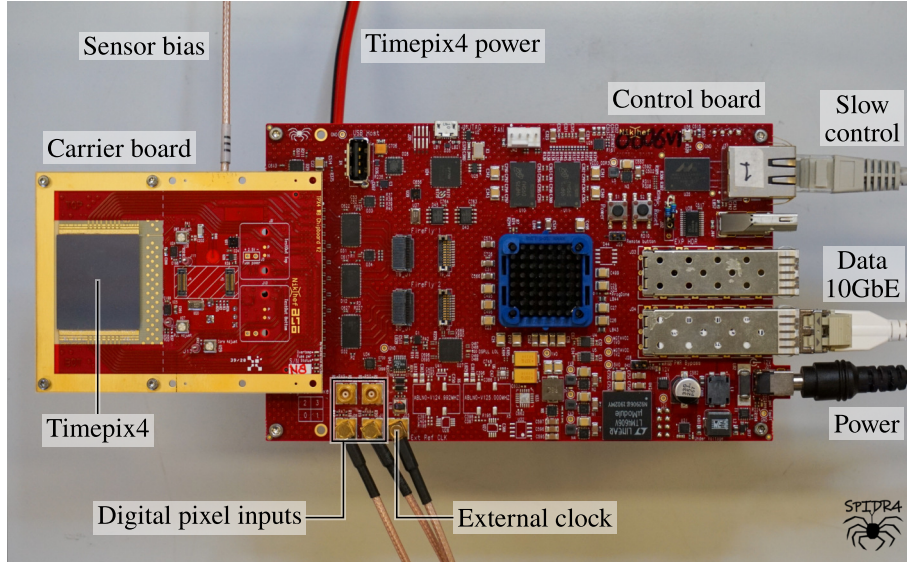**Figure 5**. Diagram of the measurement setup.

Figure 6. A SPIDR4 control board with a Timepix4 carrier board containing a Timepix4v1 with a 300 μm sensor. The Timepix4 power cable is directly connected to the carrier board.

hits that arrive in or after[4] a certain time bin can be modelled as

$$f\left(t_{\text{delay}}, t_n, \sigma_{\text{j}}\right) = \frac{N_{\text{tp}}}{2}\left[1 + \text{erf}\left(\frac{t_{\text{delay}} - t_n}{\sqrt{2}\,\sigma_{\text{j}}}\right)\right], \tag{3.1}$$

where t_{delay} is the trigger delay, t_n is the left-edge location of the n-th bin where n is an arbitrary sequential number assigned to the bins, σ_{j} is the jitter of the measured arrival time of the pulses with respect to the reference clock, and N_{tp} is the total number of pulses per measurement. In

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[4]This is a subtle detail, but it is important in ensuring that the data are well-described by an error function when the time bins are small because the hits might be distributed over more than two time bins.

order to determine the time-bin sizes, equation (3.1) is fitted to the data, and the bin sizes are then determined as

$$w_n = t_{n+1} - t_n . \tag{3.2}$$

Figure 8 shows the fit results for the bottom half of a Timepix4v1 device. The mean bin size of 1.26 ns is smaller than the design value of 1.56 ns due to the problem with the VCO frequency of Timepix4v1 as was explained in section 2.2. The data indicates that the VCOs are running at a mean frequency of 794 MHz with a standard deviation of 1.7 % over the superpixels. The majority of superpixels have 21 fine time bins, except for a small fraction of 0.7 % that have 20 or 22 fine bins. It is also observed that the ultra-fine time bins exhibit a clear structure in size. Furthermore, time bins that are located immediately before a rising edge of the 40 MHz reference clock show a relatively large pixel-to-pixel variation in size.

Figure 9 shows the results for both matrix halves of a Timepix4v2 device. A difference of 2 % is observed in the mean bin size between the bottom and top halves, which could be due to a difference in the ground potential. It was checked that the variation in bin size is not correlated to the variation in the VCO control voltage due to the distribution over the EoCs. The overall bin size of 1.565 ± 0.017 ns corresponds to a VCO frequency of 639 ± 7 MHz, which is in agreement with the design value. The ultra-fine bins show the same structure as observed in Timepix4v1. It is also observed that the ultra-fine time bins that are located directly in front of a rising edge of the 40 MHz clock vary in size from almost 0 up to about 300 ps. This variation will add to the relative time offsets between pixels, and degrade the overall time resolution if not corrected. The contribution to the total time resolution can be approximated by the bin size RMS of 89 ps.

The increased size of ufToA bins 0 and 4 can be understood by considering the VCO, which consists of a chain of four 195 ps delay cells whose outputs are the four clock phases that were shown in figure 3. The first delay cell can be seen as an AND gate with a 195 ps delay; one input is the OR function of the eight discriminators in the superpixel to activate the VCO, and the other input is the inverted output of the last delay cell. The delay of this inversion was not completely accounted for in the design, and has led to an extra delay between the edges of the fourth VCO clock phase and their corresponding edges in the first clock phase, resulting in the increased bin size for ufToA 0 and 4. The difference between them is likely due to a difference in the rise and fall times of the inversion. The remaining structure is not observed in post-layout simulation, but the similarity between the two devices suggests that it is not due to process variation.

3.3 TDC time resolution

In a real application of Timepix4, the hit-time of each pixel can be reconstructed as

$$t_{\text{hit}} = \left(\text{cToA} - \frac{\alpha}{16} \, \text{fToA} - \frac{\alpha}{128} \, \Delta \text{ufToA} + \alpha\beta \right) 25 \, \text{ns} + \Delta t_{\text{pixel}} , \tag{3.3}$$

where $\Delta \text{ufToA} = \text{ufToA} - 4$ for hits arriving when the superpixel VCO has not yet been activated by earlier hits,[5] α is a correction factor that compensates for variation in the VCO frequency, β compensates the non-uniformity of the ultra-fine bins, and Δt_{pixel} is a per-pixel term that corrects

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[5]As detailed in section 2.1, this study is restricted to primary hits for which the ufToA-start code is invariably equal to 0000, which translates to a bin number of 4. The relationship between the ufToA code and its corresponding time bin number was shown in figure 7.
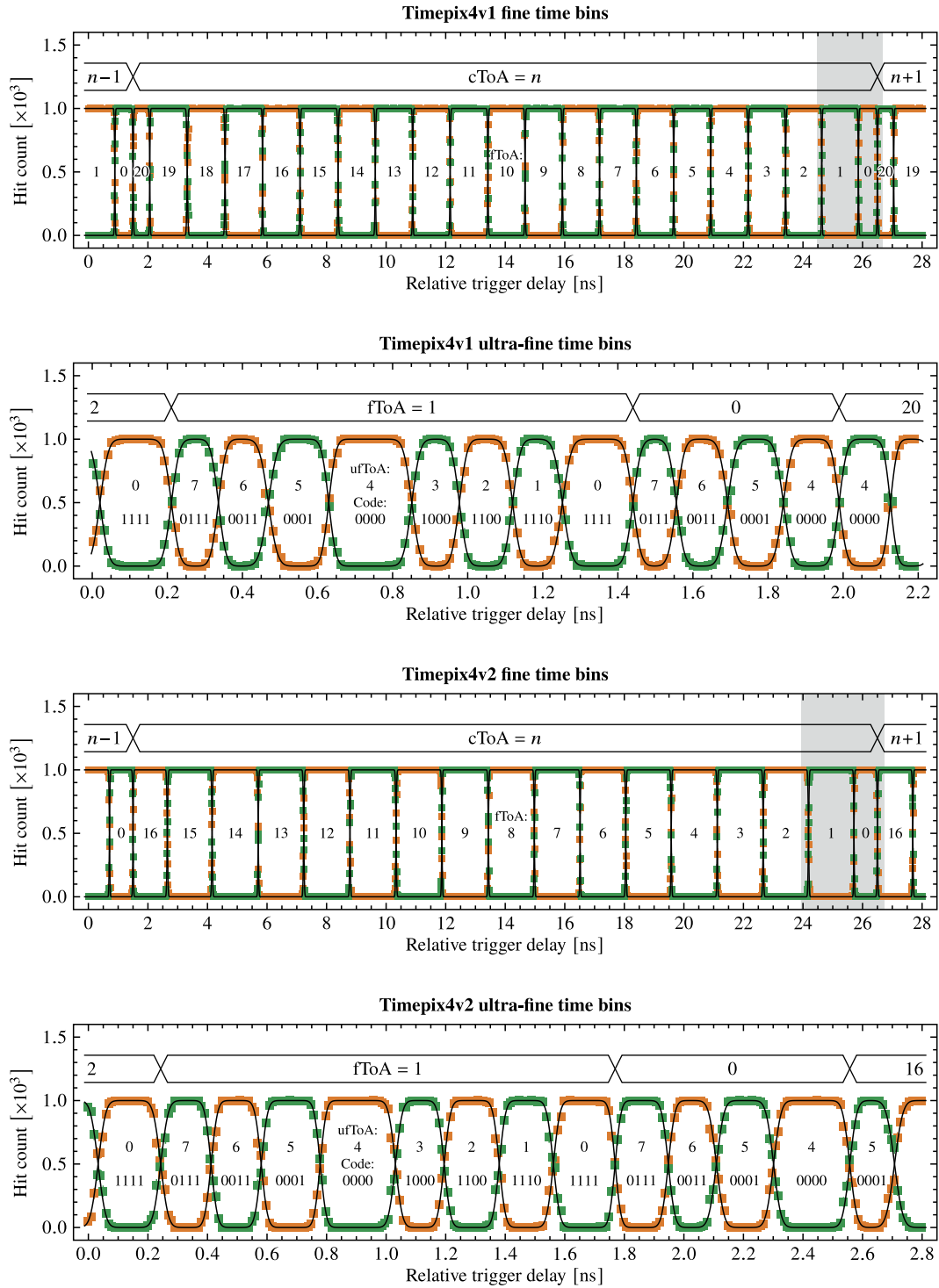
Figure 7. Number of hits in alternating bins as seen by a single pixel of a Timepix4v1 device (top two plots) and a Timepix4v2 device (bottom two plots) as a function of trigger delay for both types of time bins. The two datasets in each plot (orange and green points) correspond to the parity of an arbitrary sequential number that has been assigned to each time bin. Timepix4v1 has smaller time bins due to a design problem of the VCO, which has been fixed in Timepix4v2.
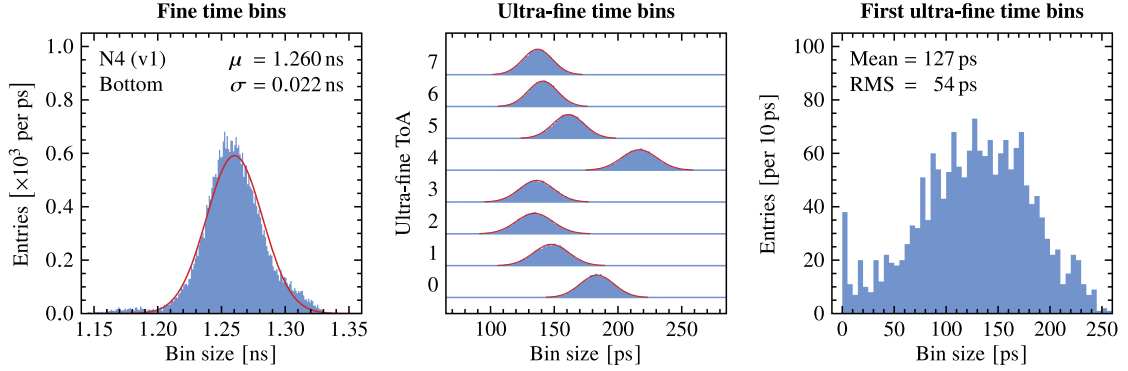
Figure 8. Distribution of fine time bin sizes the central fine time bins with $0 < \text{fToA} < 20$ (left), the ultra-fine time bins (centre), and the first bins before a rising edge of the 40 MHz reference clock (right) for the bottom half of a Timepix4v1 device.
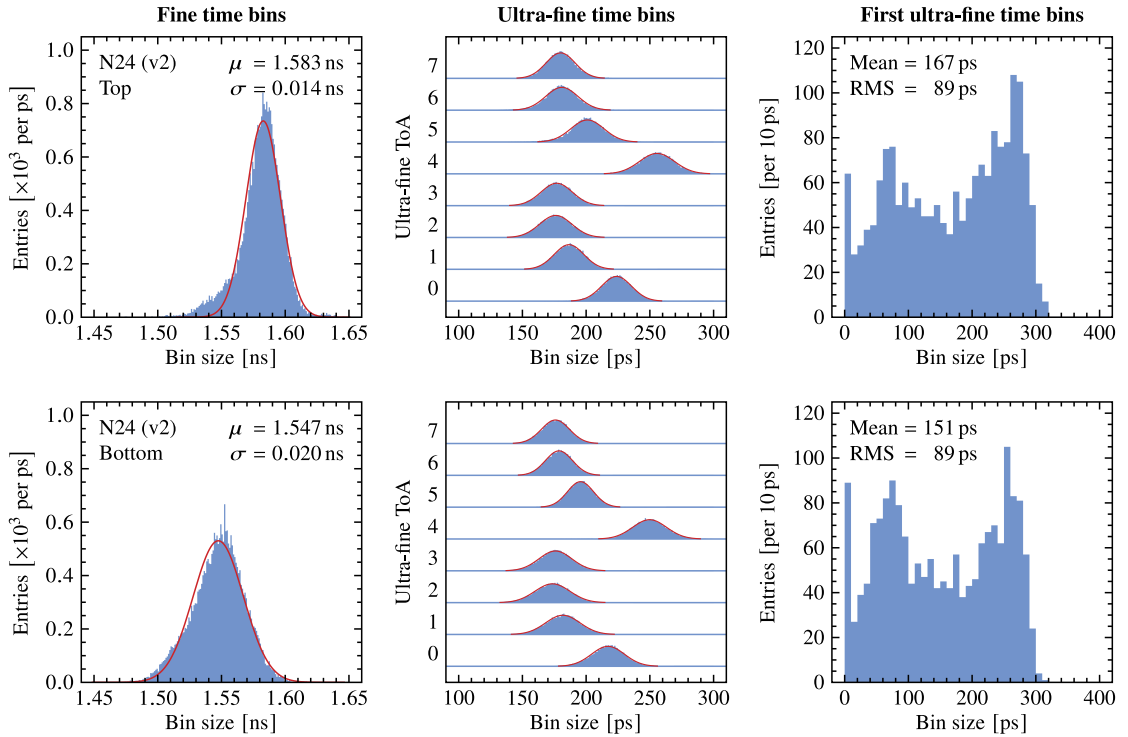

Figure 9. Distribution of fine time bin sizes the central fine time bins with $0 < \text{fToA} < 16$ (left), the ultra-fine time bins (centre), and the first bins before a rising edge of the 40 MHz reference clock (right) for the top and bottom halves of a Timepix4v2 device.

time offsets between pixels originating from differences in clock phase due to the reference-clock distribution. The latter also compensates for more subtle timing differences that originate from mechanisms such as variation in the capacitive loading of traces connecting the pixel front-ends to the superpixel VCO, as was observed in Timepix3 [7, 17].

To study the TDC resolution, the measured bin sizes are used to construct the expected time-residual distribution (with respect to an imaginary perfect time reference) under the assumptions that equation (3.3) is applied and that all time offsets between pixels have been calibrated out. Initially, three types of VCO frequency corrections are considered:

$$
\begin{array}{lll}
\text{(i)} & \text{chip-wide:} & \alpha \rightarrow \alpha_{\text{chip}}, \\
\text{(ii)} & \text{per matrix half:} & \alpha \rightarrow \alpha_{\text{half}}, \\
\text{(iii)} & \text{per VCO:} & \alpha \rightarrow \alpha_{\text{vco}},
\end{array} \tag{3.4}
$$

where the bin structure is ignored ($\beta \rightarrow 0$) for all cases because its overall contribution is negligible at the current stage. For a complete pixel matrix, the number of correction factors are 1, 2, and 29×10^3 (the number of superpixels), respectively. An additional correction is considered in order to demonstrate the impact of the bin structure on the TDC resolution:

$$
\text{(iv)} \quad \text{per VCO and ufToA:} \quad \alpha \rightarrow \alpha_{\text{vco}} \ \& \ \beta \rightarrow \beta_{\text{ufToA}}, \tag{3.5}
$$

which introduces 8 additional parameters with 7 degrees of freedom.[6]

The correction parameters are determined by minimising the standard deviation of the resulting time-residual distribution. The results are shown in figure 10. The best possible TDC resolution that can be achieved with the nominal TDC is 56.4 ps.[7] However, the observed bin structure limits the best possible resolution to 58.3 ± 0.9 ps, where the uncertainty is taken as the RMS value over the pixels. When no correction is applied ($\alpha \rightarrow 0$ and $\beta \rightarrow 0$), a TDC resolution of 111 ± 33 ps is observed. Introducing a chip-wide correction factor (i) only has a very minor impact on the TDC resolution (less than 1 %) because the mean VCO frequency is already very close to the design value of 640 MHz. Correcting the VCO frequency of both matrix halves individually (ii) gives a more pronounced improvement, resulting in a resolution of 80 ± 22 ps. Further improvement can be achieved by taking into account the frequency of each individual VCO (iii), resulting in a resolution of 61.9 ± 1.3 ps. Incorporating the bin structure (iv) gives an additional improvement of 2.6 %. Lastly, it is noted that the observed size variation in the first and last ultra-fine bins has not been taken into account in i–iv, and that doing so results in an improvement of 0.1 to 1 %.

Figure 11 shows how the TDC resolution is distributed over the pixels. It can be seen that methods i–ii both result in distributions with long tails towards worse TDC resolutions. For methods iii and iv it can be seen that the top half of the pixel matrix has a slightly worse resolution than the bottom half, which is due to the observed difference in the mean VCO frequency as was shown in figure 9.

3.4 Adjustable delay buffer calibration

In this study the reference-clock distribution (section 2.3) is used to control the clock phase with respect to the internally generated analog test pulses. The precision to which the clock phase can

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[6]It has been assumed that all pixel offsets are calibrated out which amounts to the constraint that $\sum_n \beta_n = 0$.

[7]This figure is defined by the variance of a rectangular distribution, $\sigma^2 = w^2/12$, with $w = 25$ ns/128.
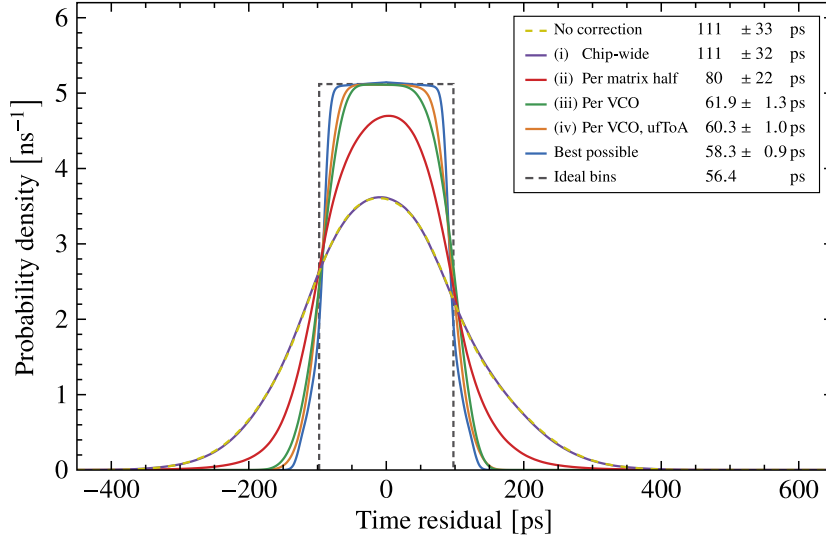
Figure 10. Expected time-residual distributions of the TDC based on the measured bin size structure of the Timepix4v2 device for various correction methods to compensate for VCO frequency variation and the ultra-fine bin structure. For each case the overall TDC resolution is presented in the legend, where the error indicates the RMS value over the pixels.
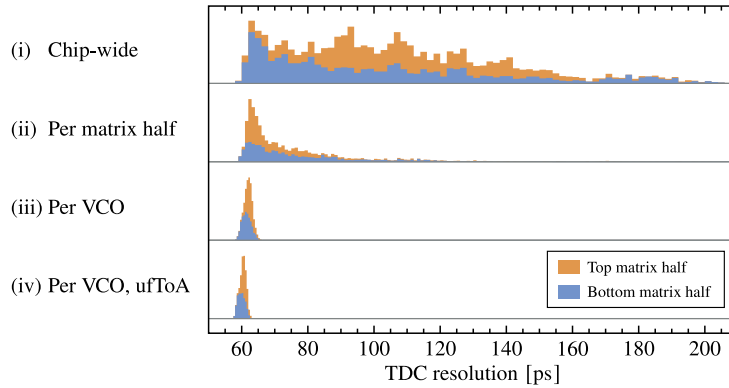

Figure 11. Distributions of the expected TDC time resolution over the pixels for three different methods of VCO frequency corrections.

be controlled depends on the number of ADBs that are enabled in the chain. For the measurements described in this paper, only the first four (out of 32) ADBs are enabled. For this configuration all pixels see the same change in clock phase when the DLL control code is changed because they receive their clock from the last 16 buffers in the chain. The DLL control code determines how many coarse- and fine-delay elements are enabled within each ADB. The lowest four bits of the control code are used to enable up to 15 fine elements, and the highest four bits are used to enable up to 14 coarse elements. The four enabled ADBs are characterised by performing the same measurement as described in the previous section for different control codes. The clock phase is observed as a shift in the bin edges t_n of equation (3.1).

Figure 12 shows the results for a single double-column structure, and distributions of the change

in clock phase for the coarse- and fine steps over all double-column structures. A discontinuity in the clock phase shift is observed between control codes 15 and 16 which is attributed to a slight discrepancy between the coarse- and fine-element delays. The precision to which the clock phase can be controlled in the current configuration is about 20 ps, and the total range that can be scanned with this calibration (DLL codes 0 to 31) is about 600 ps, which is sufficient for performing the analog front-end characterisation in the next section.
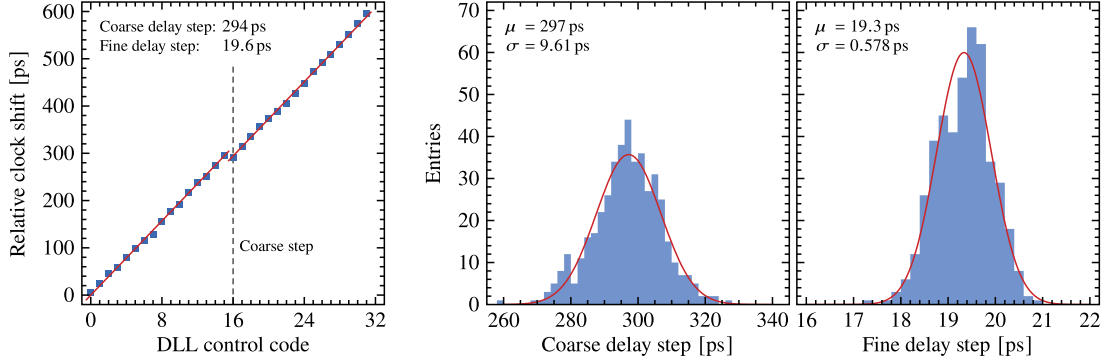

Figure 12. Reference-clock phase shift as a function of the DLL control code for a single double-column structure (left), and the delay step distribution over all double-column structures for the coarse (centre) and fine (right) delay sections of the four enabled ADBs.

4 Analog front-end measurements

In this section the analog front-end is characterised. First the pixel matrix is equalised in section 4.1, and then the preamplifier gain is determined in section 4.2 so that the threshold can be configured in terms of signal charge. In section 4.3 the time resolution of the analog front-end is measured as a function of signal charge and various DAC configurations are explored. Another important aspect of the timing performance is the systematic effect of signal size on the time measurement, which is the subject of section 4.4.

Unless stated otherwise, the measurements in this section are performed with the DAC configuration as shown in table 1, which is based on the values that are currently recommended by the Timepix4 manual for fast timing purposes. The bias voltage DACs are configured by tuning their outputs to the desired values using the integrated 12-bit sigma-delta ADC [22]. The measurements are performed using three Timepix4v1 devices (labeled N2, N4, and N8), and one Timepix4v2 device (N24). Devices N2 and N8 are bonded to a 300 μm planar silicon p-on-n sensor to provide a realistic input capacitance to the preamplifier.

4.1 Baseline equalisation

With Timepix3 the pixel-baseline equalisation is typically done by performing a threshold scan in the 10-bit counting acquisition mode for the minimum and maximum trim DAC values which control the pixel baseline. As the threshold level is increased, it moves through the noise that is superimposed on the baseline level where the number of threshold crossings peaks. The baseline

Table 1. DAC configuration of the Timepix4 devices.

Bias current DACs		Bias voltage DACs	
Name	Set value	Name	Output [mV]
VBiasADC	128	VCascDisc	550
VBiasDAC	65[a]	VCascPreamp	750
VBiasDiscPMOS	89	VControlVCO[b]	0
VBiasDiscTRAFF	128	VFBK	500/800[c]
VBiasDiscTailNMOS	83	VThreshold	Varied
VBiasIkrum	3	VTpulseCoarse	Varied
VBiasLevelShift	88	VTpulseFine	Varied
VBiasPreamp	85		

[a]Increased from recommended value of 47 to improve pixel equalisation

[b]Only used in the Timepix4v1 devices

[c]Electron/hole-collecting mode

level of each pixel is then taken as the peak position obtained by fitting a Gaussian to the number of threshold crossings as a function of threshold value.

Timepix4 has two frame-based counting modes that could be used to apply a similar method. However, both modes are affected by bugs which make it impractical to do so, and therefore a different method is applied. In this study the pixel-baseline equalisation of Timepix4 is performed in the data-driven 24-bit counting mode. In this mode the user sets a chip-wide counting threshold whose value is an integer multiple of 256. When the number of threshold crossings in a pixel reaches this value, it sends out a data packet and resets its counter. In this mode it is not feasible to measure a Gaussian profile of the noise since this would either lead to an impractically high data rate or a very limited counting resolution. The baseline is therefore obtained by determining two edges on either side of the noise profile of a pixel, and taking the midpoint as its baseline level.

To do so, two threshold scans are performed in opposite directions. For the first scan, all trim DACs are initialised to their lowest value, and the global threshold value is scanned in ascending order. For each threshold value the chip-wide counting threshold is set to 512, and the shutter is opened for 50 μs. When a pixel reaches a count rate of about 10 MHz it sends out a data packet, and the equalisation routine stores the current threshold DAC value as the left noise-edge for the current trim DAC value of that pixel. Then the trim DAC is incremented by one, which increases the baseline value of that pixel, and therefore reduces its count rate until the threshold reaches the same noise edge for a second time after the scan is resumed. At the end of the scan, the left noise-edges for all pixels and trim values are known, and the scan is performed in the opposite direction to find all right noise-edges. The baseline levels are then obtained by assuming a symmetrical noise profile and taking the midpoint between the left and right noise-edges.

A target baseline value is defined as the mean baseline level of the middle trim values (15 and 16). For each pixel the trim value is chosen such that its baseline distance to the target value is minimised. Figure 13 shows the equalisation results for device N4 for two different values of the bias-current DAC that controls the pixel trim range. Increasing this DAC from its recommended value of 47 to 65 increases the trim range from about 150 threshold-DAC units (or 83 mV) to 222 (123 mV), and reduces the fraction of pixels that cannot be equalised (because their required

trim values are out-of-range) from 2 % to 0.1 %. Doing so, however, also increases the baseline spread from 1.43 threshold-DAC units (0.797 mV) to 2.01 (1.12 mV). The baseline spread can be expressed in electrons by taking into account the gain, which is determined in the next section. The baseline spread for the default and increased trim range are 22 e and 30 e, respectively. All measurements in this study are performed with the increased trim range.
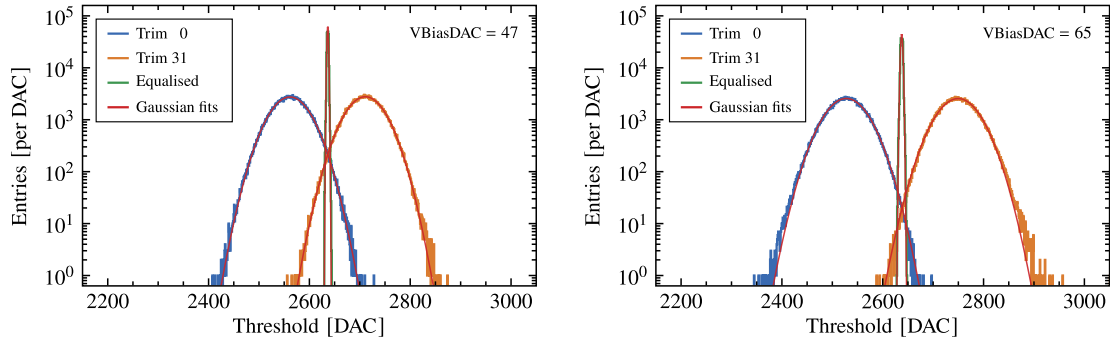

Figure 13. Pixel-baseline distributions of N4 before and after equalisation with the bias-current DAC at its recommended value of 47 (left) and 65 (right). The device was configured in the electron-collecting mode.

Figure 14 shows the mean left and right noise-edge level as a function of the pixel trim value. Error bars indicate the one-sigma pixel-to-pixel spread. The data of each pixel are aligned at the mean midpoint value of trim values 15 and 16. The increase in pixel-to-pixel spread towards trim values 0 and 31 reflects a divergence in the trim value dependence of the pixel baselines. The mean separation between the left and right noise-edge levels is 11.3 ± 0.5 mV, which corresponds to about 317 ± 15 e. This implies that the baseline spread could potentially be larger than 30 e. However, in the next section the baseline spread is determined by a different method with compatible results. Nevertheless, the equalisation method may still be improved by choosing a shorter shutter time or by increasing the counting threshold in order to reduce the separation between the two noise-edges. The measurements presented in the remainder of this paper are all performed with the equalisation performed as described above.
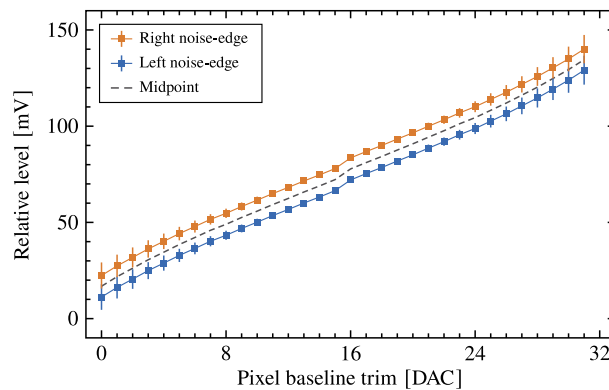

Figure 14. Mean noise-edge levels over the pixels as a function of pixel trim value.

4.2 Preamplifier gain

A measurement of the preamplifier gain is performed in order to control the threshold in terms of signal charge. This measurement is performed by means of a threshold scan in the data-driven ToA/ToT mode with test pulses enabled in order to inject 1000 signals with a controlled amount of charge. To control the amount of injected charge q, the two test-pulse DACs are tuned such that their potential difference is equal to q/C_{tp}, where C_{tp} is the nominal test-pulse coupling capacitance of 3.2 fF. By varying the amount of injected charge, the preamplifier gain can be determined.

Figure 15 shows the measured number of hits as a function of threshold level in a single pixel for injected charges ranging from 0.6 ke to 2 ke in steps of 100 e with the device configured in electron-collecting mode. For each scan the results are modelled as

$$n_{\text{hits}} = n_0 \, e^{-v_{\text{thr}}/\mu_v} + \frac{n_{\text{tp}}}{2} \left[1 - \text{erf}\left(\frac{v_{\text{thr}} - v_{\text{peak}}}{\sqrt{2}\,\sigma_v} \right) \right] , \qquad (4.1)$$

where v_{thr} is the threshold level, n_0 and μ_v are fit parameters used to model the noise edge at the lower threshold levels, n_{tp} is the number of test pulses, v_{peak} is the peak level of the preamplifier output, and σ_v is the voltage noise at the preamplifier output. The relationship between v_{peak} and the injected charge is determined by fitting equation (4.1) to the measurement data. Due to the limited data rate of the slow-control readout, this measurement is performed for only 896 pixels that are located roughly along the diagonals of the bottom and top halves of the pixel matrix.
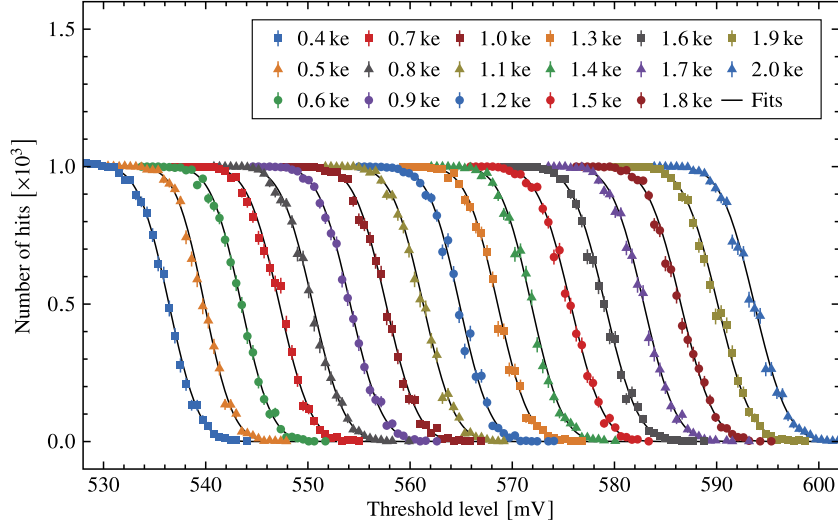

Figure 15. Threshold scan results from a single pixel of N24 for injected test pulses ranging from 0.6 ke to 2 ke measured in the electron-collecting mode.

Figure 16 shows the mean preamplifier peak-level (over the pixels) as a function of injected charge for all devices and both input polarities. The gain is modelled as

$$v_{\text{peak}} = v_{\text{b}} + q\,g , \qquad (4.2)$$

where v_{b} the baseline level, q the injected charge, and g the gain. In this paper the injected charge is always quoted by its absolute value so that $q > 0$, and the charge that is actually injected into the

front-end is understood to be of the correct sign for the relevant polarity mode. The observed mean gain is 35.0 mV/ke for collecting holes, and 35.5 mV/ke for collecting electrons. The observed pixel-to-pixel RMS of the gain ranges from 0.5 % to 0.9 %. In this study, the linear fits shown in figure 16 are used to determine the threshold levels.
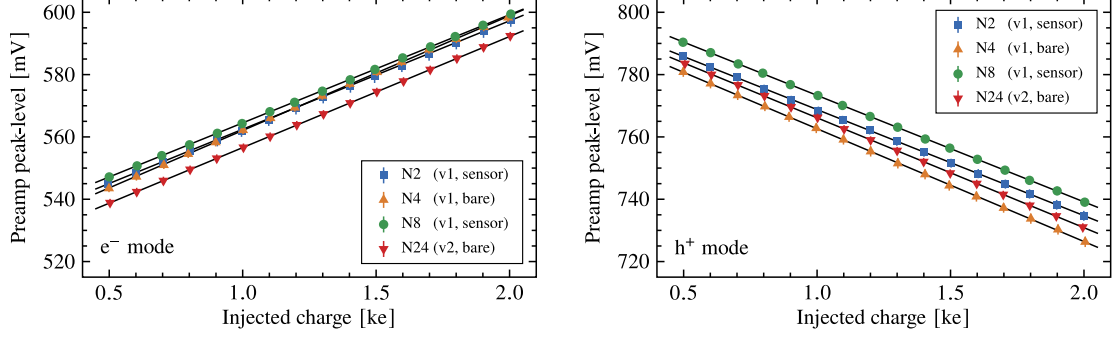

Figure 16. Preamplifier output peak-level as a function of injected charge for all devices configured in electron-collecting mode (left) and hole-collecting mode (right). Error bars indicate the pixel-to-pixel variation.

The baseline spread is determined by fitting equation (4.2) for each pixel separately and calculating the standard deviation of v_b. The result is divided by the mean gain to express the baseline spread in electrons. The results for all devices are presented in table 2. The baseline spread is compared to the value obtained from the equalisation as described in the previous section, and it can be seen that both measurements are in agreement. Lastly, the equivalent noise charge (ENC) is determined as σ_v/g, and is quoted in the rightmost column. It can be seen that devices N2 and N8 have an increased ENC, which is due to the additional input capacitance provided by the bonded sensors. Both devices are fully depleted, and no significant dependence on bias potential is observed.

Table 2. Gain measurement results for all devices used in this study. The baseline spread derived from these gain measurements is compared to the value obtained from the equalisation (eq.) method. Uncertainties indicate the pixel-to-pixel variation. A reverse bias potential of 100 V is applied to both sensors.

Device	Mode	Baseline spread [e] Gain meas.	Eq.	Gain [mV/ke]	ENC [e]
N2 (v1, sensor)	e^-	31	31	34.8 ± 0.2	81 ± 5
	h^+	29	28	-34.0 ± 0.3	74 ± 3
N4 (v1, bare)	e^-	30	30	36.8 ± 0.3	65 ± 2
	h^+	27	28	-36.2 ± 0.3	57 ± 2
N8 (v1, sensor)	e^-	28	28	34.7 ± 0.2	82 ± 4
	h^+	29	26	-34.2 ± 0.3	74 ± 4
N24 (v2, bare)	e^-	32	30	35.7 ± 0.2	69 ± 2
	h^+	29	28	-35.3 ± 0.2	62 ± 2

4.3 Analog front-end time resolution

The time resolution of the analog front-end (AFE) is characterised by measuring the cumulative ToA distribution of internally generated analog test pulses which inject a controlled amount of charge at the preamplifier input. The cumulative ToA distribution is measured by recording the number of hits that arrive in or before each time bin while varying the reference-clock phase using the configurable delays in the clock distribution system as described in section 3.4. Figure 17 shows the results of four different pixels for different amounts of charge as measured with device N4 in the electron-collecting mode. As the clock is delayed, test pulses can be seen to arrive earlier (relative to the clock) as more of them end up in time bins with larger fToA and ufToA values.
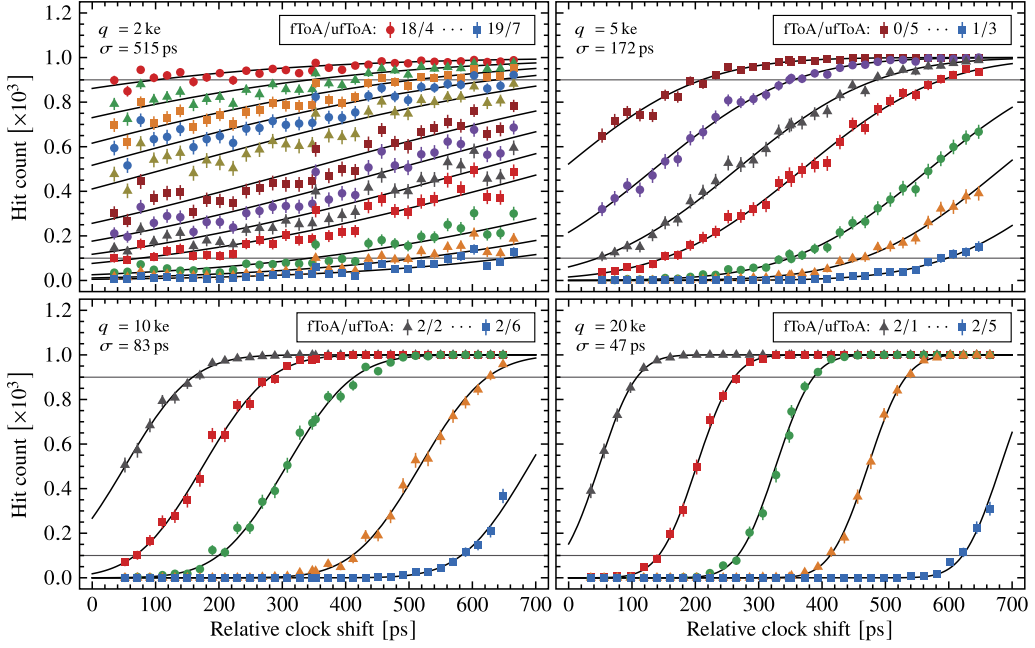

Figure 17. Number of hits in single pixels of device N4 that arrive in or before consecutive time bins as a function of the relative clock shift for four different amounts of injected charge in the electron-collecting mode. The horizontal grey line at $y = 100$ indicates the minimum number of hits that are required at the maximum clock shift for a time-bin edge to be included in the analysis, and the line at $y = 900$ indicates a maximum at the minimum clock shift.

For each amount of charge and pixel a simultaneous fit is performed by minimising

$$\chi^2 = \sum_{i,j} \left[\frac{N_{ij} - f(t_j, t_i, \sigma_t)}{\sigma_{ij}} \right]^2 , \tag{4.3}$$

where N_{ij} is the number of hits that arrived in or before the i-th time bin at the j-th step in the clock delay, f is the function defined by equation (3.1), t_j is the j-th clock delay, t_i is the right-edge location of the i-th bin, σ_t is the time resolution (which is the quantity of interest), and lastly, σ_{ij} is the statistical uncertainty that N_{ij} out of N_{tp} test pulses arrive before the edge located at t_i. This uncertainty is defined by

$$\sigma_{ij}^2 = \frac{N_{ij} (N_{tp} - N_{ij})}{N_{tp}} , \tag{4.4}$$

which is the variance of a binomial distribution: $np(1 - p)$, with $n = N_{tp}$ and $p = N_{ij}/N_{tp}$. Note that equation (4.4) requires that only data points with $0 < N_{ij} < N_{tp}$ are to be involved in the minimisation of equation (4.3) to ensure that $\sigma_{ij}^2 \neq 0$. Furthermore, in order to ensure that the edge locations are well-defined, edges are only included in the fit when they satisfy $N_{ij} < 900$ at the start of the clock-delay scan range ($j = 0$) and $N_{ij} > 100$ at the end of the scan range ($j = 31$). Note that σ_t becomes large compared to the scan range for small amounts of injected charge (top left plot in figure 17). Its value, however, is still well-constrained by the data because N_{tp} is fixed to 1000.

Figure 18 shows the measured time resolution of the AFE as a function of injected charge. Firstly, it can be seen that the additional input capacitance from a bonded sensor has a significant impact on the time resolution. For the hole-collecting mode, the time resolution is limited due to an upper bound to the current with which the first amplifier stage can discharge its capacitive load, as was explained in section 2.1. The AFE resolution levels off to a value of 105 ± 7 ps, and therefore it would dominate the total time resolution (obtained by including the TDC resolution) of 122 ± 6 ps. In the electron-collecting mode, however, the AFE resolution keeps improving (roughly exponentially) with signal charge, and the total time resolution is dominated by the TDC for signals larger than 15 ke for the bare devices. For the bonded device the break-even point is expected to be about 22–23 ke based on the trend.
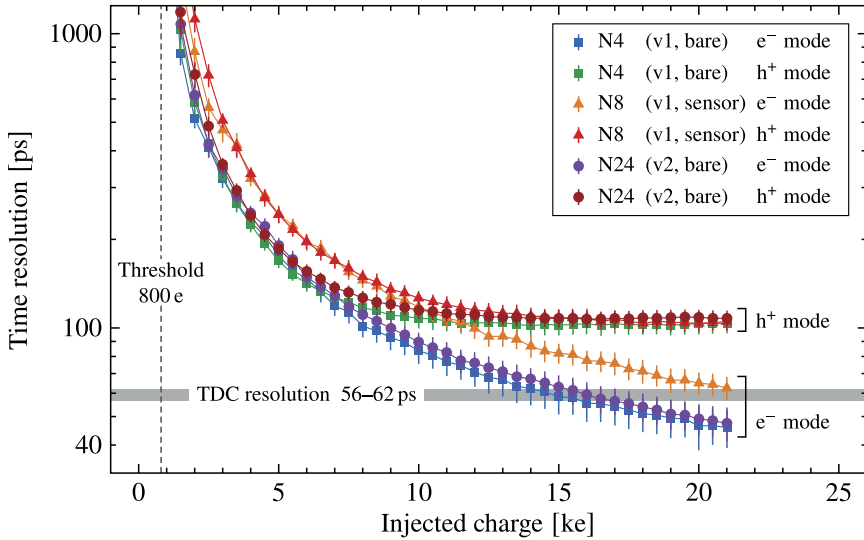

Figure 18. Mean time resolution of the analog front-end as a function of injected charge for various devices and both polarity modes. Errors bars indicate the pixel-to-pixel variation in the time resolution. The TDC resolution is also indicated, assuming that VCO frequency variation is corrected on at least a per-VCO basis, and that time offsets between pixels are calibrated out.

The preamplifier rise-time can be decreased by increasing the preamplifier bias current, which can potentially improve the AFE time resolution. A scan of the preamplifier bias-current DAC is performed in order to study the change in time resolution, and the results are shown in figure 19. In the electron-collecting mode, setting the DAC to its maximum value improves the AFE resolution by about 21–38 %, depending on the signal charge and input capacitance. Increasing the bias current is more effective for lower signal charge and higher input capacitance. In the hole-collecting

mode, the AFE resolution improves by about 35–42 %, without a clear dependence on charge and capacitance. The improvement, however, comes at the expense of a significant increase in power consumption. In the electron-collecting mode, the total power consumption, as measured by the SPIDR4 system, increases linearly from 4.1 W at the default bias current to 6.0 W at the maximum value. The hole-collecting mode shows a similar increase from 3.8 W to 5.6 W.
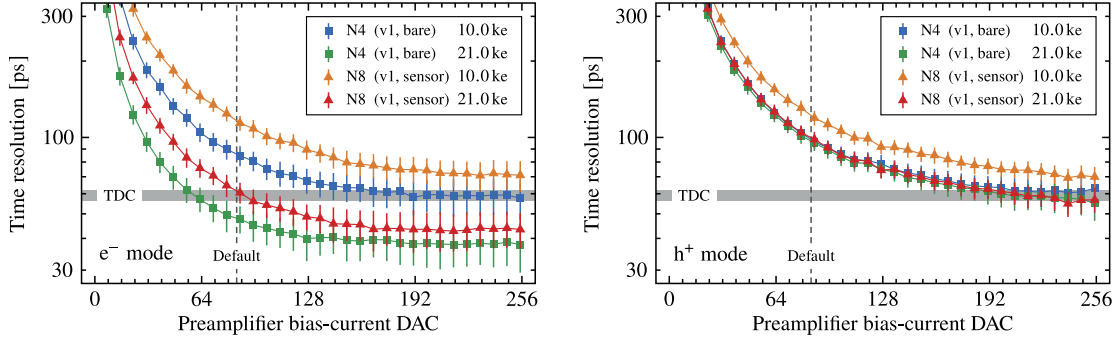

Figure 19. Mean time resolution of the analog front-end as a function of the preamplifier bias-current DAC for various amounts of injected charge with the devices configured in electron- (left) and hole-collecting mode (right). Errors bars indicate the pixel-to-pixel variation in the time resolution.

Figure 20 Shows the AFE time resolution as a function of threshold for the hole-collecting mode. The AFE resolution expresses a clear minimum whose location depends on both signal charge and input capacitance. For instance, the bare device (N4) has a minimum at a threshold of roughly 2.5 ke for a signal charge of 10 ke whereas the bonded device (N8), which has a larger input capacitance, has a minimum at a threshold of about 2 ke. Furthermore, it can be seen that the minimum of device N8 also increases with signal charge. This also seems to happen for device N4, but it is not so clear due to the limited threshold range used in the measurement. The mechanism behind this improvement can be found most likely in the slew rate of the preamplifier output. The time resolution is approximately related to the noise at the preamplifier output σ_v from equation (4.1) by

$$\sigma_t = \frac{\sigma_v}{dv/dt} , \qquad (4.5)$$

where dv/dt is the slew rate of the preamplifier output at the threshold level. By changing the threshold, the maximum slew rate can be found to optimise the time resolution.

Considering the threshold dependence in the electron-collecting mode (shown in figure 21), it is observed that the AFE time resolution shows a slight improvement when increasing the threshold up to a value of about 1 ke. At higher thresholds, however, many pixels develop a substantially worse AFE resolution, producing a tail in the distribution. On an individual pixel basis, the AFE resolution appears to peak at some pixel-specific threshold before subsequently improving again as the threshold is increased further. This effect is observed for all devices tested in this study, and the thresholds at which the AFE resolution peaks show no clear structure, do not depend on the column or row position, and also differ among the devices. The effect is currently not understood, and requires further investigation.

Based on additional front-end simulations, a modified DAC configuration was suggested to improve the timing performance. The preamplifier bias-current DAC, which was studied above, is
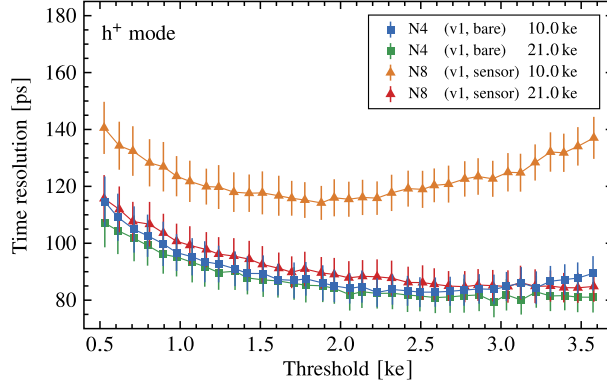
Figure 20. Time resolution of the analog front-end as a function of threshold for various amounts of injected charge measured in the hole-collecting mode. Error bars indicate the pixel-to-pixel variation.
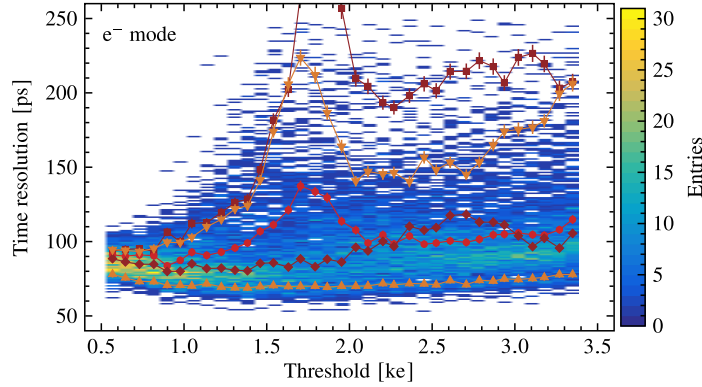

Figure 21. Distribution of the time resolution of the analog front-end as a function of threshold measured with device N4 at a signal charge of 10 ke in the electron-collecting mode. The data points show the resolution of five individual pixels. For thresholds above 1 ke there is a significant pixel-to-pixel variation in the time resolution.

increased from 85 to a value of 135. In addition, the VBiasDiscPMOS DAC is increased from 89 to 135, and the VBiasDiscTRAFF is decreased from 128 to 64. This modified DAC configuration shows no significant impact on the gain and ENC measurements presented above. The improvement in AFE resolution of the Timepix4v2 device is shown in Figure 22. In the electron-collecting mode, the modified configuration improves the AFE resolution by about 25 to 30 % for signals up to 8 ke. For larger signals, the improvement decreases linearly to about 3 % at 21 ke. The point at which the TDC starts dominating the total front-end time resolution is lowered to 12 ke. In the hole-collecting mode, the resolution improves by 25 to 30 % overall, and it now levels off to a value of 75 ± 5 ps. The improved time resolution comes at the cost of an increase in power consumption by 14 % from its baseline figure of 4.1 W in the electron-collecting mode, and by 20 % from its baseline figure of 3.8 W in the hole-collecting mode.
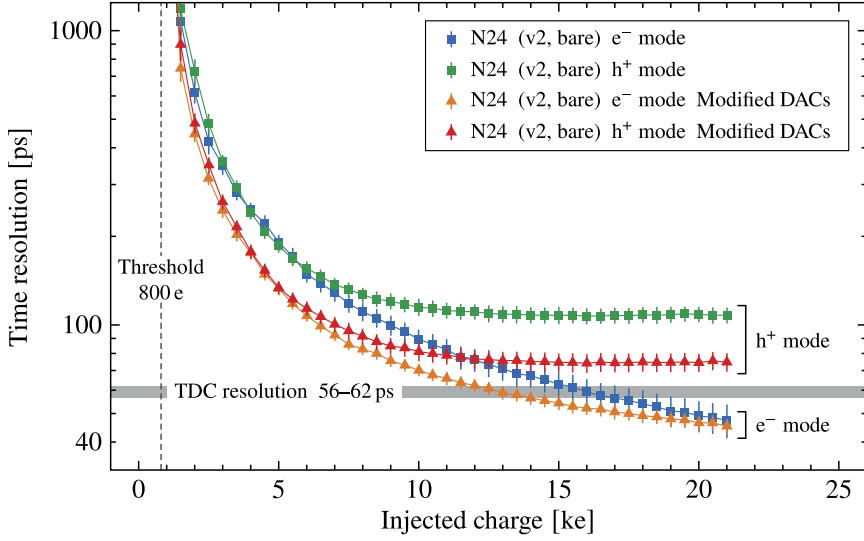
Figure 22. Comparison of the mean analog front-end time resolution between two DAC configurations. Errors bars indicate the pixel-to-pixel variation in the time resolution. The TDC resolution is also indicated, assuming that VCO frequency variation is corrected on at least a per-VCO basis, and that time offsets between pixels are calibrated out.

4.4 Timewalk

In the previous section the analog front-end time resolution was determined as a function of injected charge. In most applications the number of electron-hole pairs that are generated in the sensor material will fluctuate from one event to another—colloquially referred to as Landau fluctuations. The resulting time resolution will therefore depend on the particular charge distribution of the events. Moreover, the time resolution will be negatively affected by an additional mechanism that comes into play when combining time measurements that are performed with distinct amounts of charge: Lower-charge measurements will be systematically later than higher-charge measurements. This effect, known as *timewalk*, can be corrected by means of the time-over-threshold (ToT) measurement, which is performed alongside the time-of-arrival (ToA) measurement of each hit. The ToT is a surrogate measure of the signal charge, and it can be mapped to a correction term by either a model or a lookup table.

The relationship between injected charge and ToT is shown in figure 23. For a given amount of injected charge, a pixel-to-pixel variation in ToT is observed. This is a consequence of variation in the discharge current of the feedback capacitor onto which the signal is integrated. For injected charges larger than 2 ke, the pixel-to-pixel RMS of the ToT ranges from 11 to 15 % in the electron-collecting mode, and from 7 to 9 % in the hole-collecting mode. This effect is expected, and a per-pixel calibration is required when the ToT is used to measure signal charge or particle energy. The relative uncertainty of these measurements is determined by the relative ToT resolution, which is also shown in figure 23. It improves from about 10 % at a signal charge of 2 ke to 5 % at 3.5 ke. For signals of 21 ke the relative ToT resolution is about 1 %. The absolute ToT resolution ranges from about 40 to 90 ns depending on the polarity mode, the input capacitance, and the signal charge. The absolute ToT resolution worsens as the signal charge increases. The modified DAC settings

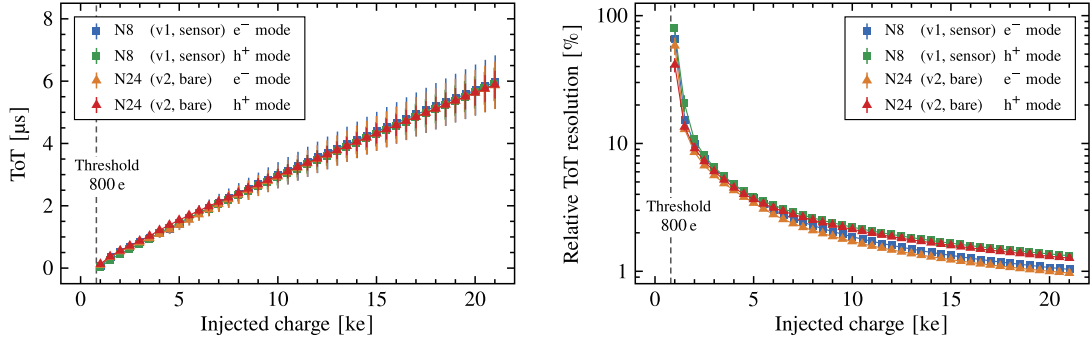specified in section 4.3 have no significant impact on these results.

Figure 23. Mean time over threshold (left) and the mean resolution (right) as a function of injected charge for two devices in both polarity modes. Error bars indicate the pixel-to-pixel RMS.

The timewalk can be extracted from the measurements of the previous section by tracking the change in time-bin locations t_i from equation (4.3) as a function of injected charge. Figure 24 shows the mean timewalk over the pixels for various devices in both collection modes. The pixels are time-aligned for a signal charge of 21 ke. The error bars indicate the pixel-to-pixel timewalk variation, and disappear at 21 ke as a result of the time alignment. The pixel-to-pixel variation can be seen to increase as the amount of injected charge decreases, which reflects a divergence in the timewalk curves of the individual pixels. In the electron-collecting mode, the timewalk behaves approximately as 75 ps/ke at a signal charge of 21 ke. For the modified DAC configuration, defined in section 4.3, the timewalk behaves as 50 ps/ke. It is also observed that the hole-collecting mode suffers from less timewalk than the electron-collecting mode, which is probably related to the difference in gain. For the hole-collecting mode, it can also be clearly seen that the bonded device (N8) has more timewalk, which may be expected as additional input capacitance typically reduces the bandwidth of an amplifier [23], though the effect is not so apparent in the electron-collecting mode.

5   Conclusion and outlook

A characterisation of the Timepix4 timing performance has been performed. The pixel TDC in the digital front-end of Timepix4 has been studied using externally generated pulses that were synchronised with the 40 MHz reference clock. Externally generated pulses have also been used to calibrate the column DLLs, which distribute the reference clock over the pixel matrix. This allowed for the characterisation of the analog front-end using internally generated analog test pulses by making it possible to control their arrival time with a step size of about 20 ps.

It has been shown that the high VCO frequency has been fixed in Timepix4v2. The time bins are not completely uniform in size, but there are adjustment mechanisms available for both the PLL in the periphery and the individual VCOs in the pixel matrix that can potentially improve the time-bin uniformity. These are still to be tested. However, the non-uniformity only has a minor impact (less than 1 %) on the time resolution of the TDC. It has been shown that, depending on how the VCO frequency variation is handled in the timestamp reconstruction, a TDC time resolution
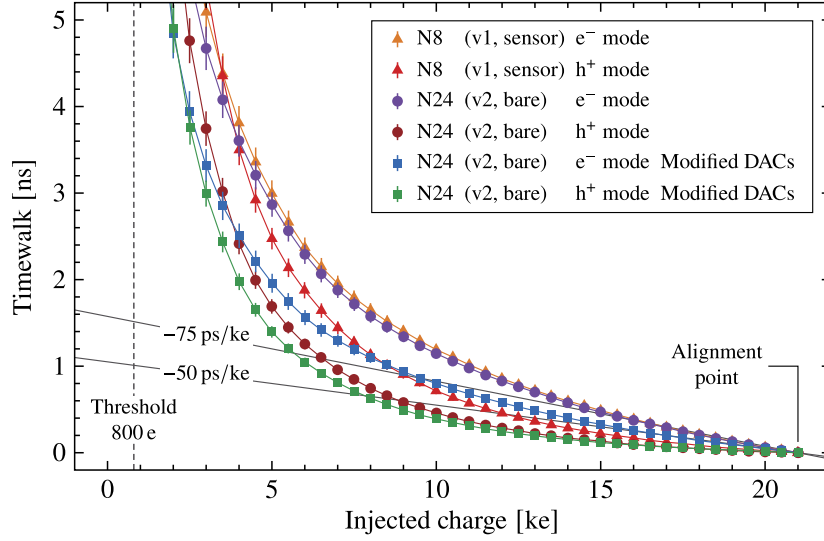
Figure 24. Timewalk obtained by tracking the shift in time bins for various devices.

ranging from about 58 ps to 80 ps can be achieved. A TDC resolution of 62 ps is likely attainable with a moderate calibration effort.

The pixel baselines have been equalised with a pixel-to-pixel spread of less than 32 e. The fraction of pixels that cannot be equalised because their baselines deviate too much from the majority is reduced from 2 % to 0.1 % by increasing the bias-current DAC that controls the trim range from the default value of 47 to 65.

Internally generated analog test pulses have been used to measure the preamplifier gain by injecting controlled amounts of charge and determining the peak level of the preamplifier response. The observed mean gain is 35.5 mV/ke in the electron-collecting mode, and 35.0 mV/ke in the hole-collecting mode. The ENC has been determined in the same measurement. For the bare devices an ENC ranging from 57 to 69 e is observed, depending on the polarity mode. The bonded devices have a higher ENC ranging from 74 to 82 e due to the additional input capacitance from the sensor.

A characterisation of the analog front-end time resolution has been performed. For both polarity modes, the analog front-end time resolution shows the same signal-charge dependence up to values of about 6–9 ke. Beyond this point, however, the resolution levels off to 105 ± 7 ps in the hole-collecting mode whereas it keeps improving in the electron-collecting mode, eventually reaching values of 47 ± 7 ps and 62 ± 6 ps at an injected charge of 21 ke for the bare and bonded devices, respectively. The injectable charge is limited to this value by the internal DACs that define the test-pulse amplitude, and it is clear that the time-resolution still shows a tendency to improve with increasing charge. However, for these large signals the TDC will be the dominating contribution to the total front-end time resolution.

An alternative DAC configuration has been shown to improve the analog front-end time resolution. In the electron-collecting mode, this alternative DAC configuration improves the analog front-end time resolution by 25 to 30 % for signals up to 8 ke, and the point at which the TDC starts dominating the total front-end resolution is lowered from 15 ke to 12 ke. This comes at the cost of

an increase in power consumption of 14 %. In the hole-collecting mode, the analog front-end time resolution improves by 25 to 30 % overall, and the limiting resolution improves from 105 ± 7 ps to 75 ± 5 ps at an increase in power consumption of 20 %. For hole-collecting sensors it could also be worthwhile to experiment with the threshold level. For fixed amounts of injected charge, the analog front-end time resolution expresses a clear minimum, which can potentially improve the resolution by up to 30 ps depending on the amount of charge and the efficacy of the applied timewalk correction.

Finally, to put these results into perspective, an electron-collecting version of the 3D-silicon sensor that was mentioned in the introduction is considered. For this sensor, it has been observed that a perpendicularly incident beam of minimally ionising particles generates a charge distribution that peaks at 22 ke and has a FWHM of about 9 ke [7]. Ignoring the tail towards higher charges, the signal charge can be approximated to follow a Gaussian distribution with a standard deviation of about 3.8 ke. Based on the measurements presented in this paper, the analog front-end time resolution for such a charge distribution is expected to have a lower limit of around 62 ps, which is the resolution of device N8 at 21 ke. Furthermore, a TDC resolution of 62 ps is taken into account, resulting in a lower limit for the best achievable front-end time resolution of about 88 ps. It is also important, however, to consider the effect of timewalk. The timewalk approximately behaves as 50–75 ps/ke at a charge of 21 ke. Taking into account the 3.8 ke standard deviation of the charge distribution, it follows that timewalk alone will contribute about 190–285 ps to the total time resolution, which would make the front-end time resolution insignificant. Methods to correct for timewalk should therefore be studied in more detail when test-beam measurements are performed.

Acknowledgments

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