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Mohammad Sedghi for the CMS Collaboration

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The Fast Beam Condition Monitor as standalone luminometer of the CMS experiment at the HL-LHC

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Abstract: For the Phase-2 CMS upgrade for the High-Luminosity LHC, a luminosity uncertainty of 1% is targeted. To achieve this goal, measurements from multiple luminometers with orthogonal systematics are required. A standalone luminometer, the Fast Beam Condition Monitor (FBCM) is being designed for the online bunch-by-bunch luminosity measurement. Its fast timing properties also enable the measurement of beam-induced backgrounds. In this paper, the hardware architecture and the readout protocol of the FBCM is described. The expected performance with a simple behavioral model of the front-end comprising a constant fraction discriminator is discussed, although the final implementation in the ASIC is still under discussion. Simulation results show that the FBCM will provide the required statistical uncertainty and deviation from linearity by employing 336 silicon-pad sensors, each with an area of about 3 mm^2. In addition, the front-end with sensitivity to at least 6000 electrons will satisfy the longevity constraints for an exposure of 1 MeV neutron equivalent fluence of 3.5×10^{15} per cm^2.

Keywords: Front-end electronics for detector readout, Models and simulations

Contents

1 Introduction

A fast beam condition monitor (FBCM) is being designed as a standalone luminometer to run independently of the CMS central trigger and data acquisition systems at the HL-LHC and to provide a bunch-by-bunch luminosity measurement in real time. The ultimate goal of 1% luminosity uncertainty after final calibration requires a negligible statistical error on the calibration constant, the visible cross-section and a deviation from linear response of less than 0.02%/(Hz/μb) up to an average pileup of 200 [1]. To meet this goal, the FBCM will utilize 336 silicon-pad sensors with a zero-counting algorithm of the observed hits and it will provide the time of arrival (ToA) and the time over threshold (ToT) of the signal pulses with a few ns resolution. The FBCM will have a semi-digital readout to transfer these data to the back-end, with the front-end chip producing a non-clocked output pulse upon the creation of an ionising signal in the silicon-pad sensor.

The FBCM will be divided into four quarters, as shown in Figure 1 (right), where one quarter covers one half at one end of the detector. In the baseline design, each quarter of FBCM comprises four front-end modules, each one is connected to an inner tracker port card [2] for data transmission and for connection to the power supply. It is proposed to install the FBCM behind disk 4 of the Tracker Endcap Pixel Detector system, close to the bulkhead, corresponding to $8 < r < 30$ cm and $277 < |z| < 290$ cm, as illustrated in Figure 1.

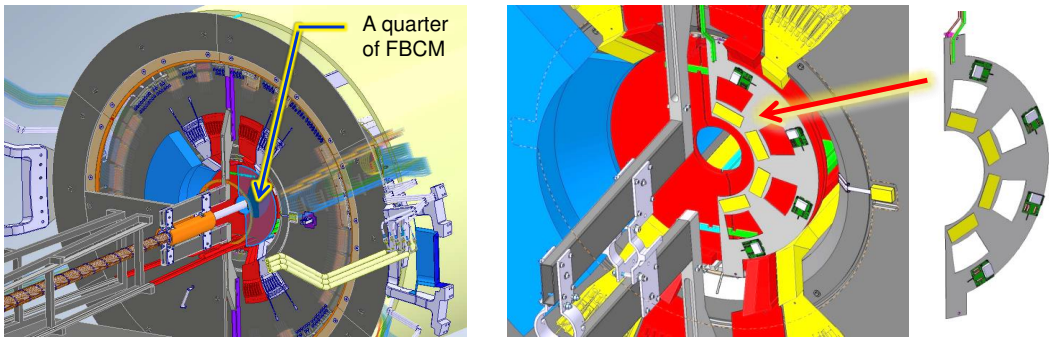

Figure 1. The proposed location for FBCM behind the last disk of the Tracker Endcap Pixel Detector. A quarter of the FBCM is shown in the right in which the the front-end modules and the port cards are visible.

2 Readout electronics

The readout chain for a channel is depicted in Figure 2. Once a hit is received on a silicon-pad sensor, the collected ionization charge produces a short pulse. The signal will be amplified and shaped in the front-end ASIC, then a non-clocked digital output pulse will be produced which is transmitted to the lpGBT (Low Power GigaBit Transceiver [3], an ASIC widely used for data transmission and control in the Phase-2 projects) via flex cables called e-links. The lpGBT continuously samples the output signal of the front-end channels every 0.78 ns corresponding to the e-link speed (1.28 Gbps). Then the data will be sent to the back-end by versatile optical link transceivers (VTRx+) [4]. At the back-end, an ATCA (Advanced Telecommunications Computing Architecture) digital processing unit makes histogram of the number of hits per bunch-crossing per sensor and performs labeling the ToA and the ToT after synchronizing to the LHC clock. The timing information will be used for beam-induced background measurement. By counting the number of zero-hit occurrence, known as the zero-counting method, the hit rate and consequently, the luminosity will be calculated. The FBCM ASIC design is planed to be launched in early 2022, and it will make the best use of existing 65 nm electronic building blocks.

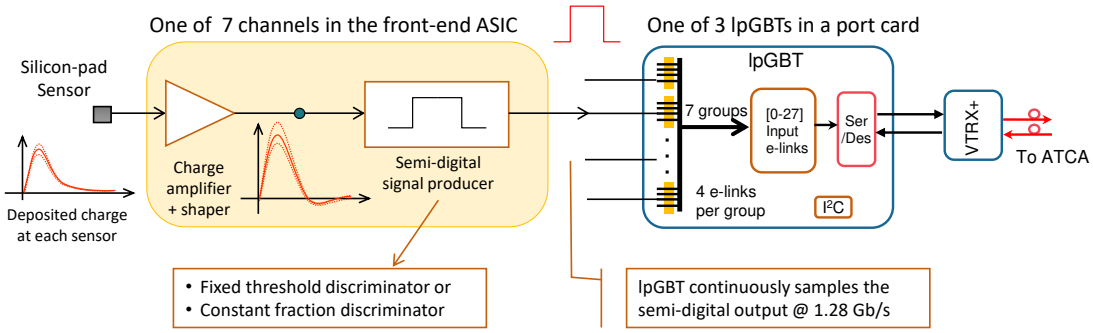

Figure 2. A simple diagram for only one channel shown the readout chain and data transmission. Each lpGBT supports 7 channels and each port card includes 3 lpGBTs. There will be four port cards per quarter. Thus, each quarter of the FBCM supports 84 channels, leading to 336 silicon-pad sensors for the FBCM.

3 Front-end ASIC

The requirements on the analog part of the FBCM front-end ASIC are similar to the current BCM1F ASIC [5] which include an analog amplifier, shaper, and a discriminator to produce a non-clocked semi-digital signal. The output carries the ToA and ToT information, so that the ASIC would be compatible with a readout over the Phase-2 pixel electronics. The FBCM front-end ASIC will be designed such a way that the ToT is maintained below 25 ns. This feature makes it compatible with high data rate applications that are needed for linearity for a luminometer. The front-end ASIC will be designed in 65 nm technology to benefit from building blocks already developed by CERN EP/ESE and other collaborators for Phase-2 projects. The ASIC would be capable of adjusting the thresholds to tune the rising edge at the signal peak. The discriminator in the ASIC could be either a constant fraction discriminator (CFD) or a fixed-threshold discriminator with time-walk compensation. The choice between these two architectures will be made during the engineering design stage, taking into account performance and existing ASIC building blocks in

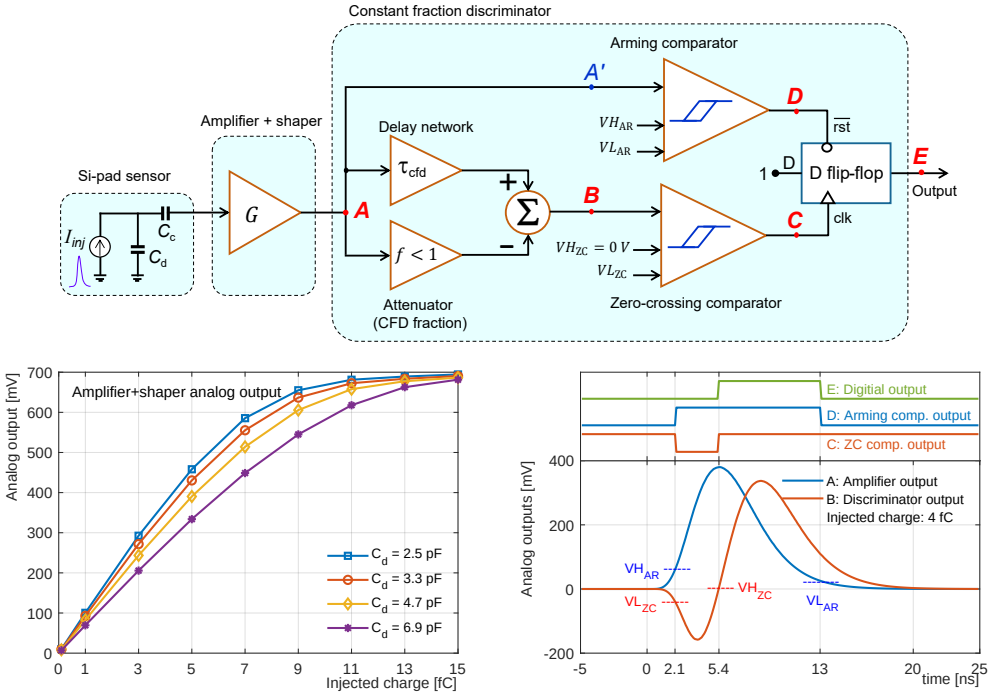

Figure 3. Block diagram of the front-end model developed for the FBCM ASIC, employing an amplifier followed by a constant fraction discriminator. C_c and C_d: coupling and sensor capacitance, G: amplifier gain, τ_{cfd} and f: CFD shaping network delay and the fraction parameter, VL_x and VH_x: lower and upper thresholds of a hysteresis comparator at which its output become low and high respectively. Signal at nodes A (A') and B are in differential pairs, but for simplicity are shown with single lines. Additional optional amplifier and shaper could be placed between A-A' that are not shown here. The bottom-left panel depicts the output voltage at node A as function of accumulated injected charge. The bottom-right panel shows the variation of signals at nodes A–E with respect to the time, assuming a sensor size of 2.89 mm^2 with collected chage of 4 fC wherein $C_c = 315$ pF, $C_d = 2.5$ pF, $\tau_{cfd} = 2$ ns, $f = 0.53$, $VL_{ZC} = -42$ mV, $VH_{ZC} = 0$ mV, $VL_{AR} = 25$ mV and $VH_{AR} = 60$ mV.

the 65 nm technology that can be adopted for use in the FBCM ASIC. In this paper, the results of a hypothetical front-end ASIC with a CFD is reported as a case-study.

Front-end with a CFD as a case-study

In order to evaluate the effects of the front-end ASIC on the detector performance, the behavioral model of various blocks of the front-end electronics was implemented with C++ programming embedded in CMSSW, the CMS software framework [6]. Here, an ASIC model based on CFD is simulated using the transfer function of each block. The simulation model includes a fast analog transimpedance amplifier followed by a post-amplifier and shapers, similar to the BCM1F front-end ASIC [5] with peaking time < 7 ns and peak to the baseline less than 14 ns, as well as a CFD block inspired by the VFAT3 architecture [7]. Figure 3 illustrates a simplified block diagram of the front-end. The simulated output of the amplifier as a function of injected charge is depicted in Figure 3 (bottom-left), showing a linear relationship up to 6 fC with a gain of $G \approx 100$ mV/fC. The delay (τ_{cfd}) and the fraction (f) in the CFD block are two parameters used for amplitude-

independent analog peak detection. Figure 3 (bottom-right) shows simulated signals at nodes ***A*** and ***B*** in Figure 3. Two hysteresis comparators (assuming non-inverting ones), namely zero-crossing (ZC) and arming (AR), are employed to feed the clock (clk) and the active-low reset ($\overline{\text{rst}}$) inputs of a positive edge-triggered D-type flip-flop. The lower (VL) and the upper (VH) thresholds in a non-inverting hysteresis comparator are adjustable parameters, so that the comparator output becomes high when its input voltage (v_i) is larger than VH and returns to the low state when v_i < VL. The lower threshold of the zero-crossing and the arming comparators, namely VL_{ZC} and VL_{AR}, adjust the cut-off for the amount of collected charges and the duration of output pulse (i.e., ToT) respectively. With an appropriate setting of parameters, the CFD block produces an asynchronous pulse, rising at the peak of received signal and lasting for the duration of ToT. Eight different sensor sizes were considered for CMSSW simulations, and for each case, f was set to a value for which the zero crossing occurs at the peak of signal and VL_{ZC} was tuned so that the front-end model was sensitive to signals with collected charges >1 fC (≈6000 electrons).

4 Simulation results

In [8], it has been shown that very large sensors sizes (> 8 mm^2) are not practical, because the large sensor capacitance leads to long-lasting pluses. In this study, an upper limit of 8 mm^2 was considered, corresponding to the maximum input capacitance of 7 pF for the front-end ASIC. Eight sensor sizes, as labeled in the vertical axis of Figure 4, and positions at different r, spanning the range from 8 to 20 cm, were studied. The final sensor area will be optimized during the engineering design of the FBCM detector. The linearity of the FBCM measurement as a function of average pileup, ⟨PU⟩, was evaluated with CMSSW simulations in which the front-end electronics was modeled as described in Section 3. Figure 4 [1] shows the deviation from linearly and the statistical uncertainty as a function of various combinations of sensor sizes and radius with ⟨PU⟩ = 200 corresponding to the leveled instantaneous luminosity of 7.5×10^{34} cm^{-2} s^{-1}. The results show that there is a trade-off between statistical uncertainty of rate and the linearity, where the linearity becomes worse for large sensors located at lower radii close to r = 8 cm. Assuming sensor sizes equal to 2.89 mm^2 at r = 14.5 cm and with front-end parameters mentioned in the captions of Figure 3, the statistical rate uncertainty per second and the deviation from linearity could be reached as 0.18% and 0.1%, respectively, on average pileup of 200.

5 Conclusion

The FBCM ASIC was modeled by using a transfer function of building blocks, including a fast analog amplifier with 14 ns settling time from peak to baseline, shapers and a constant fraction discriminator (CFD) with the capability of adjusting the thresholds to tune the rising edge to the signal peak. The pulse width of the semi-digital output is a monotonic function of the signal amplitude, which is also beneficial to monitor the MIP amplitude spectrum and thus the sensor's radiation damage. Simulation results also show that the FBCM will provide the required statistical uncertainty and deviation from linearity by employing 336 silicon-pad sensors, each with an area of about 2.89 mm^2. In addition, the front-end with sensitivity to at least 6000 electrons will satisfy the longevity constraints for an exposure of 1 MeV neutron equivalent fluence of 3.5×10^{15} per cm^2.

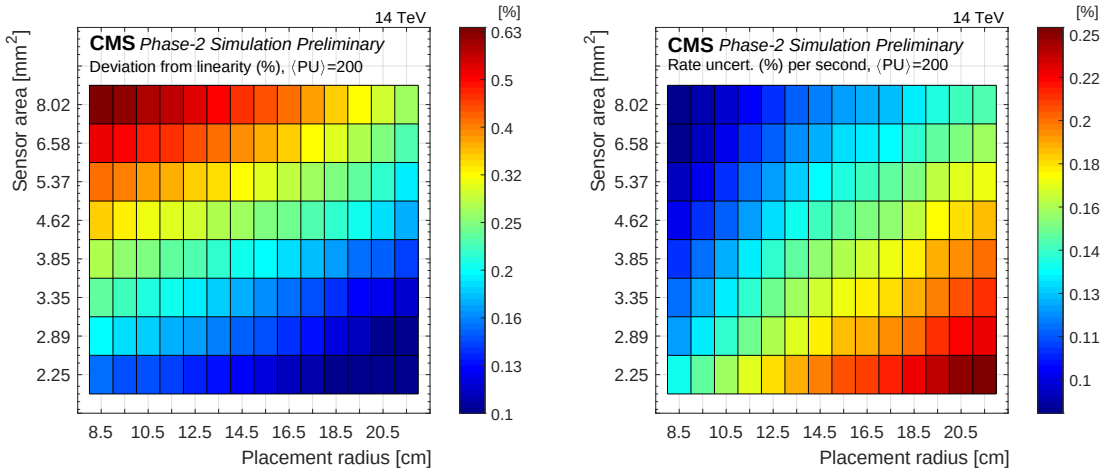

Figure 4. Deviation from linearity (left), statistical uncertainty in the rate (right) evaluated at average pileup 200, for different sensor sizes and placement radii, assuming 336 sensors in FBCM. For better illustration, the color bars are presented in logarithmic scale.

Acknowledgments

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References

[1] CMS collaboration, *The Phase-2 Upgrade of the CMS Beam Radiation Instrumentation and Luminosity Detectors*, Tech. Rep. CERN-LHCC-2021-008, CMS-TDR-023, CERN, Geneva (2021).

[2] CMS collaboration, *The Phase-2 Upgrade of the CMS Tracker*, Technical Design Report CERN-LHCC-2017-009, CMS-TDR-014, CERN, Geneva (2017).

[3] P. Moreira et al., *The lpgbt: a radiation tolerant asic for data, timing, trigger and control applications in hl-lhc*, in *Topical Workshop on Electronics for Particle Physics*, 2019, https://indico.cern.ch/event/799025/contributions/3486153/.

[4] J. Troska, A. Brandon-Bravo, S. Detraz, A. Kraxner, L. Olanterä, C. Scarcella et al., *The VTRx+, an optical link module for data transmission at HL-LHC*, *PoS* **TWEPP-17** (2017) 048. 5 p.

[5] D. Przyborowski, J. Kaplon and P. Rymaszewski, *Design and performance of the BCM1F front end ASIC for the beam condition monitoring system at the CMS experiment*, *IEEE Trans. Nucl. Sci.* **63** (2016) 2300.

[6] CMS collaboration, *CMS Physics: Technical Design Report Volume 1: Detector Performance and Software*, Tech. Rep. CERN-LHCC-2006-001 ; CMS-TDR-8-1, CERN, Geneva (2006).

[7] D. Abbaneo et al., *Design of a constant fraction discriminator for the VFAT3 front-end ASIC of the CMS GEM detector*, *JINST* **11** (2016) C01023.

[8] M. Sedghi, *Fast Beam Condition Monitor of the CMS experiment at HL-LHC*, in *International Conference on Technology and Instrumentation in Particle Physics*, no. CMS CR-2021/111 in TIPP, 2021.