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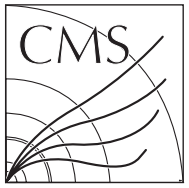

The Compact Muon Solenoid Experiment

Conference Report

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Readout and Trigger Electronics for the Triple-GEM Detectors of the CMS GE2/1 System

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Abstract

The Triple Gas Electron Multiplication (GEM) technology has been adopted for the upgrade of the forward muon detector system at the CMS experiment for the future High-Luminosity phase of the Large Hadron Collider (LHC) at CERN. The GE2/1 subdetector comprises 72 chambers that will be installed after the second LHC Long Shutdown. The GE2/1 chambers are segmented in 4 modules with 12 sectors in each module, and each sector is composed of 128 radial strips. The strips are read out by the front-end VFAT3 ASIC. It has 128 channels, each with a charge sensitive preamplifier, shaper and a discriminator. Each module is equipped with the OptoHybrid (OH) board that provides the readout and trigger interfaces for 12 VFAT3 ASICs. The OH board uses CERN designed GigaBit Transceivers (GBT) for the readout path. VFAT3 ASICs also provide trigger information that allows the OH to build trigger clusters using the Xilinx Artix-7 FPGA and to transmit this cluster data the back-end Trigger Processor and to the local Cathode Strip Chamber Trigger Motherboard to improve local trigger efficiency at an early stage of the trigger processing. The back-end electronics will use the ATCA Trigger Processor farm; it will send the data to the Endcap Muon Track Finder and to the CMS DAQ system. In this presentation, we report on progress on the GE2/1 electronics and results from the first demonstrator tests performed at CERN in 2019, and we outline our future design and production plans.

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Readout and Trigger Electronics for the Triple-GEM Detectors of the CMS GE2/1 System

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ABSTRACT: The Triple Gas Electron Multiplication (GEM) technology has been adopted for the upgrade of the forward muon detector system at the CMS experiment for the future High-Luminosity phase of the Large Hadron Collider (LHC) at CERN. The GE2/1 subdetector comprises 72 chambers that will be installed after the second LHC Long Shutdown. The main goal of these chambers is to improve muon momentum measurements and triggering capabilities in the $1.6 < |\eta| < 2.4$ pseudo-rapidity region. The GE2/1 chambers are segmented in 4 modules with 12 sectors in each module, and each sector is composed of 128 radial strips. The strips are read out by the front-end VFAT3 ASIC. It has 128 channels, each with a charge sensitive preamplifier, shaper and a discriminator. Each module is equipped with the OptoHybrid (OH) board that provides the readout and trigger interfaces for 12 VFAT3 ASICs. The OH board uses CERN designed GigaBit Transceivers (GBT) for the readout path. VFAT3 ASICs also provide trigger information that allows the OH to build trigger clusters using the Xilinx Artix-7 FPGA and to transmit these clusters to the back-end Trigger Processor and to the local Cathode Strip Chamber Trigger Motherboard to improve local trigger efficiency at an early stage of the trigger processing. The back-end electronics will use the ATCA Trigger Processor farm; it will send the data to the Endcap Muon Track Finder and to the CMS DAQ system. In this presentation, we report on progress on the GE2/1 electronics and results from the first demonstrator tests performed at CERN in 2019, and we outline our future design and production plans.

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[1]Speaker

1. Introduction

The CMS Collaboration at CERN's Large Hadron Collider is preparing to install three new muon detectors in the forward endcap regions. They are based on triple Gas Electron Multiplication (GEM) technology and are called GE1/1, GE2/1, and ME0 [1]. The system described in this paper, GE2/1 (where "G" stands for the GEM, "E" stands for the Endcap, "2" stands for the 2nd muon station from the Interaction Point (IP), and "1" stands for the 1st ring of chambers from the beam line), improves muon momentum measurements and trigger capabilities in the $1.6 < |\eta| < 2.4$ pseudo-rapidity region in conjunction with the Cathode Strip Chambers (CSC) in station ME2/1 (Fig.1, left).

Triple GEMs have 3 foils made of 50 µm thick polyimide and coated on both sides with 5 µm of copper; each foil is perforated with holes (Fig.1, right). Four gaps are filled with a gas mixture of 70% Ar + 30% CO_2. A high voltage difference, on the order of 1 kV, is applied to each gap. An incoming muon ionizes gas in the drift gap, electrons are multiplied during transfer due to an avalanche, and the charge is collected at the bottom of the induction gap in strips. The ions recombine at the cathode. The total electron gain is ~10^4.

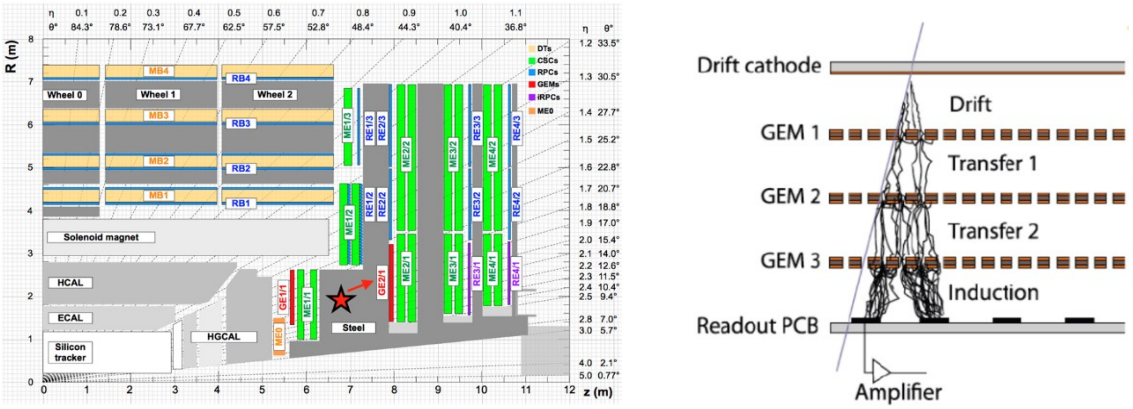

Figure 1: CMS with GEM detectors (left) and the basic principle of GEM operation (right)

Each GE2/1 trapezoidal chamber spans a 20-degree region and consists of four independent modules M1-M4 (Fig.2, left). Each module is assembled from drift and readout boards, external and internal frames, and sets of GEM foils. It has 12 sectors, and each sector is composed of 128 radial strips. The intrinsic spatial resolution of GEM detectors is of the order of 100 µm, time resolution is better than 10 ns and a rate capability of ~10^5 Hz/cm^2. There will be 72 GE2/1 chambers, arranged as 18 "staggered" super-chambers in each CMS endcap (Fig.2, right). The dimensions of M5-M8 modules on the "front" chamber are slightly different from the ones of M1-M4 on the "back" chamber to avoid gaps in the GE2/1 acceptance. The total number of readout channels is 72 chambers x 4 modules x 12 sectors x 128 strips = 442,368.

The GEM-based muon detectors provide both tracking and trigger capabilities. Simulations show that with 140 pile-up collisions, the probability to have more than 5 trigger clusters in one GE2/1 module is ~10^{-5}. Assuming 13 bits per cluster and 5 clusters per bunch crossing, the required trigger bandwidth is below 3 Gbps. For the tracking data, one GBTx ASIC [2] can handle 6 VFAT3 ASICs [3]. The total integrated dose in the GE2/1 area will be well below 10 kRad for an integrated luminosity of 3000 fb^{-1} [1].

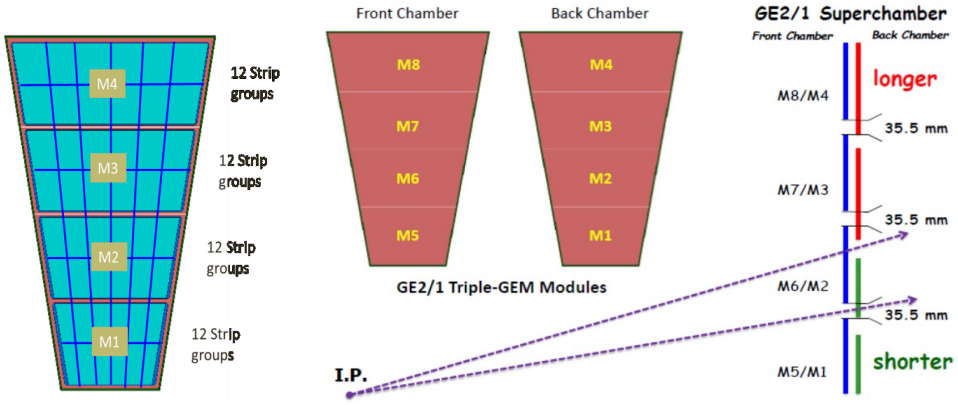

Figure 2: GE2/1 readout regions (left) and super-chamber design, top and side views (right)

Among three GEM projects at CMS, the GE2/1 follows the GE1/1 project, which is in a much more advanced state of design. We use the experience, technical solutions, software and firmware developments of GE1/1, but take into account all the specifics of GE2/1 chambers, especially their larger size (GE2/1 active readout area is 1.45 m^2 or three times larger than that of GE1/1). Initial testing and integration of all electronic parts have been done within the demonstrator project. The goals of the demonstrator are the following: to verify soundness of the mechanical design and mechanical interfaces; to design, build and integrate all the prototypes of electronics for one GE2/1 chamber; to evaluate electronics performance, to measure noise levels, and to optimize the grounding scheme of the detector.

2. GE2/1 DAQ and Trigger Electronics

A block diagram of the target GE2/1 DAQ and Trigger system is shown in Fig.3 (left). Each module is equipped with its own OptoHybrid (OH) boards with the DAQ/Trigger optical interfaces to the ATCA processor (GBT links, shown in blue) and Trigger links to the CSC Optical Trigger Motherboard (OTMB) in the ME2/1 region. Timing, Trigger and Control (TTC) information is distributed through the DAQ and Timing Hub (DTH). Trigger links from the ATCA processor are also routed to the Endcap Muon Track Finder (EMTF).

The Readout Board (ROB) is a 2-sided trapezoidal printed circuit board. One side is facing the gas volume and has copper strips where the charge is induced. Signals are routed to the other side where the connectors to rigid-flex PlugIn cards are located (Fig.3, center). Each PlugIn card carries the VFAT3, a CERN-designed ASIC with 128 channels of charge sensitive amplifier, shaper and discriminator [1]. The VFAT3 has been designed specifically for the GEM readout. It has a DAQ path compatible with the CERN designed radiation hard GBTx ASIC, and a separate 8-bit Trigger path. The VFAT3 supports up to 2 MHz L1Accept rates and has a latency of more than 20 μs. On top of the ROB resides the GEM Electronic Board (GEB). It provides power, as well as all of the electrical connections between 12 VFAT3 ASICs and the OH board. Also it serves as shielding for the detector. The flex part of the PlugIn card absorbs residual misalignment of the GEB vs ROB and provides a much more reliable connection in comparison with the assembly of VFAT3 ASICs directly on a large and thin (1 mm) GEB board.

The OH board resides in the centre of the GEB board and utilizes two GBTx ASICs. Unlike the GE1/1 OH which serves two modules (24 VFAT3 ASICs), the GE2/1 OH serves only one

module (12 VFAT3 ASICs) and because of this it can use a smaller and cheaper Xilinx Artix-7 FPGA and more reliable mechanical connection with the GEB. The FPGA is needed only to reconstruct trigger clusters and transfer them to the backend processor and to the CSC OTMB. Radiation hard VTTX and VTRX optical parts [4] designed at CERN are used for optical transmission. The same OH design fits all the M1-M8 GEB boards.

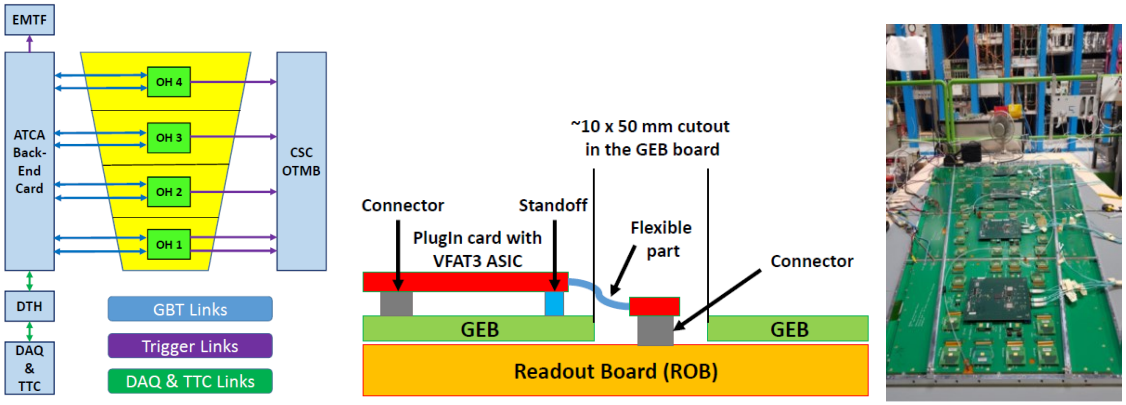

Figure 3: Block diagram of the GE2/1 electronic system (left); connections between electronic boards (center); GE2/1 demonstrator at CERN (right)

There will be 3456 PlugIn cards in the system; 288 ROB and 288 GEB boards of 8 types; 288 OH boards. The total number of DAQ (based on GBTx ASIC) optical links is 576. We will need 8 future backend ATCA processors for the entire GE2/1 system.

3. First GE2/1 Demonstrator Tests at CERN in 2019

The GE2/1 demonstrator detector has been set up in the building 904 at CERN (Fig.3, right), next to the GE1/1 and CSC electronics test stands to simplify the integration. Initially, four M1-M4 detectors with the OH boards were installed. Each GEB is equipped with the VFAT3 pluggable boards borrowed from the GE1/1 system (as of this writing, we don't have a prototype version of the GE2/1 PlugIn card yet). Low voltage power for all VFAT3 and OH boards is provided by five radiation hard FEAST DC-DC converters [5] residing on each GEB board. DAQ and trigger optical links from all OH boards are connected to a µTCA CTP7 processor [6].

A set of GE1/1 software tests was tailored for the GE2/1 detectors. The basic GBTx phase scan for all VFAT3 ASICs checks all the GBT links. It demonstrates a wide "safe window" of operation. All links on all prototype boards are fully functional. The "window" varies for each GEB board due to different lengths of traces. A phase scan is done with 10K repeated register read operations of three VFAT3 registers after each phase has been set. DAC scans are used to determine optimal settings for multiple DAC registers in each VFAT3. A latency scan determines the ratio of events with detected hits over the total number of events per different latency values. The latency is the time difference (in bunch crossings (BX), each LHC bunch crossing is equal to ~25 ns) between the time of arrival of an L1Accept signal and the time at which the related event was recorded. Finally, S-curves measure the response of the channel to an injected pulse calibrated to a given charge at a given threshold. It shows at which amplitude of the calibration pulse a signal becomes visible. S-curves can be converted into Equivalent Noise Charge (ENC) values to characterize the noise of each channel.

All modules show an expected latency peak at 33 BX. First measurements of ENC are ~0.2 fC without the chamber attached (i.e. with a capacitive load of 0 pF) and below 0.8 fC with the chamber, but without high voltage. These tests are in progress.

Various grounding schemes have been studied and the ultimate low-noise configuration has been found, where the chamber frame is connected to the lab ground with a thick braid. The proper GEB shield layer grounding appears to be the key point.

4. Conclusions and Plans

Two GE2/1 chambers, one front and one back (8 modules in total, without DAQ electronics) were fully assembled, tested and mechanically integrated in 2019. Designs of most critical electronic prototypes of M1-M5 GEB boards are completed, boards fabricated, assembled and integrated within the first demonstrator at CERN. Boards M6-M8 will be fabricated and tested in the Fall of 2019. Firmware and software developments are largely based on the GE1/1 project which is well ahead of the GE2/1.

The Technical Design Report [1] states that the GE2/1 OH is based on a new low-power LpGBT ASIC. However, we found the production schedule of the LpGBT to be incompatible with the GE2/1 electronics production schedule. So we have decided to use two GBTx devices instead on the production OH board for DAQ purposes. One proposed change for the final OH design is to use one of these two devices in a "wide-bus" mode that allows higher user bandwidth and the ability to embed trigger information into the GBTx path. We could remove the dedicated optical links to the backend processor then. This idea is currently being evaluated.

We expect to produce and test the PlugIn card with the packaged VFAT3 ASIC by the end of 2019. One GE2/1 chamber will be installed alongside the ME2/1 CSC at the test stand at CERN to take cosmic data. We plan to finalize all electronic designs for the GE2/1 chambers in 2020.

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