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Front-end hybrid designs for the CMS Phase-2 upgrade towards the production phase

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Abstract

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Front-end hybrid designs for the CMS Phase-2 upgrade towards the production phase

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ABSTRACT:

Sixteen thousand 2S front-end hybrids and twelve thousand PS front-end hybrids will be produced for the CMS Tracker Phase-2 upgrade. The hybrids consist of flip-chips, passives and mechanical components mounted on a flexible substrate, laminated onto carbon-fibre stiffeners with thermal expansion compensators. In the prototyping phase, several critical issues have been solved to manufacture these complex circuits. Final designs are now reaching readiness for the full-scale production. Lessons learned during the prototyping phase and different improvements implemented for manufacturability will be presented in this contribution.

KEYWORDS: Manufacturing; Digital electronic circuits; Data acquisition circuits; Analogue electronic circuits

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1. Introduction of the CMS Phase-2 upgrade

The CMS Tracker Phase-2 upgrade is required to adapt the CMS detector [1] to the 4000 fb^{-1} total integrated luminosity and 14 TeV centre-of-mass energy of the HL-LHC. Two main types of silicon detector modules are being developed for the upgrade: Strip-Strip (2S) and Pixel-Strip (PS). The modules are arranged in different structures, in order to minimize the required number of sensors while maintaining sufficient detector performance. The 2S modules are arranged on ladders while the PS modules are mounted on structures called "rings" and "planks" with various angles. These structures are then mounted in the Tracker Barrel to form the core track finding element of the detector. In the end-cap structure of the detector, the modules are arranged in a different way. Due to these structures, the dimensional constraints of the hybrids are imposed. The arrangement of modules is illustrated in Figure 1.

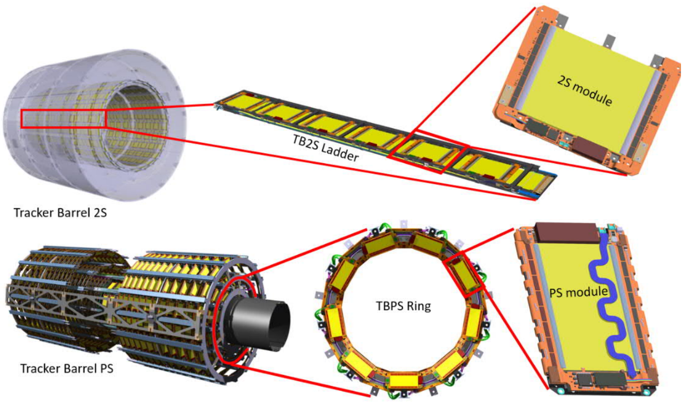


Figure 1 The arrangement of the different types of modules in the Outer Tracker.

The requirements for the electronics are driven by the detector performance needs and are very demanding: low mass, up to 2032 analogue channels on a single hybrid, Carbon-Fibre (CF) reinforcement for matching with the Coefficient of Thermal Expansion (CTE) of the silicon sensors and high thermal conductivity, reliable operation up to 15 years and radiation tolerance. In total, 5592 PS modules and 7608 2S modules will be constructed for the upgrade.

The 2S module consists of two parallel strip sensors, wirebonded to two front-end hybrids (2S-FEH). The wirebond pads on these hybrids are routed to the analogue inputs of eight CMS Binary Chips (CBC) that are processing the signals from these sensors.

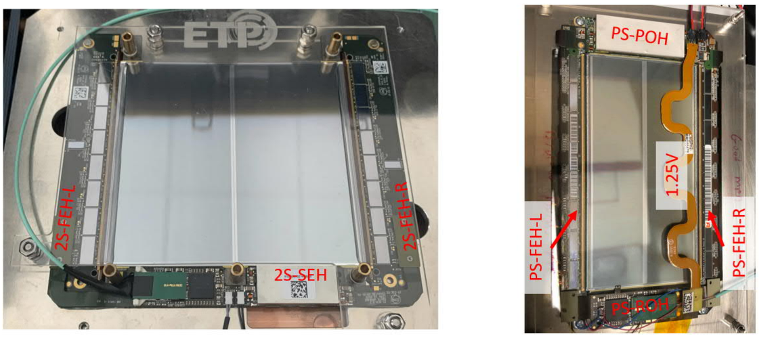


Figure 2 A 2S module prototype (left) and a PS module prototype (right).

The FEHs are then connected to a service hybrid (2S-SEH) with high density connectors in order to transfer the data to the back-end and provide powering and control signals. The three hybrids are then mounted on support structures and glued into the module assembly.

In the PS modules the sensor sandwich is constructed from a strip sensor and a macro-pixel sensor assembly with eight Macro Pixel ASICs (MPA). There are two front-end hybrids (PS-FEH) in this module as well, but the powering is provided by a dedicated hybrid (PS-POH) separate from the one that provides the data communication (PS-ROH) with the back-end. In case of PS modules, the hybrids and the sensors are glued on a CF baseplate during module assembly. A prototype of each module type is shown in Figure 2.

2. Evolution of 2S and PS Front-End Hybrid prototypes

The architecture and construction of the different front-end hybrids is the result of a long-term development with several milestones, but several difficulties as well. This development is described in the sub-sections below.

2.1. Evolution of the 2S-FEH

The first prototype of the 2S-FEH was manufactured in 2012, using a six-layers build-up on a rigid substrate, with the early prototype of the front-end ASIC for the 2S modules called CBC2 [2]. This first prototype had two of these ASICs, therefore it was named 2CBC2 (Figure 3). Mechanical prototypes with eight ASICs were designed later and they showed excessive bend due to the CTE mismatch caused by the ASICs on the weak substrate.

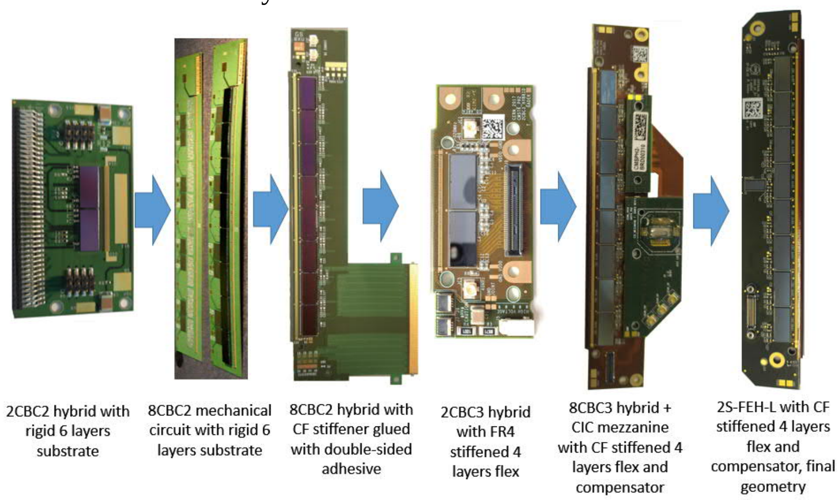


Figure 3: The evolution of 2S-FEH prototypes.

A CF reinforced flexible circuit was designed, in order to match the sensor wire-bonding level and provide a stronger substrate that can withstand the forces during wirebonding while providing excellent thermal conductivity. In this case, a flexible adhesive was applied in order to relax the stress caused by the CTE mismatch between the flex circuit and CF stiffener. A few pieces were successfully produced of this circuit called 8CBC2 [3].

In the next iterations, the problems explained in Section 3.1 appeared and as a safe choice an FR4 stiffened 2CBC3 circuit was produced [4] in order to test the new front-end ASICs (CBC3.0). The final build-up was already used with the 8CBC3 circuits, where a compensator was applied to keep the circuit build-up symmetric [4]. The Concentrator Integrated Circuit (CIC) is the data aggregator ASIC connected to all the FE ASICs. It was not yet available at the time of circuit production. Due to this, a pluggable mezzanine was foreseen for the circuit during the design phase in order to give access to all the CIC data lines for the test system and to enable the on-board ASIC tests without the production of a new prototype circuit. The final 2S-FEH prototype design was derived from the 8CBC3 design with the integration of the CIC and a new placement of the data connector that enabled a more flexible connection to the 2S-SEH.

2.2. Evolution of the PS-FEH

The PS-FEH development started much later compared to the 2S hybrid line. This was due to the late availability of the front-end readout chips, the Short Strip ASIC (SSA) and MPA ASICs that were required for the development. In order to try the different circuit construction (full size fold-over with CIC ASIC) a mock-up circuit (PS-MCK) was designed with various test features, but with the CBC2 ASICs [5],[6]. These test features allowed to collect useful information for the manufacturing of the next PS-FEH prototype. The PS-FEH prototype was designed using the experience from the 2S-FEH and PS-MCK prototypes (Figure 4). Thanks to these, the prototype needed only minor changes in the final design for the pre-production of the hybrids.

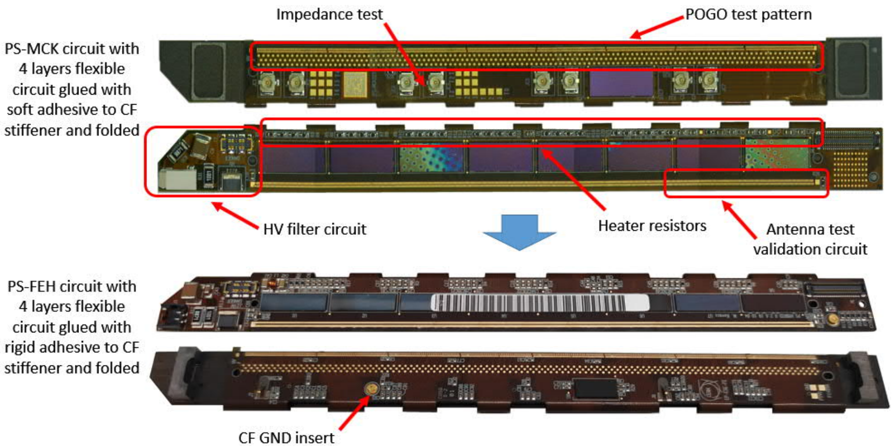


Figure 4: The evolution of the PS-FEH prototypes.

3. Issues discovered during prototype production and the developed solutions

During the numerous hybrid prototype productions, various issues were discovered. Some of them were very serious, risking the feasibility of the hybrid assemblies, some of them were less important. In the following sub-sections, many of these issues and their solutions are detailed.

3.1. CF stiffener delamination and circuit bow

The first hybrid prototypes explained in Page 3 were using a rigid substrate. Due to the reasons explained in Subsection 2.1 the substrate was changed to a CF reinforced four layers flexible construction. The first circuits were laminated with a double-sided adhesive that remained flexible after application. The intention of this was to compensate the effects of the CTE mismatch between the CF and the flexible PCB. Unfortunately, due to the softening of the adhesive at reflow temperature (230 °C-240 °C) the circuit delaminated and waves were formed (Figure 5). These compromised the flip-chip assembly with catastrophic consequences.

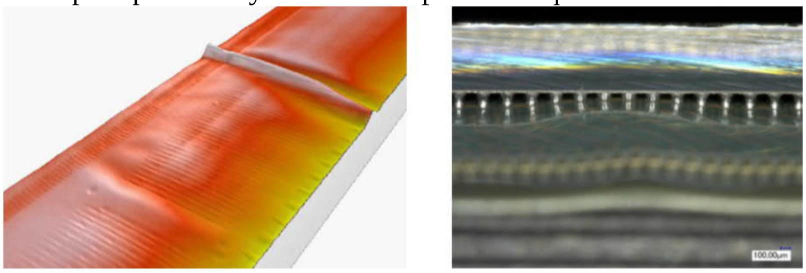


Figure 5 Waves formed during the reflow of a circuit laminated with a double-sided transfer tape.

In order to mitigate this problem, the usage of hard adhesives was explored. One initiative was to use the Dupont Pyralux adhesive family, which is widely used for the lamination of multilayer flexible circuits. The first trials showed excessive bow due to the asymmetric construction. A compensator was introduced to keep the build-up symmetric and therefore flat (Figure 6).

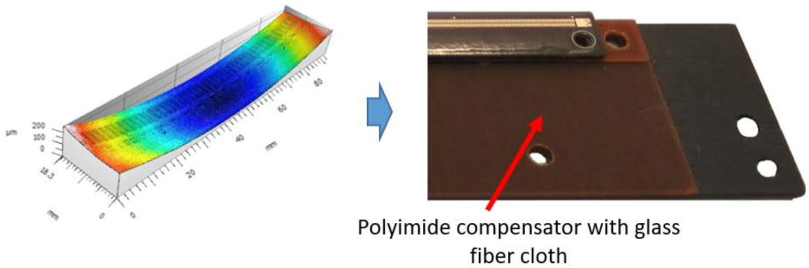


Figure 6 Bow caused by the asymmetric build-up (left) and a circuit laminated with compensator (right).

With the new lamination procedure, the circuits remained flat and the waves did not appear anymore, but a new delamination effect was observed. This effect turned out to be caused by the "popcorn effect" due to the excessive water absorption of the cyanate-ester resin system of the CF stiffeners. If circuits are exposed to the ambient for more than 3 hours, the water absorption might be already critical and delamination might occur during the reflow soldering (Figure 7).

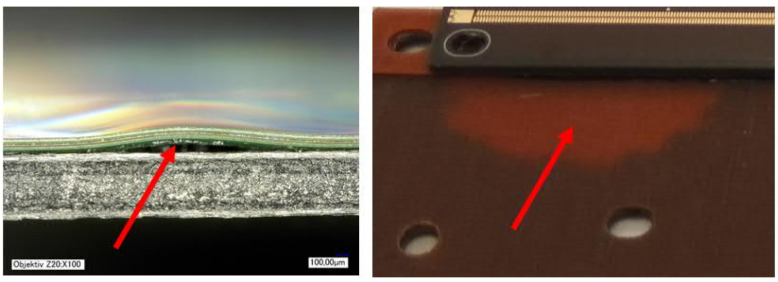


Figure 7: Delamination caused by the "popcorn effect" due to water absorption.

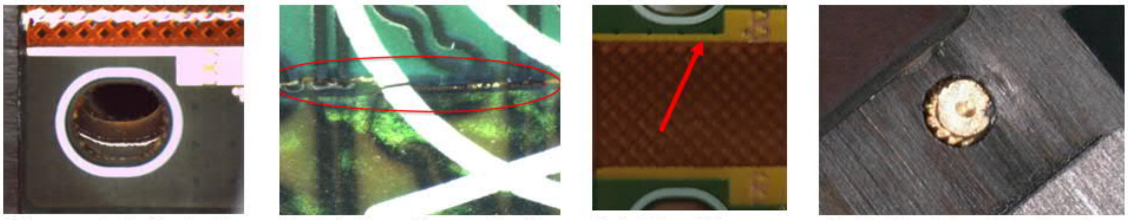
The solution to this problem is the application of a strict drying procedure and the limitation of processing time before reflow soldering.

3.2. Blockage of alignment holes, soldermask cracking and CF stiffener grounding

During the hybrid production, several alignment holes are used to laminate the circuit itself, the CF stiffener and to prepare the fold-over. After these processes, the same holes are used for the alignment during the module construction and hybrid testing. In order to avoid the blockage of these tooling holes, in the 2S-FEH and PS-FEH pre-production designs additional tooling holes were added and will be reserved exclusively for the CF lamination step.

Soldermask cracking in the fold-over region of the hybrids was observed when a tight fold radius was applied. As a solution, coverlay was applied instead of soldermask (only in the fold-over region, due to the limited accuracy of the coverlay) with a transition zone where the coverlay and soldermask was overlaying. This overlaying zone was also prone to cracking, therefore a plated (uncovered) transition zone was created. No problems were observed with this solution.

In order to eliminate the noise caused by the electrically conductive CF stiffeners, a gold plated aluminium insert is pressed into them to provide connection to the circuit ground (GND). All issues and solutions discussed in this section are illustrated in Figure 8.



Alignment hole blocked by misaligned internal layers or adhesive leakage | Crack in the soldermask in the transition zone between soldermask and coverlay | Plated transition zone between coverlay and soldermask next to the bend-zone | Gold plated aluminium inserts are press fitted into the CF stiffeners and connect them to the hybrid's GND

Figure 8 Blocked alignment holes, soldermask cracking, plated transition zone and a GND insert.

4. Summary

There were many prototyping steps leading to the final prototype designs of the 2S and PS FEHs. Solutions for all the identified problems were developed and implemented in the latest hybrid designs that are ready for the pre-production starting in 2022. The implemented improvements are expected to increase the manufacturing yield and the reliability of the hybrids.

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