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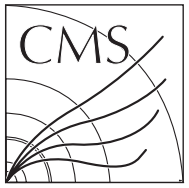

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CIC2 a radiation tolerant 65nm data aggregation ASIC for the future CMS tracking detector at LHC

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Abstract

The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-II CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). This data aggregator, designed in 65nm CMOS technology, will be a key element of the tracker front-end chain. A first prototype, CIC1, was tested successfully in early 2019 and was followed by the development of a final radiation tolerant version of the chip: the CIC2. CIC2 design, implementation, and complete test results, are presented.

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CIC2: a radiation tolerant 65nm data aggregation ASIC for the future CMS tracker

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Abstract: The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-II CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). This data aggregator, designed in 65nm CMOS technology, will be a key element of the tracker front-end chain. A first prototype, CIC1, was tested successfully in early 2019 and was followed by the development of a final radiation tolerant version of the chip: the CIC2. CIC2 design, implementation, and complete test results, are presented.

Keywords: ASIC, LHC Upgrade, Tracker, 65 nm CMOS technology

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Contents

1 Introduction **1**

2 CIC2 specifications **1**

3 CIC2 characterization results **2**

3.1 Data processing 2

3.2 Power measurements 2

3.3 Thermal scan 3

3.4 Radiation hardness assessment 3

4 Next steps **5**

1 Introduction

The Concentrator Integrated Circuit (CIC) ASIC is a front-end (FE) chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-2 CMS Outer Tracker (OT) upgrade at the High-Luminosity LHC (HL-LHC) [1]. This 65nm CMOS radiation tolerant data aggregator is a fundamental element in the future detector FE chain.

The main new OT feature will be its inclusion in the first level of the CMS trigger system. This requires 40MHz capability for the detector. To this end, a very innovative detection element, the p_T-module, has been developed. The main principle, two silicon sensors placed a few mm apart, is already in use in current tracking systems. The readout electronics, on the other hand, is fundamentally different from existing system. Indeed, in order to reach the data reduction levels necessary for the track trigger, the signals from the 2 sensor layers will be put in coincidence directly at the module level. This coincidence will be performed by a set of 3 front-end ASICs types: CBC [2] and SSA/MPA [3] for 2S and PS modules respectively. Each p_T-module will contain 16 such ASICs.

The CIC [4] handles the data produced by those chips and performs another data compression stage, and data truncation if necessary. It must be compatible with both module flavors (different hybrids, voltages, input streams) and is therefore highly configurable.

In order to validate the chip model, a first physical version, the CIC1, was developed and implemented, along with a complete standalone testbench. This chip, which incorporates all the data processing functionalities of the final system along with the same footprint, was successfully tested in 2019 [5]. These results paved the way for a fast second iteration in 2020 of the CIC2.

This document summarizes the characterization tests performed in 2020 on this chip, which could be considered as a pre-production version. The CIC2 specifications are summarized in section 2. Section 3 presents the results of the characterization campaign. Finally, the next stages of the project are introduced in section 4.

2 CIC2 specifications

The main features of the CIC2 were already presented in [4, 5]. The chip aggregates the data coming from 48 input lines at the rate of 320 MHz. The whole chip architecture is divided into two independent paths: the trigger path and the L1 path. The trigger data represents 80% of the overall input bandwidth. The rest is reserved for the data extracted upon the reception of an L1 accept signal by the detector.

In order to be correctly deserialized, the input data must be phase aligned w.r.t. the CIC 320MHz clock. This is the role of the PHYport block, which is a simplified version of the lpGBT ePort module. Further alignment steps are required for the trigger data to be correctly retrieved, see Ref. [4] for more details.

The CIC2 architecture (PHYport, L1 path and data path) is completed by two other blocks: system manager and slow control. The slow control block handles the communication of the different configuration parameters via the I^2C protocol. The system manager decodes the fast control information and generates the different signals relevant to the chip such as clocks and reset.

Output is sent over 7 lines, either clocked at 320 or 640 MHz depending on the required configuration. As for the input, most of the bandwidth, 6 out of 7 lines, is used by the trigger path. Output data format is standardized in order to simplify the subsequent processing by the data acquisition. Along with the data compression, this is one of the main goal of the CIC ASIC.

The CIC2 was the first version of the chip designed to meet all the requirements of the final system. Compared to the CIC1, the CIC2 includes triplicated logic, 640MHz output capability, and a significant power optimization of the L1 path.

3 CIC2 characterization results

3.1 Data processing

The CIC2 chip tests started in December 2019 using the same experimental test-bench as the CIC1 (both chips have the same footprint). The different stages of chip configuration and data processing were tested successfully. A few minor bugs related to the RTL model, not affecting the overall chip performance, were observed. The only potentially problematic feature was a data corruption problem observed in some output lines under very particular conditions (very high occupancy and low core voltage). The origin of this issue was understood and addressed in the production version, but it does not affect the CIC2 when running at nominal voltage under HL-LHC occupancies.

3.2 Power measurements

Great care was paid to power budget optimization during the CIC2 design development. Figure 1 shows a comparison of the CIC2 and CIC1 power usage. As explained earlier, the L1 path architecture has been substantially revisited between the two versions. A significant reduction is observed for all the configurations in each of the working modes, in particular in the data sending phase which will be the default running mode for the CIC. In this mode, it is actually interesting to see that the values measured are well below the requirements, which are 250 and 315 mW for PS and 2S modules respectively.

Mode	Core Voltage	Periphery Voltage	Max power budget (in mW)	Version	Measured power (in mw)	
					Phase alignment	Data sending
PS320	1.0V	1.2V	250	CIC1	241	206
				CIC2	218	167
PS640	1.0V	1.2V	250	CIC1	N/A	N/A
				CIC2	225	173
2S	1.2V	1.2V	315	CIC1	339	281
				CIC2	306	196

Figure 1. Comparison of CIC1 and CIC2 power consumption.

3.3 Thermal scan

The OT will be cooled at −30°C. One expects the temperature on the FE hybrids to be around −10°C, and a little higher on the chips. Standard test routines were run with the chip under constrained temperature environment. For a chip temperature between −30°C and +45°C, no errors were observed.

3.4 Radiation hardness assessment

Radiation hardness is a major feature of the CIC2. Two crucial elements were verified with the chip: the effect of radiation on its aging (Total Integrated Dose (TID)), and the impact of high energy ionizing particles on its operation (Single Event Effects (SEE)). CIC SEE and TID measurements were done with an adapted version of the CIC standalone test-bench. SEE tests were performed on the Louvain HIF beamline [6] and TID runs at CERN X-ray facility [7].

Aging effects (TID)

The total dose expected in the tracker during the HL-LHC campaign, corresponding to an integrated luminosity of 3000 fb^{-1}, will be 60Mrad for a PS module and 10Mrad for a 2S module. Impact of large radiation dose on TSMC 65nm technology was studied in detail in Ref. [8]. The main effects observed are increase of the leakage current and of the chip latency.

For each component irradiated with γ-rays a series of measurement points was recorded for total dose step ranging between 0 and 200Mrad. Average γ-ray flux was 7.6 Mrad/h. Temperature was not regulated. The output delay variations presented below are measured in 320MHz clock cycle unit (3 ns). For example, a 20% variation corresponds to $\approx$ 0.6 ns. The results, for two different core voltage configurations, are presented in Figures 2 and 3. The variation is measured for the 7 output lines of the CIC.

Expected behavior (increased latency) is observed in both cases up to 150Mrad. At low core voltage, some lines were lost for larger values, but recovered after irradiation (show by the two last entries on each figure.). High temperature impact is suspected.

Single event effects

Based on the measurements performed on the Louvain heavy ions beamline, CIC single event upset probabilities were computed following the method described in Ref. [9]. In order to extract upset rate, the PS and 2S modules regions where the hadrons fluxes were maximum have been selected. Those regions actually also corresponds to the maximum occupancy for both 2S and PS

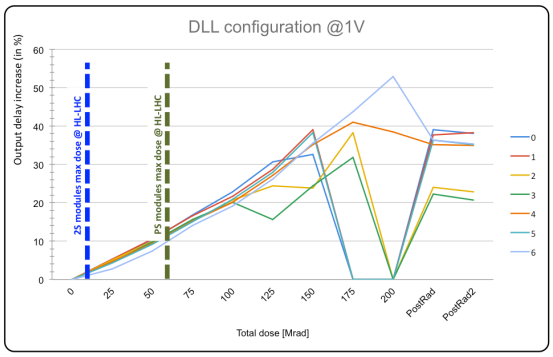

Figure 2. CIC output delay variation w.r.t. the total dose ($V_{\text{core}} = 1V$). The two last entries were measured after irradiation.

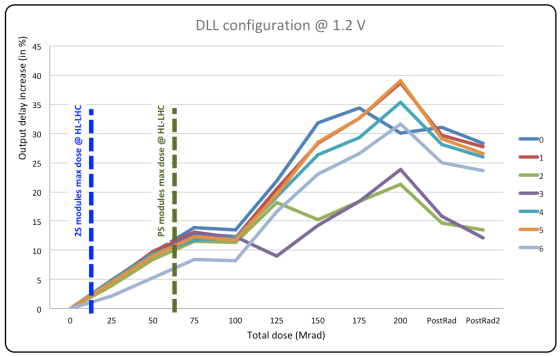

Figure 3. CIC output delay variation w.r.t. the total dose ($V_{\text{core}} = 1.2V$). The two last entries were measured after irradiation.

module types. Therefore the rates presented here should be considered as upper limits, as they were obtained for the maximum occupancy and radiation fluxes. Rates were computed for both L1 and trigger paths separately. The results obtained for the L1 path are summarized in Table 1.

Table 1. Upset rate probabilities due to SEE errors in the L1 path, per CIC and for the whole tracker.

Working mode	CBC 320M 750kHz	MPA 320M 500kHz	MPA 640M 750kHz *(est.)*
Expected upset rate per CIC (in s^{-1})	$1.1^{+3.3}_{-0.7} \cdot 10^{-4}$	$1.8^{+0.7}_{-0.6} \cdot 10^{-3}$	$2.5^{+1.0}_{-0.8} \cdot 10^{-3}$
Expected upset rate for the tracker (in s^{-1})	$1.6^{+5.0}_{-1.2}$	$20.2^{+7.8}_{-6.8}$	$28.3^{+10.9}_{-9.5}$

Values are provided per CIC, but also for the full tracker, assuming that there will be 5592 PS modules, and 7608 2S modules, with 2 CICs per module. Due to technical constraints, the rates for the PS modules were obtained only for L1A rate of 500kHz. A 40% increase would give a reasonable estimation at 750kHz. Measurements were done at 320MHz only, but 640MHz clock affecting only the output buffers, extrapolation from 320 to 640 is relatively simple.

Regarding the trigger path, upset rate probabilities are summarized in Table 2. For the MPA 640MHz mode (full occupancy) estimation, as most of the SEE were observed in the output region, we applied a factor 2 w.r.t. the 320MHz case.

Table 2. Upset rate probabilities due to soft errors in the TRG path, per CIC and for the whole tracker.

Working mode	CBC 320M	MPA 320M	MPA 640M *(est.)*
Expected upset rate per CIC (in s^{-1})	$2.0^{+1.6}_{-0.4} \cdot 10^{-4}$	$1.2^{+1.6}_{-0.5} \cdot 10^{-3}$	$2.4^{+3.2}_{-1.0} \cdot 10^{-3}$
Expected upset rate for the tracker (in s^{-1})	$3.0^{+2.5}_{-0.6}$	$13.3^{+17.8}_{-5.6}$	$26.7^{+35.6}_{-11.2}$

Values are comparable to the one observed in the L1 path. Considering that trigger represents 85% of the total CIC output bandwidth, one can even conclude that the relative impact of SEE on

the trigger path will be even smaller than in the L1 path.

Overall, SEE rates observed on both paths are compatible with expectations and will not hamper CIC behavior under HL-LHC conditions. It should also be pointed out that no errors were observed on the CIC control paths and I^2C sectors, thus confirming the good CIC performance relative to SEEs.

4 Next steps

A final CIC version was developed in 2021 in order to address remaining CIC2 features: minor bug fixes, better repartition of the output registers in order to avoid potential voltage drop issues at low core voltage.

The CIC2.1 is an improved version of the CIC2, but both chips will fulfill CMS OT requirements. Both chips will therefore be produced during the final run. The CIC2.1 as the default item, the CIC2 as a backup solution.

Acknowledgments

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