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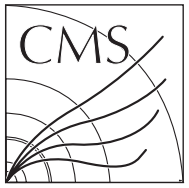

The Compact Muon Solenoid Experiment

Conference Report

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Serial powering and signal integrity characterization for the TEPX detector for the Phase-2 CMS Inner Tracker

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Abstract

The entire CMS silicon pixel detector will be replaced to operate at the High-Luminosity LHC. In this contribution, the new Tracker Endcap Pixel detector will be presented, focusing on a novel concept to provide both power and data connectivity to the modules through a disk-shaped PCB. As this part of the detector also features the longest serial powering chains in the CMS Phase-2 Inner Tracker, emphasis is put on serial powering results and the characterization of the signal integrity.

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Serial powering and signal integrity characterization for the TEPX detector for the Phase-2 CMS Inner Tracker

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Abstract: The entire CMS silicon pixel detector will be replaced to operate at the High-Luminosity LHC. In this contribution, the new Tracker Endcap Pixel detector will be presented, focusing on a novel concept to provide both power and data connectivity to the modules through a disk-shaped PCB. As this part of the detector also features the longest serial powering chains in the CMS Phase-2 Inner Tracker, emphasis is put on serial powering results and the characterization of the signal integrity.

Keywords: Particle tracking detectors (Solid-state detectors), Radiation-hard detectors

[1]Speaker

Contents

1 Introduction

The CERN LHC [1, 2] is the world's most powerful and luminous particle collider to date. After the end of the Run 3 data taking, the LHC will be upgraded to deliver instantaneous luminosities of up to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, exceeding the initial design value by a factor of 7.5 [3]. The entire CMS detector will undergo substantial upgrades in order to fully exploit the physics potential of the collisions delivered while resisting the increased level of radiation.

The new pixel tracking system [4] will extend the coverage up to pseudorapidities of $|\eta| = 4.0$. The layout and a schematic view are shown in Figure 1. Due to its proximity to the interaction point, enhanced radiation tolerance of the silicon sensor and readout chip are required. A reduced material budget and a pixel size of 100×25 or $50 \times 50\,\mu\mathrm{m}^2$ will be instrumental in ensuring stable tracking performance while maintaining a low occupancy despite the increased particle flux. The new Inner Tracker is subdivided into the Tracker Barrel Pixel (TBPX), Tracker Forward Pixel (TFPX), and Tracker Endcap Pixel (TEPX) systems, which are visible in Figure 1. The TEPX detector is presented in the following section, with particular emphasis on the characterization of the serial powering scheme and the electrical signal integrity of the TEPX readout chain.

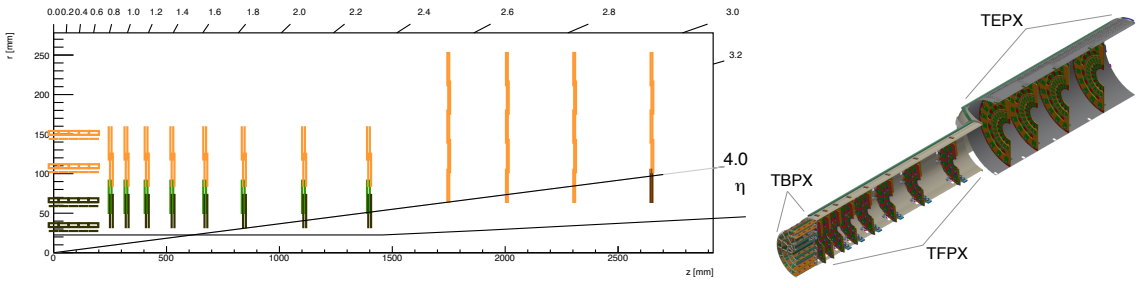

Figure 1. Layout (left, updated from Ref. [4]) and schematic view [4] (right) of a quarter of the upgraded CMS Inner Tracker. The z-axis is aligned with the beam direction.

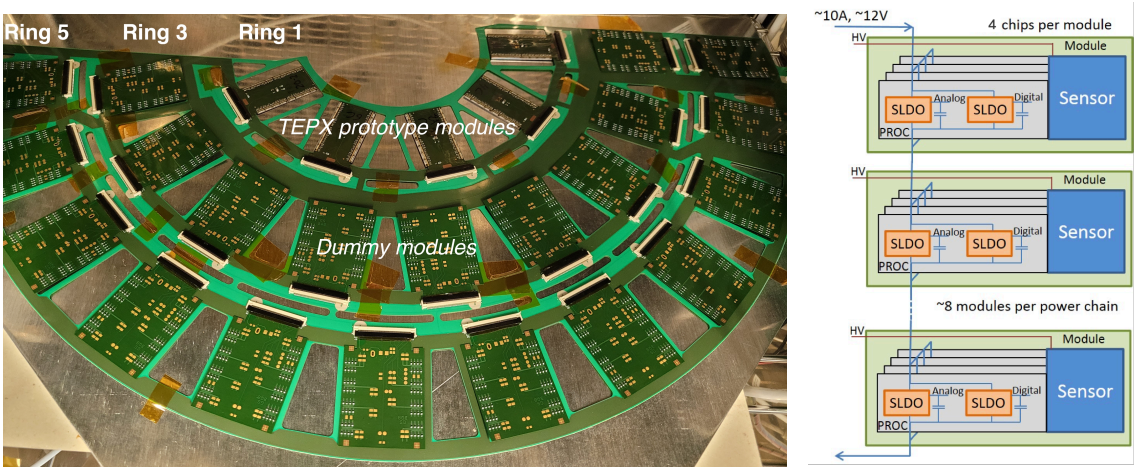

Figure 2. Left: TEPX half-disk prototype equipped with TEPX prototype modules in ring 1 and dummy modules in rings 3 and 5. Right: Schematic of the serial powering chain used in the TEPX system [4].

2 The Tracker Endcap Pixel Detector

The TEPX detector will consist of four double-disks in each of the CMS endcaps. In each disk, the TEPX modules will be arranged in five concentric rings, where the front face (towards the interaction point) of each disk will contain the odd-numbered rings and the back face will contain the even-numbered ones. Each disk is complemented by a second disk, thus forming a double-disk, in order to achieve hermetic coverage. Power and data connectivity will be provided to the modules through a five-layer Polyimide PCB of 400 μm thickness with meshed input and return current layers. In Figure 2 (left), the prototype of a TEPX half-disk with three rings is shown. The innermost ring 1 (R1) will hold five modules, the intermediate ring 3 nine, and the outermost ring 5 twelve TEPX modules. Modules in ring 1 are read out via three data lines per module because of the high expected data rate, while the modules in rings 3 and 5 are read out with a single line per module.

The TEPX modules will feature silicon sensors with a pixel size of 100×25 or $50 \times 50\,\mu\text{m}^2$, which are bump-bonded to four readout chips (ROCs or PROCs) per module. In the prototype modules studied here, the RD53A [5] ROC is used. The ROCs are wire-bonded to an HDI with a data readout, bias voltage, and power connection, where the latter is regulated by two shunt-low-dropout (SLDO) regulators for each ROC, one for the analog and one for the digital supply line. In the TEPX disk, all modules in a given ring are powered in series (serial powering, SP), while the current is shared between the four ROCs in a module. Conversely, the bias voltage (HV) is provided in parallel to all modules in the same ring. This powering scheme is illustrated in Figure 2 (right).

The data lines of the TEPX disk prototype are connected to two mezzanine cards on an FC7 [6] readout board via flat flex and DisplayPort (DP) cables. Due to the half-disk prototype design, a maximum of three ROCs per module can be read from ring 1, one per data line. In the final TEPX detector, all four ROCs of each module will be read out. In standalone operation, a single TEPX prototype module is plugged into a flex-to-DP adapter, which is directly connected to the mezzanine card through a DP cable. All four ROCs of the module are read out simultaneously in this case.

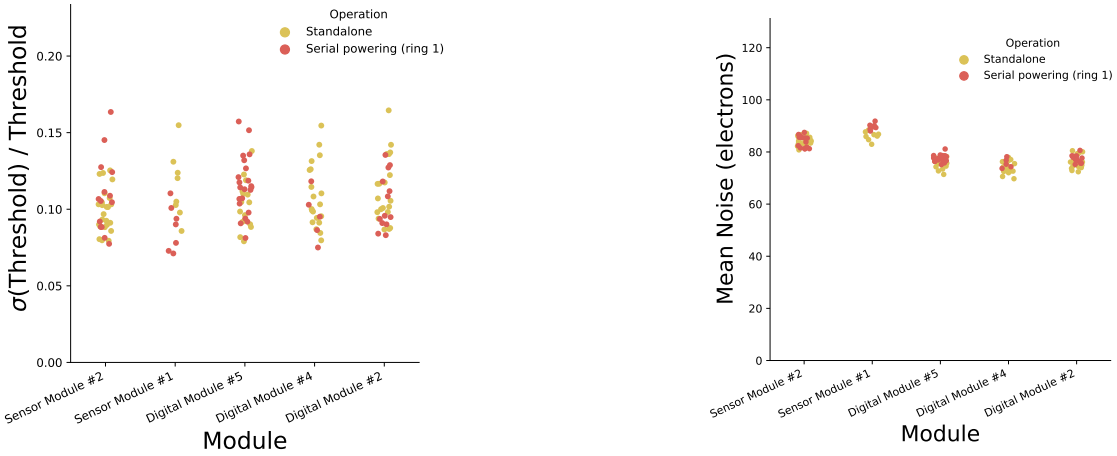

Figure 3. Comparisons of the relative width of the threshold distribution (left) and the mean noise (right) between standalone (yellow) and serial powering operation (red) for different TEPX prototype modules (x-axis). Each point corresponds to a single measurement with a single ROC.

2.1 Serial Powering Characterization

In order to characterize the performance and reliablity of five TEPX modules powered in series in R1 of the TEPX half-disk prototype, the pixel thresholds are tuned and compared to results obtained in standalone operation of single modules. In both cases, the modules are operated with an input current of 6.8 A at an ambient temperature of −50°C inside a climatic chamber. The analogue and digital voltages of each ROC are tuned to 1.20 and 1.25 V, respectively. Prototype modules with and without a silicon sensor are used, which are referred to as sensor modules and digital modules, respectively. A bias voltage of −50 V is applied to deplete the sensor of the former.

In the procedure applied to tune the tresholds, initially unresponsive pixels of a given ROC are masked. After equalizing the channels of that ROC, noisy pixels are masked. The global threshold is adjusted to a target of 1500 e before the channels are re-equalized. Finally, newly noisy pixels are masked and the efficiency as a function of the injected charge is measured for each pixel of a given ROC, from which the threshold and noise of each pixel is extracted.

In Figure 3, the relative width of the threshold distribution (left) and the mean noise (right) are compared for different modules and ROCs between standalone (yellow) and SP (red) operation. Both modes of operation yield very similar results with no systematic differences observed. It was verified that the number of masked noisy pixels as a function of the target threshold is consistent between SP and standalone operation and no additional noise is introduced by the SP chain.

The resilience of the SP chain against potential failures is tested in two scenarios. First, the middle one of the five fully operative modules in R1 is replaced by one that has only three out of four ROCs wire-bonded to the HDI. Consequently, the input current is shared between fewer chips, in turn causing increased chip temperatures. Second, a module with a broken silicon sensor, showing a high bias current, is inserted instead. In Figure 4, the relative width of the threshold distribution (left) and the mean noise (right) are compared between these two scenarios and standard SP operation. No deviation from the expected behavior is observed, indicating that the scenarios tested do not affect other modules in the serial powering chain.

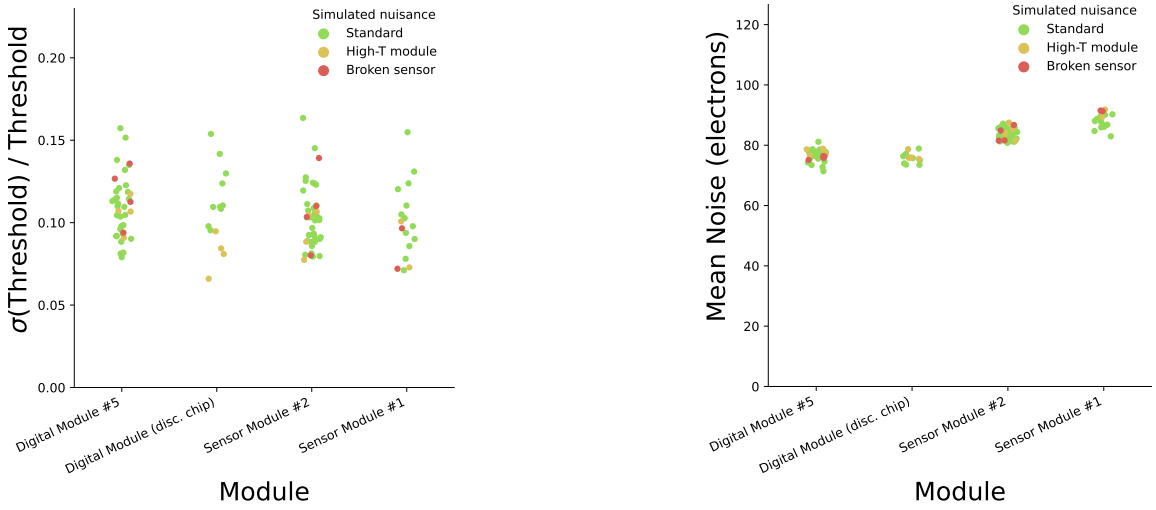

Figure 4. Comparisons of the relative width of the threshold distribution (left) and the mean noise (right) between standard operation in standalone and serial powering operation (green) and two possible failure scenarios in the serial powering mode (yellow and red) as described in the text for different TEPX prototype modules (x-axis). Each point corresponds to a single measurement with a single ROC.

2.2 Signal Integrity Characterization

The signal integrity along the electrical TEPX readout chain is tested by performing electrical bit error rate (BER) tests using the PRBS7 pattern of the RD53A ROC. In particular, results for the longest data line in the TEPX system with a length of 492 mm are reported. It corresponds to the fifth position in ring 1 (position R15) of the TEPX half-disk prototype, the leftmost position in R1 as shown in Figure 2 (left).

Here, the BER is defined as the number of 32-bit frames with at least one bit error divided by the total number N_{sent} of frames sent. The nominal data transmission rate of 1.28 Gb/s is used. In case no bit errors are recorded, a BER of $1/N_{\text{sent}}$ is reported, corresponding to a conservative upper limit on the true BER. While measuring the BER on a given chip, all other ROCs in the SP chain transmit AURORA-encoded data.

First, the BER is measured for varying signal amplitudes, which are steered using the CML_TAP0_BIAS register (TAP0) of the RD53A ROC. TAP0 can take values between 0 and 1023, with the default value being 500. In Figure 5 (left), the BER as a function of TAP0 is shown for different ROCs on different TEPX modules in position R15. Very strong improvement of the BER is found with increasing signal amplitude for all modules and ROCs tested. It is possible to consistently achieve 0 bit errors at or already below the default RD53A setting, translating to a BER below 4×10^{-12} and leaving a considerable margin for future optimization.

In order to study the effect of first- and second-order pre-emphasis on the BER, very small signal amplitudes corresponding to TAP0 = 200 are used. Only under such conditions a non-zero BER could be measured. The first- and second-order pre-emphasis is steered by the CML_TAP1_BIAS and CML_TAP2_BIAS registers of the RD53A chip (TAP1 and TAP2), respectively. In Figure 5 (right), the BER is shown as a function of TAP1 and TAP2. An improvement of the signal integrity with inverted first-order pre-emphasis of the signal is observed, while no dependence on second-

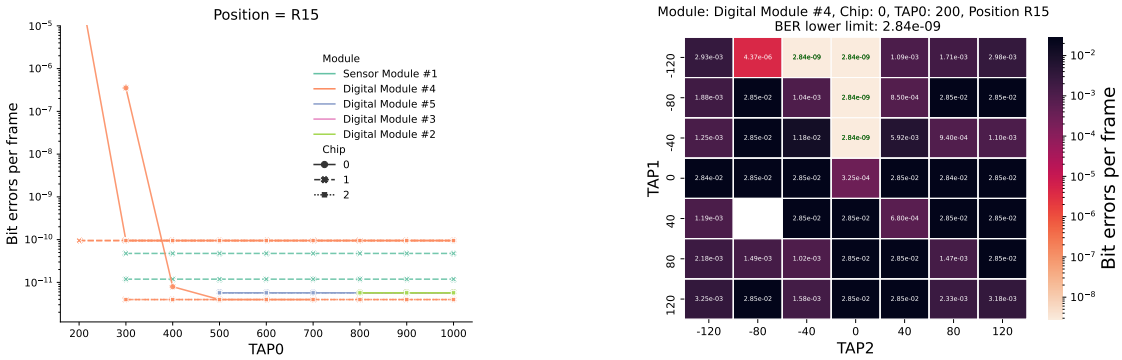

Figure 5. Bit error rate as defined in the text as a function of TAP0 (left) and TAP1 and TAP2 (right).

order pre-emphasis is found. Consequently, an optimized choice of the first-order pre-emphasis can be used to further improve the signal integrity in future operation.

Potential cross-talk between the data lines in the TEPX disk has been tested by measuring the BER for three different serializer output modes of the remaining ROCs in the SP chain. Only a small improvement with respect to the AURORA mode is observed for the PRBS7 and GND modes, and only for the smallest signal amplitude corresponding to TAP0 = 200 tested, which indicates insignificant cross-talk between data lanes in the SP chain.

3 Conclusion

The Tracker Endcap Pixel detector foreseen to be implemented during the upgrade of the CMS detector for the High-Luminosity phase of the LHC has been presented. The serial powering scheme and its influence on the pixel threshold tuning has been studied. No additional noise was found to be introduced by the serial powering chain and two potential failure scenarios were found to not affect other modules in the chain. The electrical signal integrity was studied by means of bit error rate tests, demonstrating excellent signal quality in the longest TEPX data line and leaving a promising margin for future optimization.

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