Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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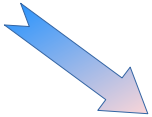
on behalf of the ATLAS Liquid Argon Calorimeter Group

TWEPP 2021 - Topical Workshop on Electronics for Particle Physics

Outline

Objectives of the ATLAS Liquid Argon Calorimeter upgrade for HL-LHC

Readout Electronics underway towards the HL-LHC



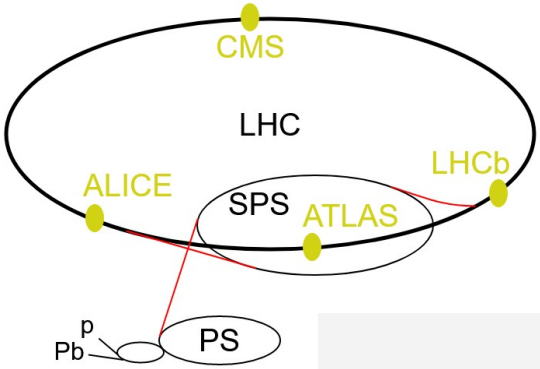
On-detector

- Pre-amplification / Shaping
- Analog to digital conversion
- Detector and control data transmission

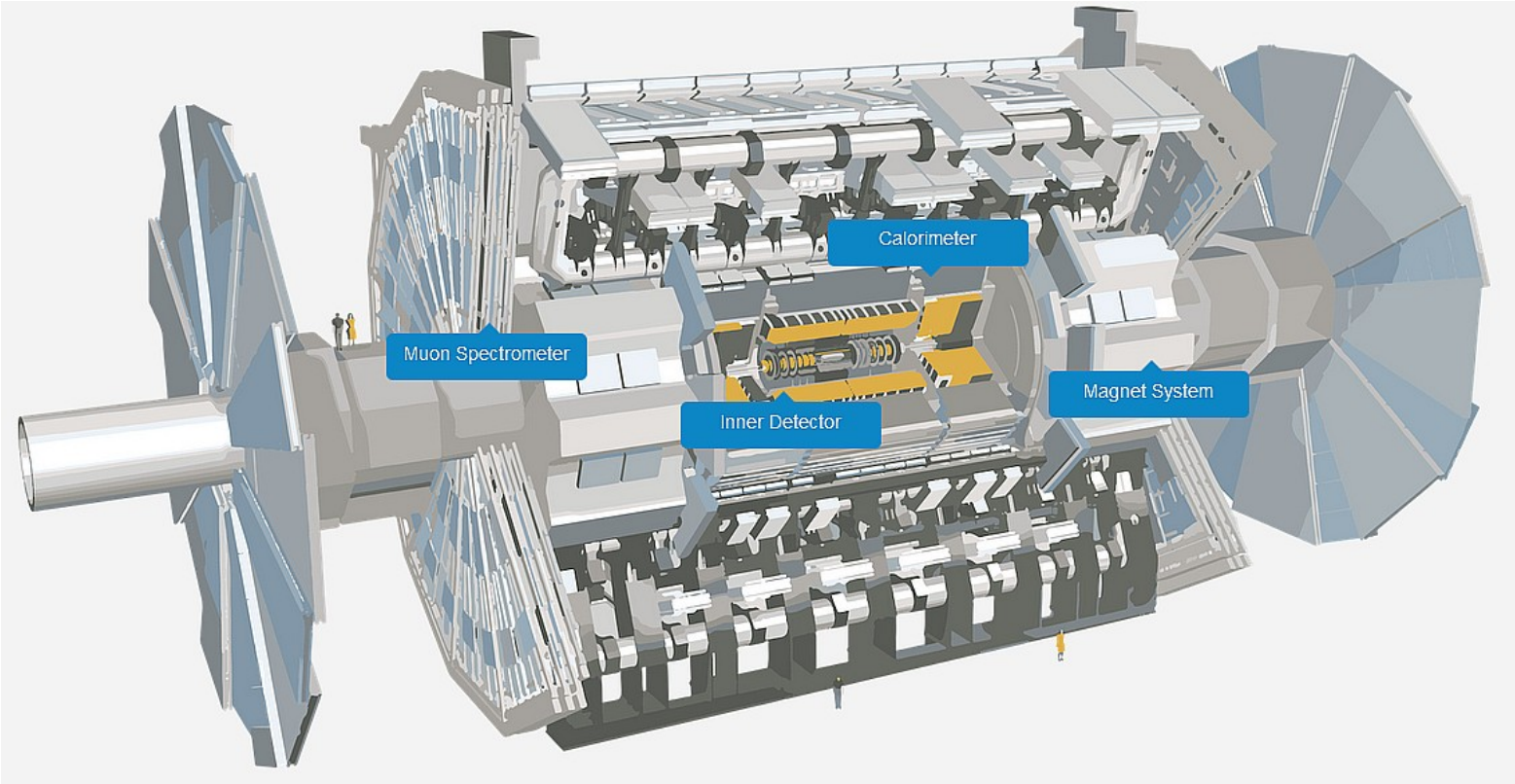
Off-detector

- Data acquisition from on-detector
- Digital processing
- Detector and control data transmission

LHC and ATLAS detector

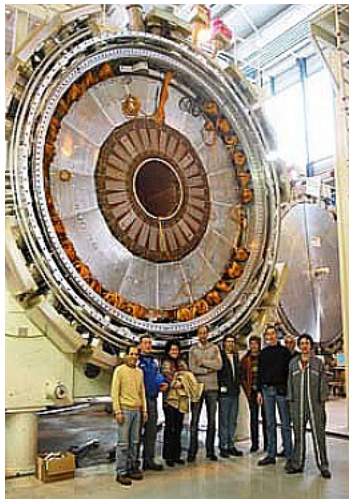


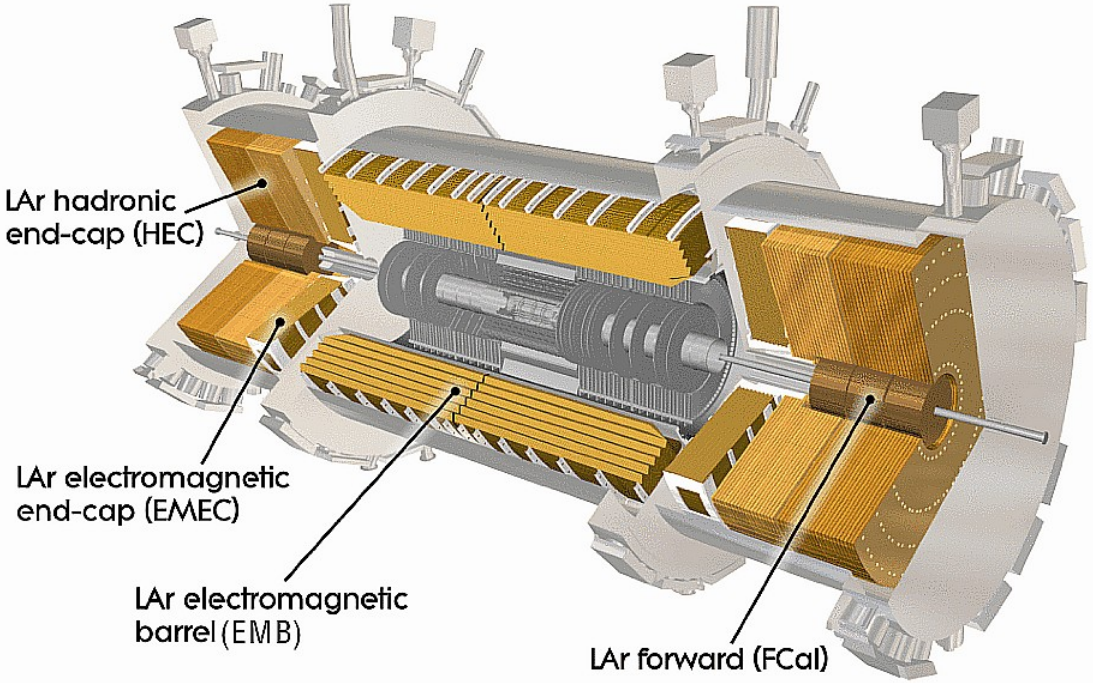
ATLAS detector

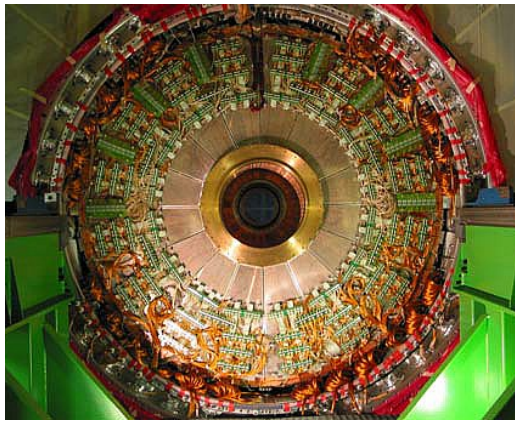


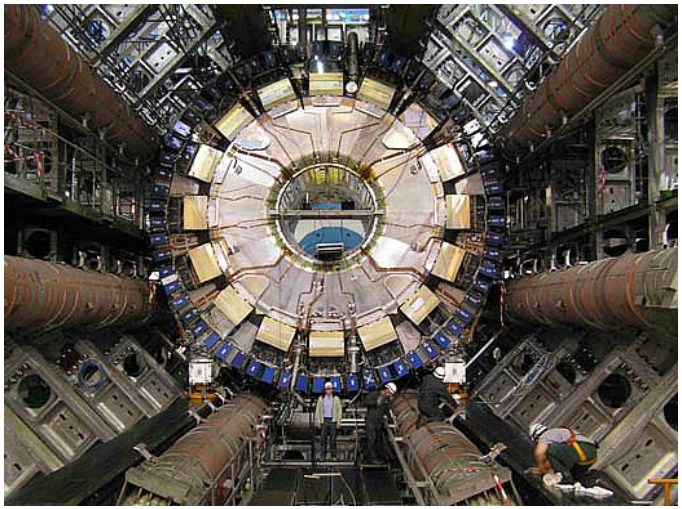
https://atlas.cern/discover/detector/

ATLAS LAr calorimeter









ATLAS LAr calorimeter readout electronics upgrades

Phase-II upgrade

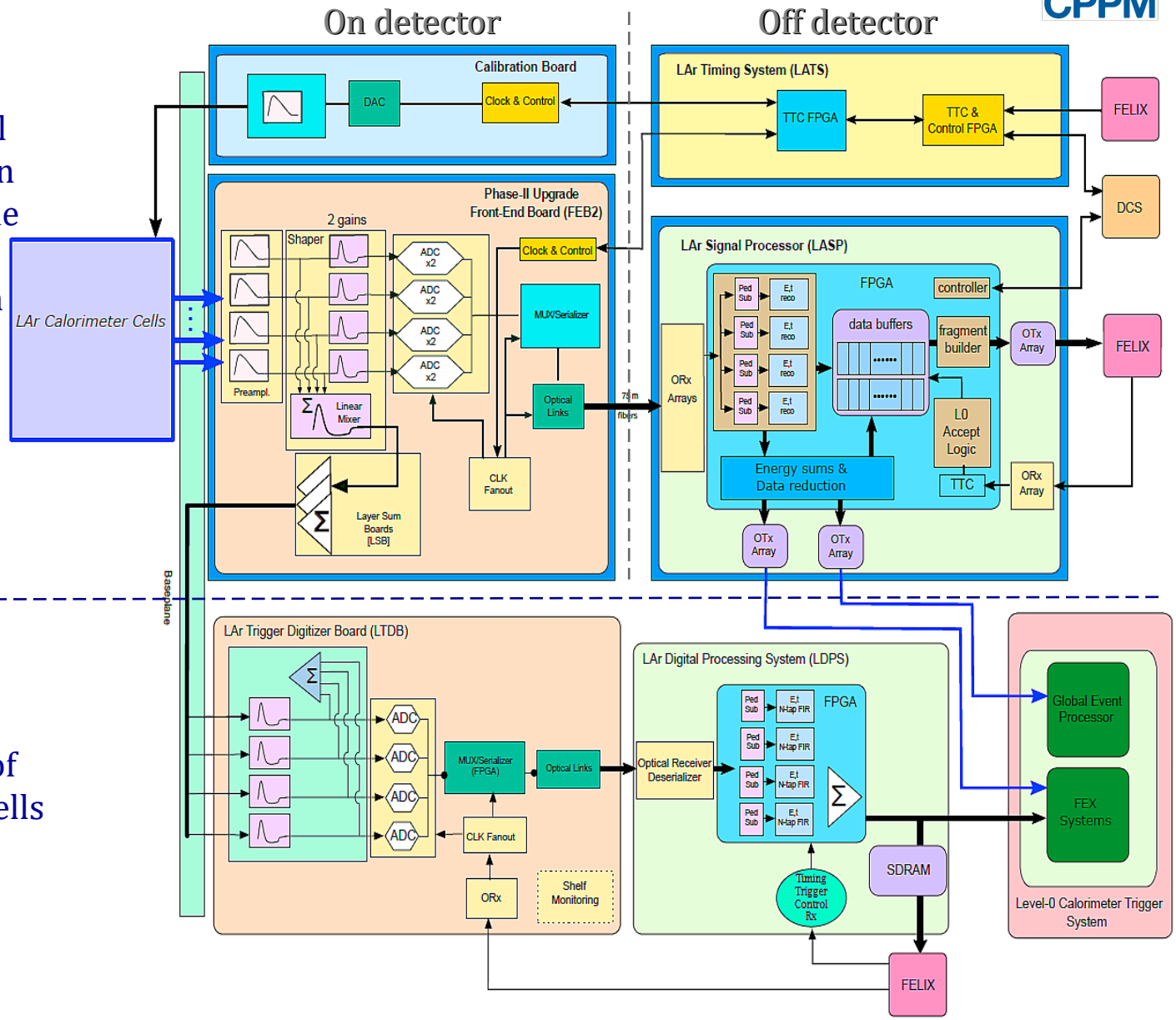
(shutdown 2025-2027)

Digitize and readout the full calorimeter (182500 cells in total) at 40 MHz and provide the information to the trigger and data acquisition systems

Phase-I upgrade

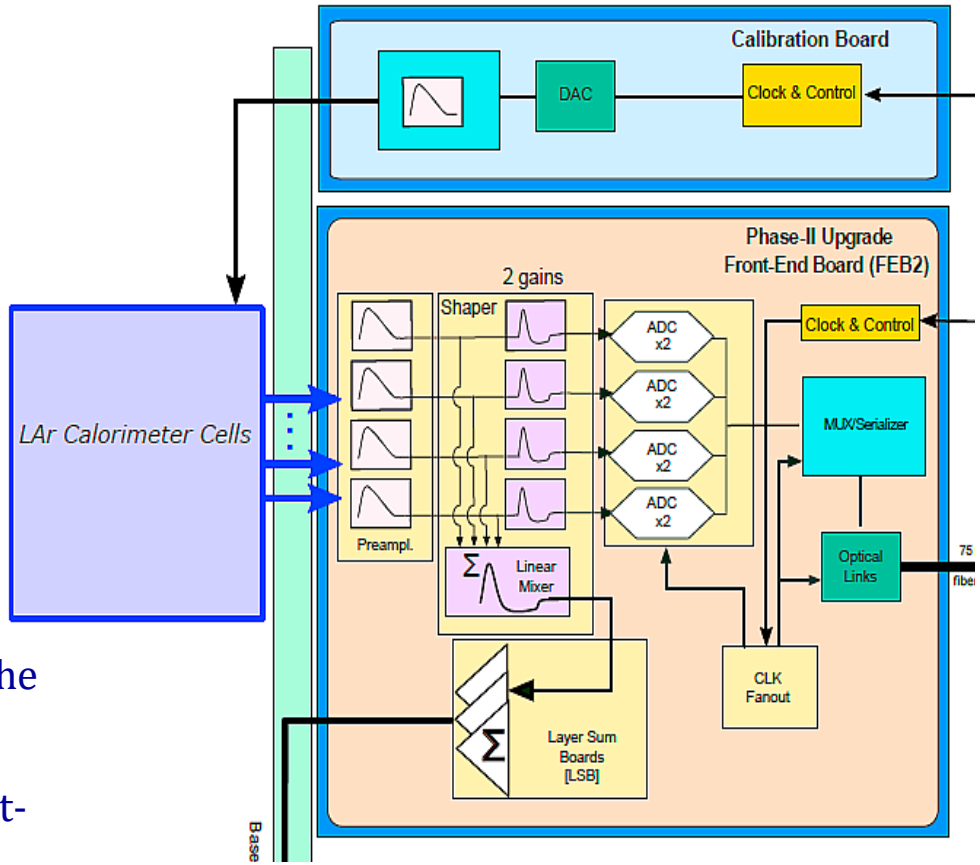
(shutdown 2019-2021)

Increase the granularity of the calorimeter trigger cells by factor ~10



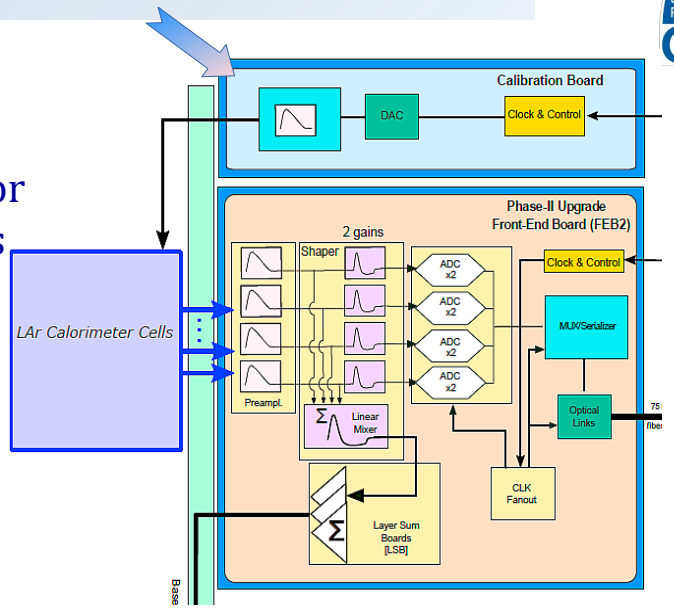
On-detector electronics specifications

- Wide dynamic range: 16 bits
- < 0.1% linearity
- Radiation tolerance:
  - TID (1.4 × kGy)
  - NIEL (4.1×10^{13} neq/cm^2)
  - SEE (10^{13} h/cm^2)
- Fully digitized readout of the entire Calorimeter at 40 MHz with two gains for the Trigger and DAQ systems:
  - 128 LAr calorimeters channels per Front-End Board (256 digitized)
  - 42 TB/s, 163.84Gb/s per board of raw data via 10Gb/s optical links



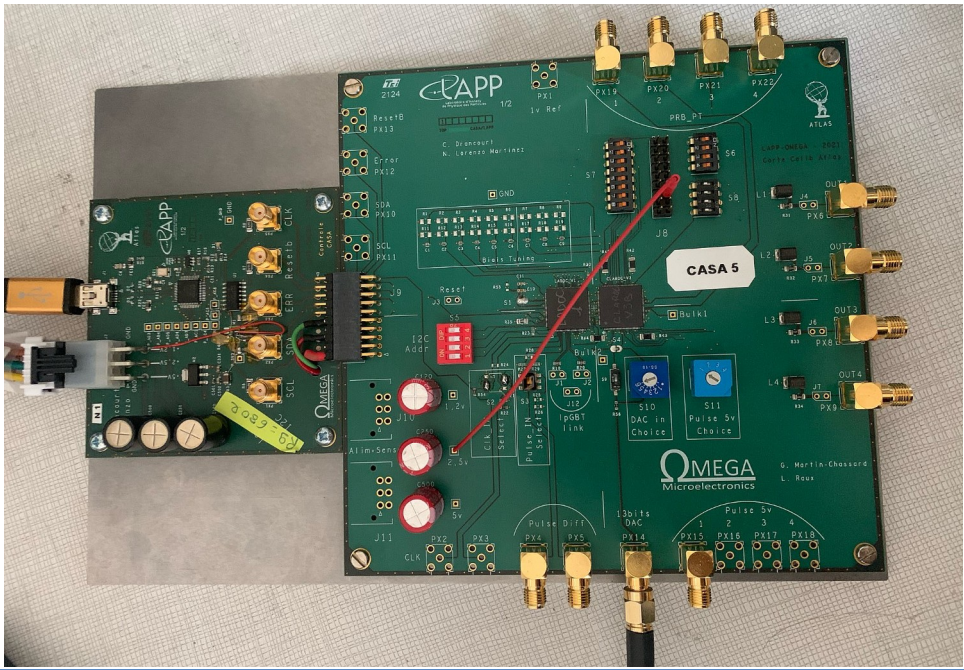
On-detector electronics: Calibration Board

- 130 boards with 128 output channels
- Provides pulses with well known amplitude and shape for the calibration and testing of the readout board channels
- 16-bit dynamic range
- < 0.1% Linearity
- Radiation hard up to 1.4 kGy
- Solution based on custom ASIC for High-Frequency Switching and Digital-to-Analog Conversion (CLAROC, LADOC)
- 4 channels/ ASIC, 32 ASICs per board

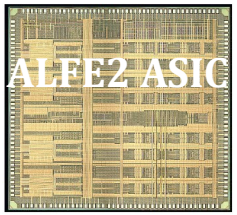


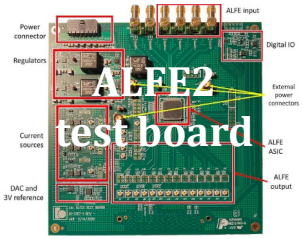
First 32-channels calibration board prototype fabricated and tested

Third ASIC prototype being tested with CASA test boards (see picture)



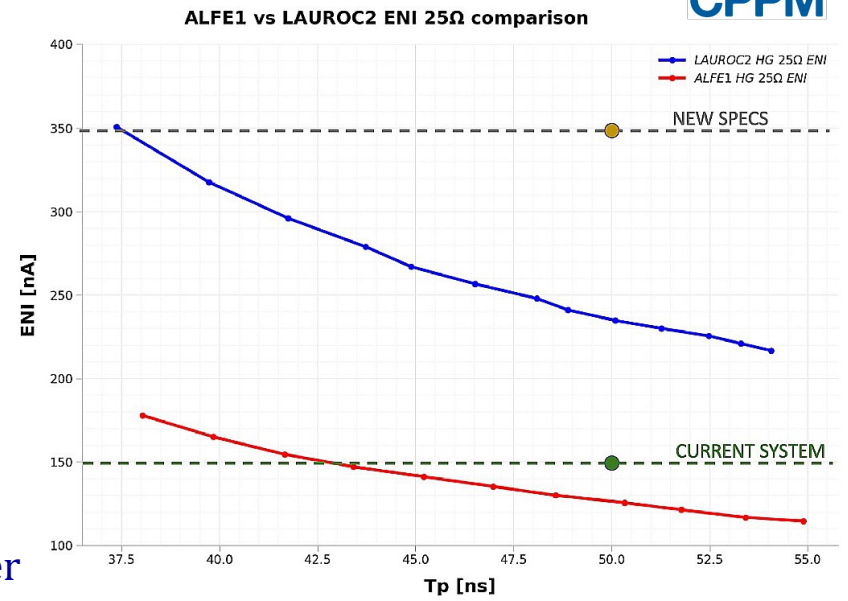
On-detector electronics: Front-End Board (FEB2)

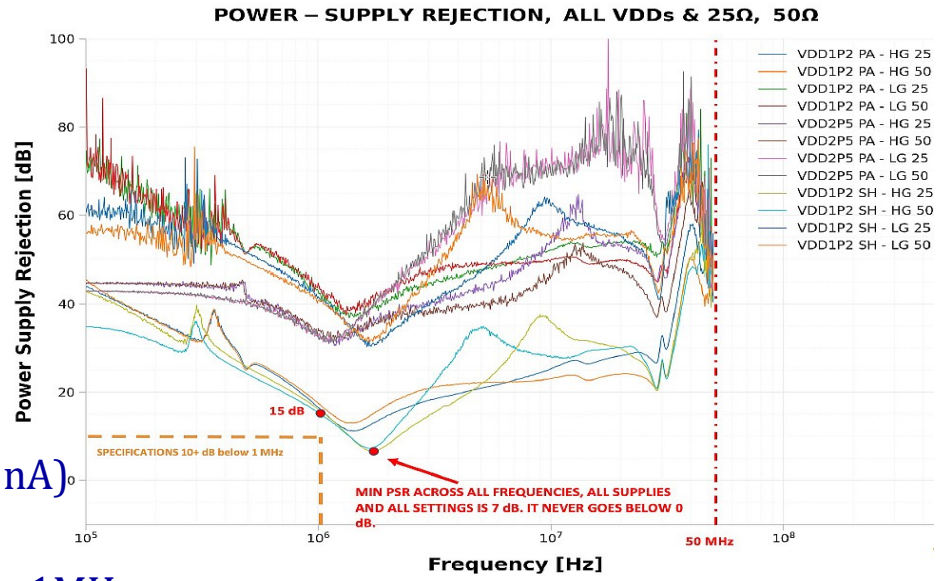




Pre-amplifying and shaping of the sensing cells

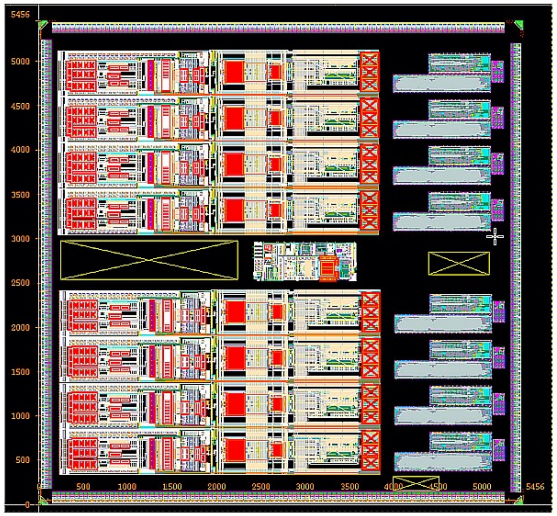
- analogue processing of the pulse signals
- amplification followed by a CR-RC^2 shaping function
- signal split into two overlapping gain scales with a gain ratio of around 23
- 4 channels input, 9 channels output (4 x LG/HG + trigger sum of 4 channels)
- dynamic range > 16-bit
- configurable design via I2C communication
- multiple prototypes developed in 130 nm CMOS:
  - ALFE (ATLAS Liquid Argon Front-End)
  - LAUROC (Liquid Argon Upgrade Readout Chip)
- INL below 0.2% on the high gain output
- equivalent noise current (ENI) below 350 nA (120 nA) for a 25 ohm (50 ohm) termination
- power-supply rejection ratio (PSRR) > +10 dB up to 1MHz





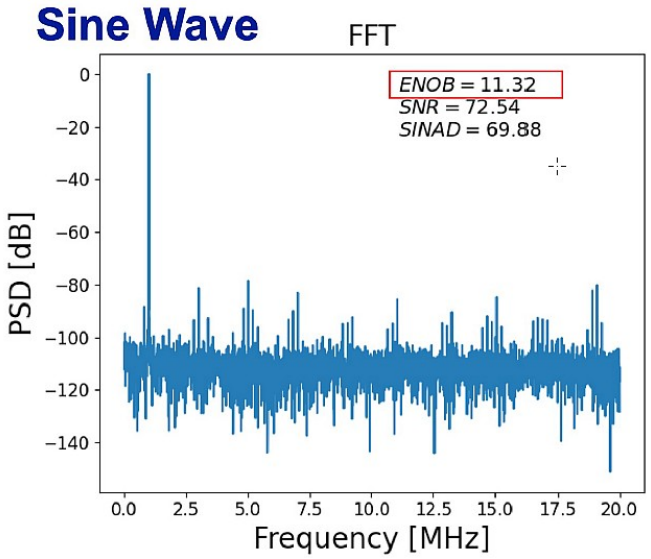
On-detector electronics: Front-End Board (FEB2)

COLUTAV4 Layout



Digitizing the pre-amplified and shaped signals

- COLUTA ASIC designed in CMOS 65nm TSMC technology
- 14-bit (3.5 bit MDAC → 12-bit SAR)
- Digitizes at 40 MHz with two gains
- 4 channels, 8 ADC/ASIC
- Low noise and good long-term stability
- Highly configurable via I2C
- Cross-talk <0.1%
- Coherent Noise < 0.2 LSB



On-detector electronics: integration

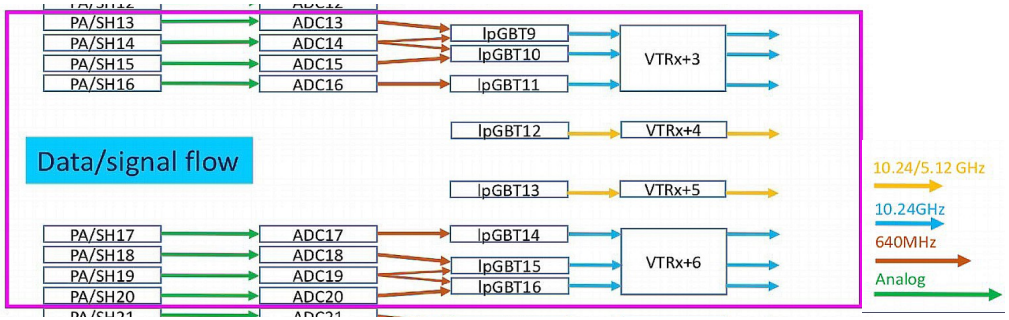
The integration of the ASICs into the FEB is done with a **succession of partially integrated board (slices)** with increasing complexity.

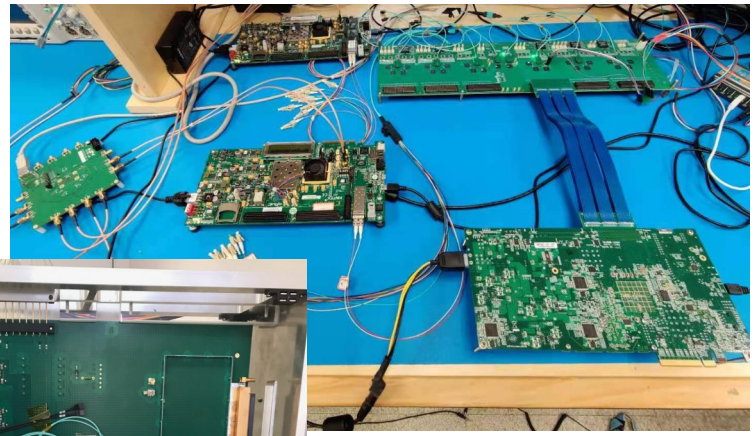
The **Slice test board** integrates the **main components of the final system**:

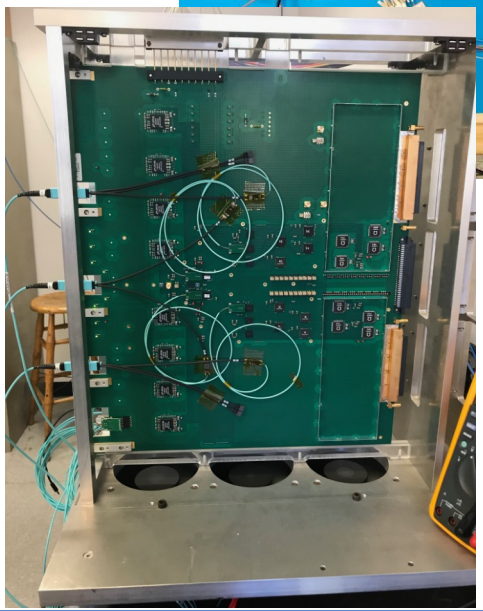
- Control and Data lpGBT for slow control and readout of 8 x COLUTA ADC
- Powering network and Input protection
- VTRx Module for optical transmission
- Signal input via backplane connector for crate integration

The board can be used to **prepare the integration of a test stand for the final production of the FEB:**

- Study of noise, linearity, cross-talk for improvement to FEB2 prototype
- Development of software and firmware for the operation and characterization of the production board







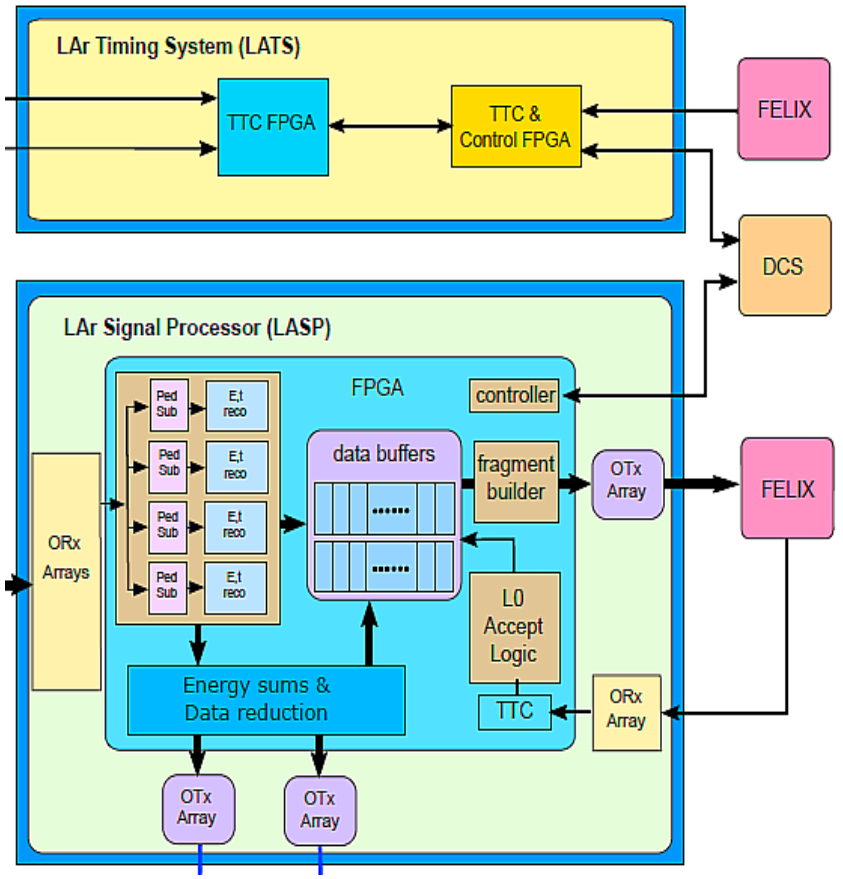
Off-detector electronics specifications

LAr Timing System:

- LATS distributes the Timing, Trigger and Control interface (TTC) to the on-detector electronics (FEB and calibration boards) and handles the configuration and monitoring
- 40 Mhz clock distributed with RMS jitter < 2 ps

LAr Signal Processor:

- LASP boards should acquire the data coming from the 1524 front-end boards ie. 40000 optical fiber @10.24 Gbps ~ 340 Tbps
- Compute signal energy and timestamping
- Feed the data to the trigger system and buffer them until L0-trigger-Accept to send them to the online processing of data (TDAQ)



40 MHz Data:

Calorimeter data reception in L0Calo and L0Muon Processors [μs]	1.7
Maximum skew between all calorimeter inputs to the FEX processors [BC]	16
Calorimeter data reception in Global Event [μs]	1.7
Muon detector data reception in L0Muon [μs]	2.8
Maximum skew between all muon detector inputs to the L0Muon [BC]	72

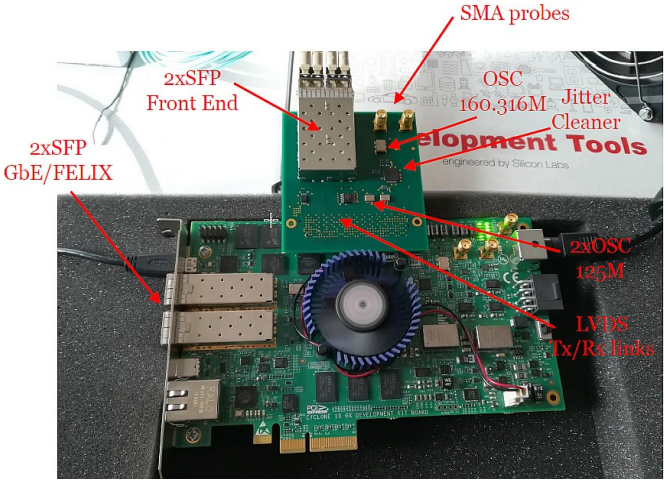
L0 Trigger:

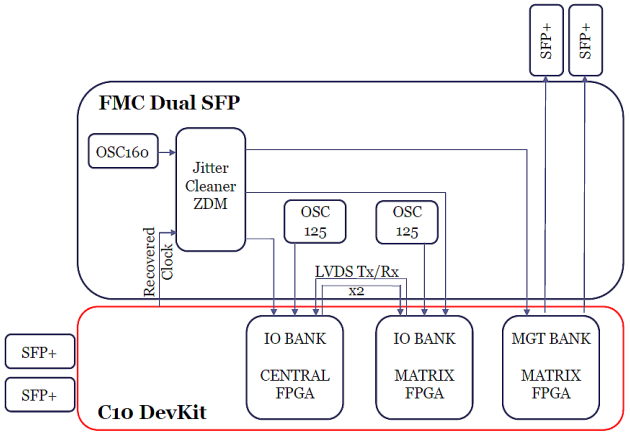
Consecutive triggers [# L0A in # consecutive BCs]	≤ 4 / 5
Burst size [# L0A in # μs]	≤ 8 / 0.5 ≤ 128 / 90
L0 trigger rate [MHz]	1
L0 latency [μs]	10

LAr Timing System (LATOURNETT)

C10 DevKit + FMC Dual SFP:

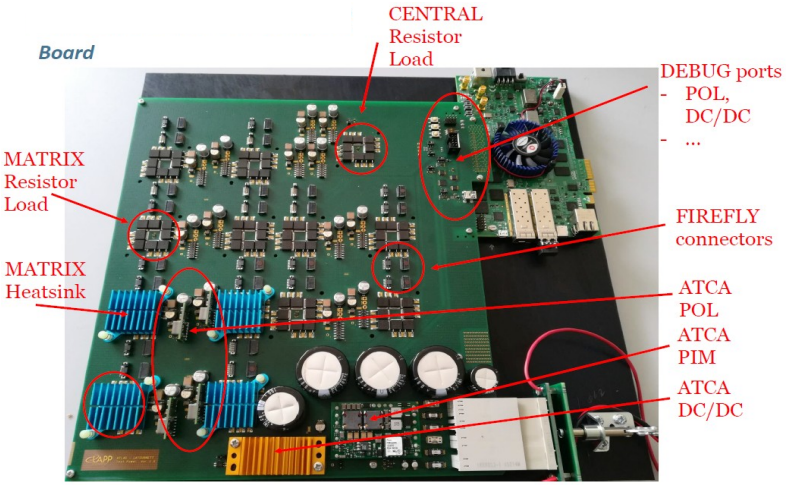
- ✔ emulate optical (SFP) and electrical (LVDS) links
- ✔ validate SI5394(Clock)
- ✔ start develop/test firmware

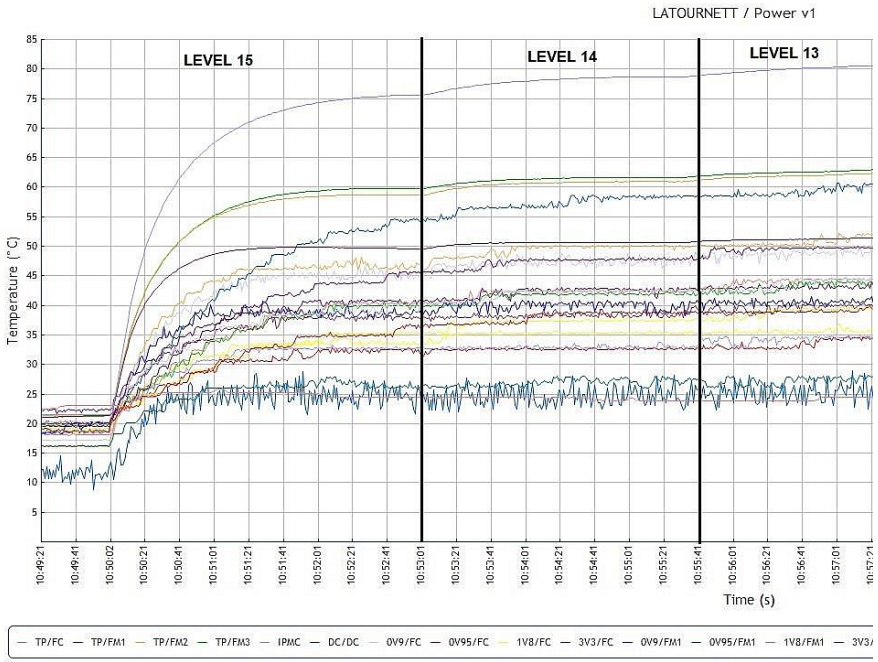




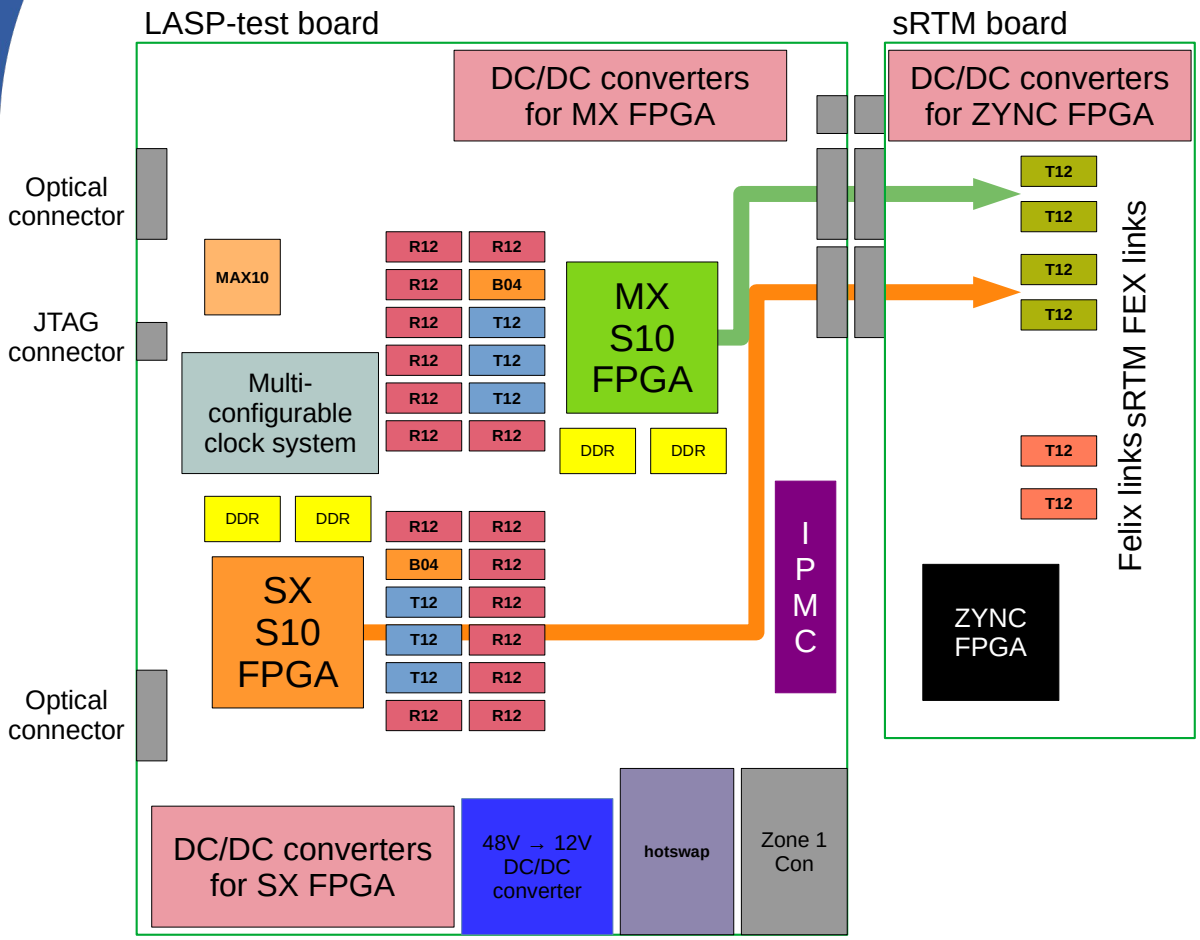
LATOURNETT Power board:

- ✔ emulate power tree with the same physical characteristics than the foressen LATOURNETT board
- ✔ test voltages, power sequences, temperature





Lar Signal Processor (LASP) test system overview



Input data for each processing FPGA :

- coming from 3/4 FEB2 boards (not decided yet)
- # of input links : 66/88 @ 10,24 Gbps

Required number of TDAQ output links per processing FPGA :

- 1 @ 10,24Gbps (or @ 25 Gbps) : FELIX
- 3 @ 25Gbps : Global Event Processors
- 20 @25Gbps : fwd Feature Extractor

Test boards (now):

- available 2021-2022
- 5 boards produced

Prototype boards:

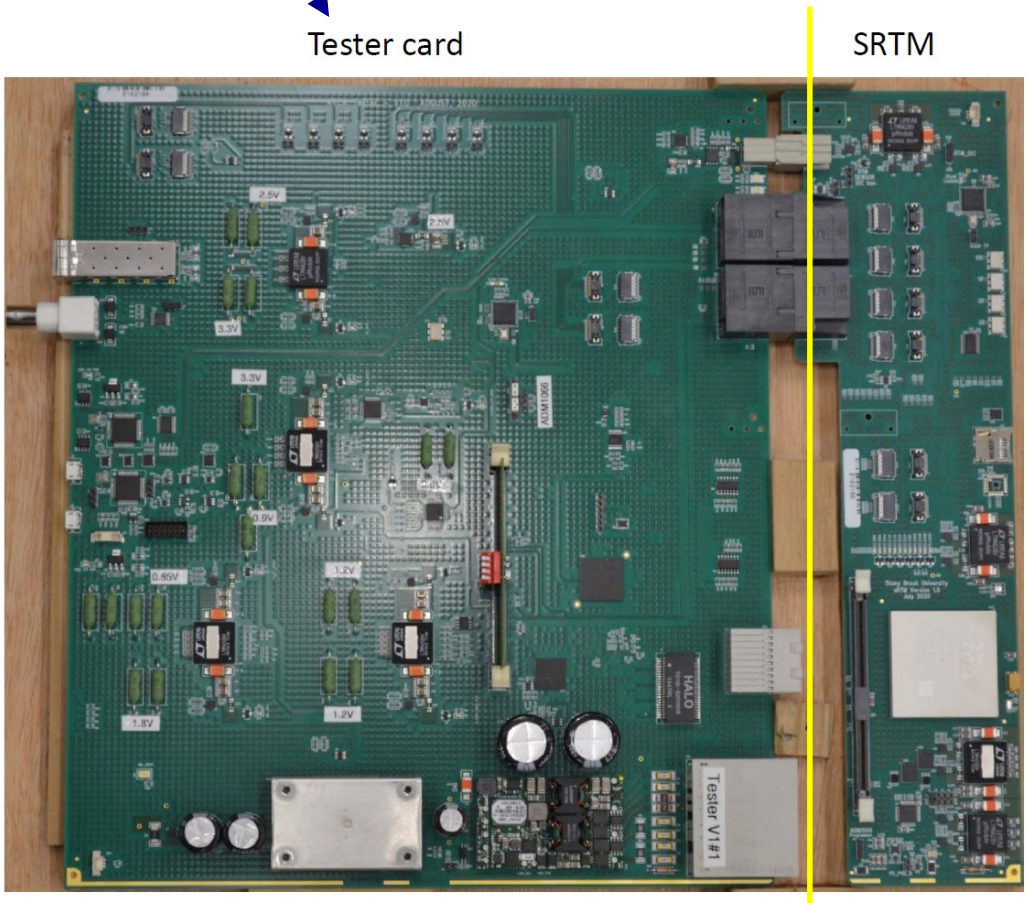
- available 2022-2023
- 6–10 boards produced

Production boards:

- available 2024-2026
- 200-400 boards produced

sRTM board

test purpose waiting LASP board fabricated



sRTM board v1 designed and fabricated:

- based on Zynq

"System infrastructure" tested OK:

- power management infrastructure
- SD card, GbE, I2C sensors (current, voltage, temperature, firefly status)
- clock synthesizer
- firefly "slow control" lines

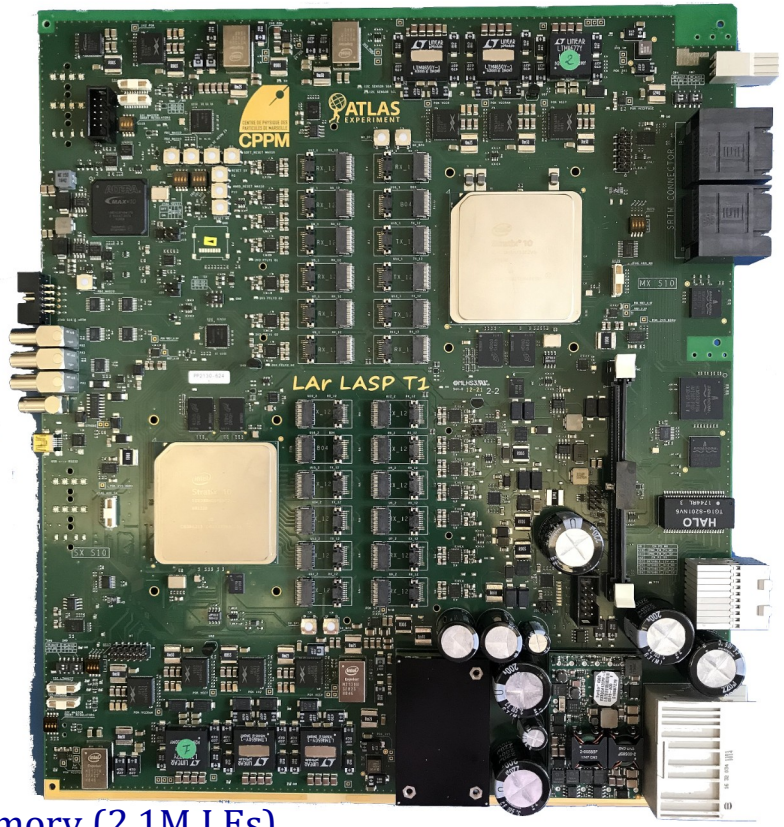
Standard software also available:

- petalinux booting & instructions (readme)
- SRTM specific software not part of petalinux (clock configuration, firefly control/status, sensor read out)

LASP test board

PCB overview :

- ATCA format
- > 4000 components
- 133 schematic pages
- 20 layer PCB (6 signal, 14 power and ground)
- Total thickness : 2.4 mm
- Dielectric material : Megtron 6
- 1st board received in June with FPGA interposer (dedicated to first tests and FPGA power sequencing)
- 1st board fully equipped with FPGA received mid september
- Production of additional LASP test blade for extensive test campaign starting Q3 2021



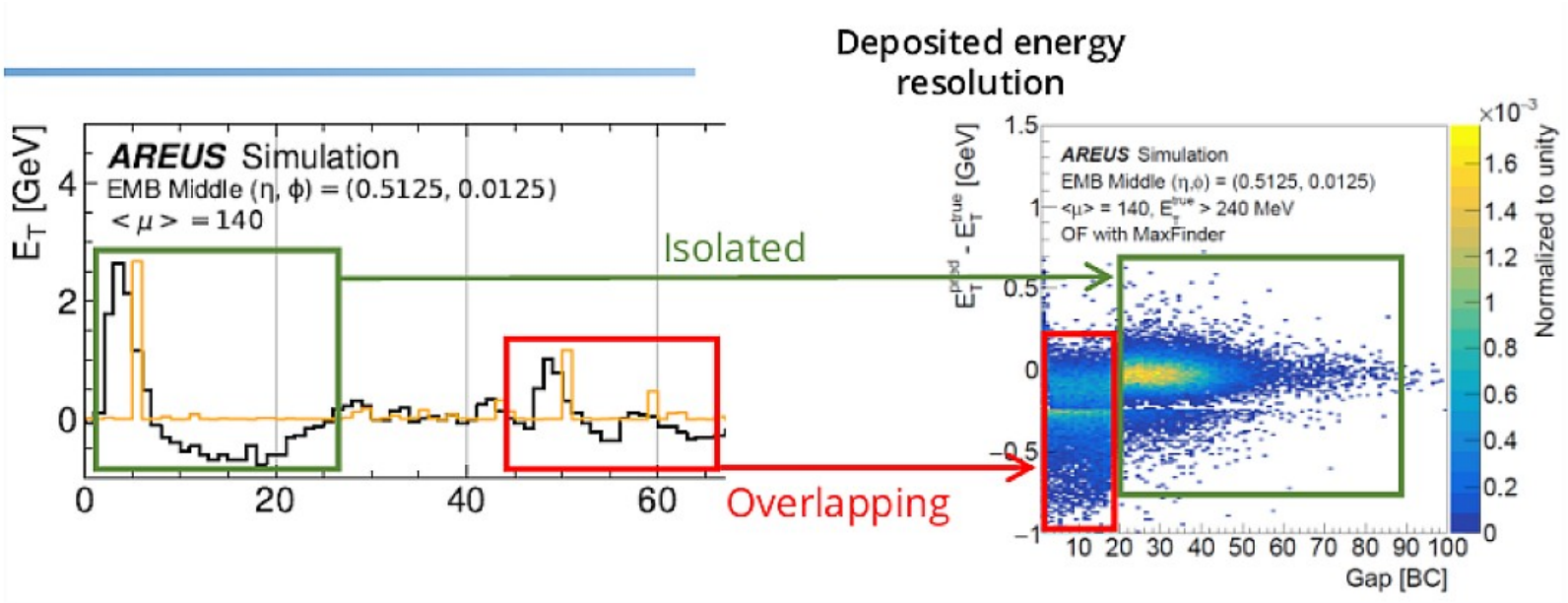
Features :

- 1 INTEL STRATIX-10 SX FPGA with ARM processor (2.8M LEs)
- 1 INTEL STRATIX-10 MX FPGA with high-bandwith DRAM memory (2.1M LEs)
- 1 INTEL MAX10 FPGA as a controller
- 12 Firefly transceiver modules per FPGA (8 x 12RX @ 11Gbps, 3 x 12TX @11 Gbps, 1 x 4RX/TX @25 Gbps)

Challenges :

- Power and cooling : ATCA shelf cooling limit @ 350+50 W/slot
- High speed links @ 25Gbps
- High density / complexity

Towards Machine Learning on FPGAs for real-time data processing ?



Optimal filter is currently used for energy computation, but has **difficulties to reconstruct energies in case of overlapping pulses.**

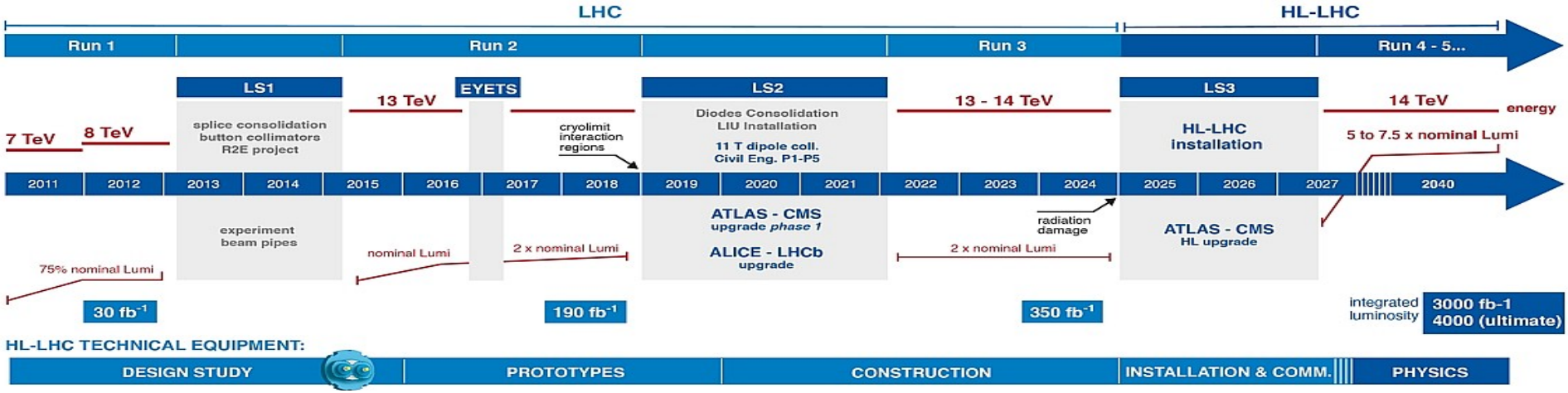
Neural network approach is being developed with prototype firmware implementations to improve the energy reconstruction (see poster by Nemer Chiedde)

Conclusion

Huge effort by many institutes of the LAr group **to prepare the electronics readout upgrade** for HL-LHC collisions starting 2027.

Measurement results performed on **prototypes and test setups** that have been designed show that the **requirements are already met or on very good way to be.**

LASP electronics under development give the opportunity to **implement Machine Learning for signal processing**. First results are promising.



Thanks a lot for your attention !

Questions ?

Backup slides

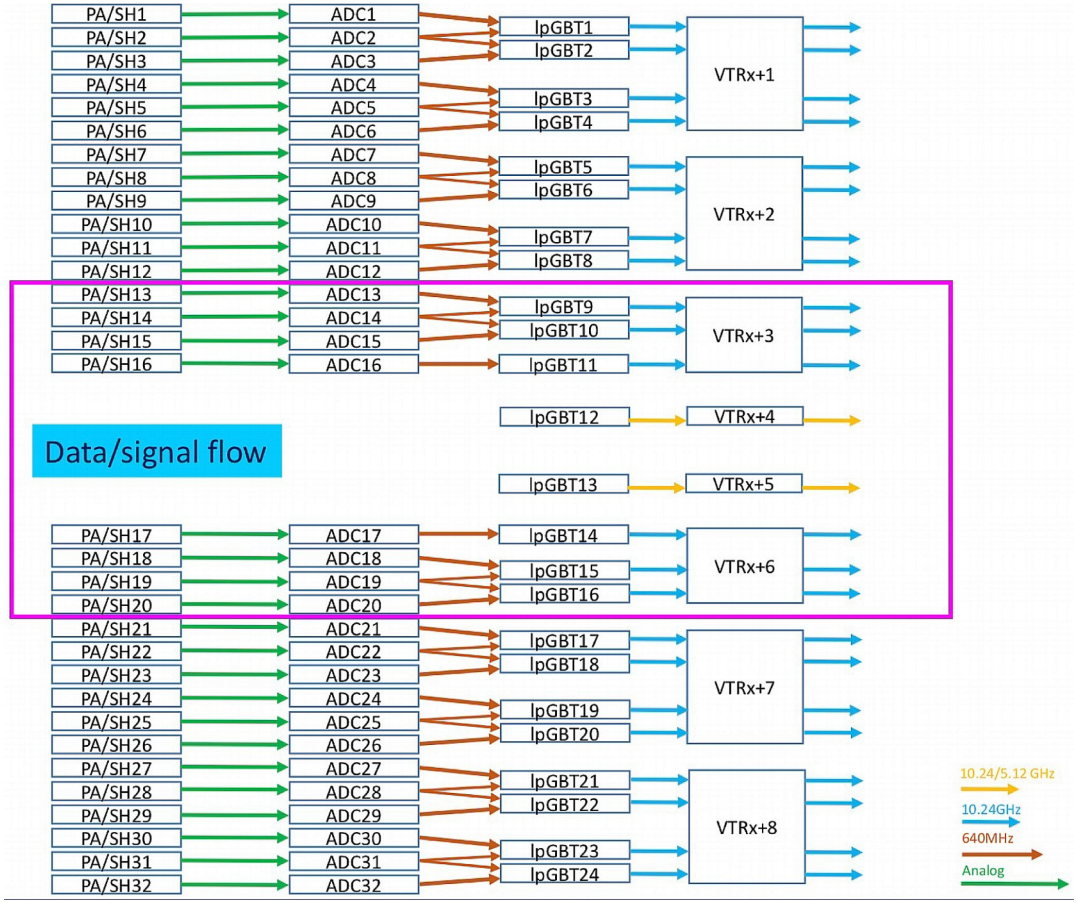
On-detector electronics: FEB integration

The integration of the ASICs into the Front-End Board design is done with a succession of partially integrated board (slices) with increasing complexity:

- Analog Test Board (2019), 2 channels
- Slice Test Board (2020-21), 32 input channels
  LAUROC + COLUTAv3 + lpGBT
- FEB2 Prototype (2022), full readout of 128 channels

The FEB2 slow control makes use of the lpGBT I2C Master, ADC and GPIO to monitor board temperature and configure ASICs

The lpGBT implement a redundancy scheme against VTRx failure

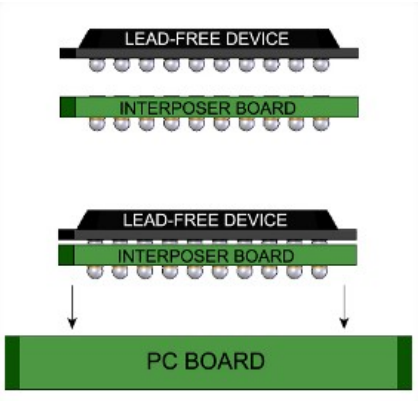


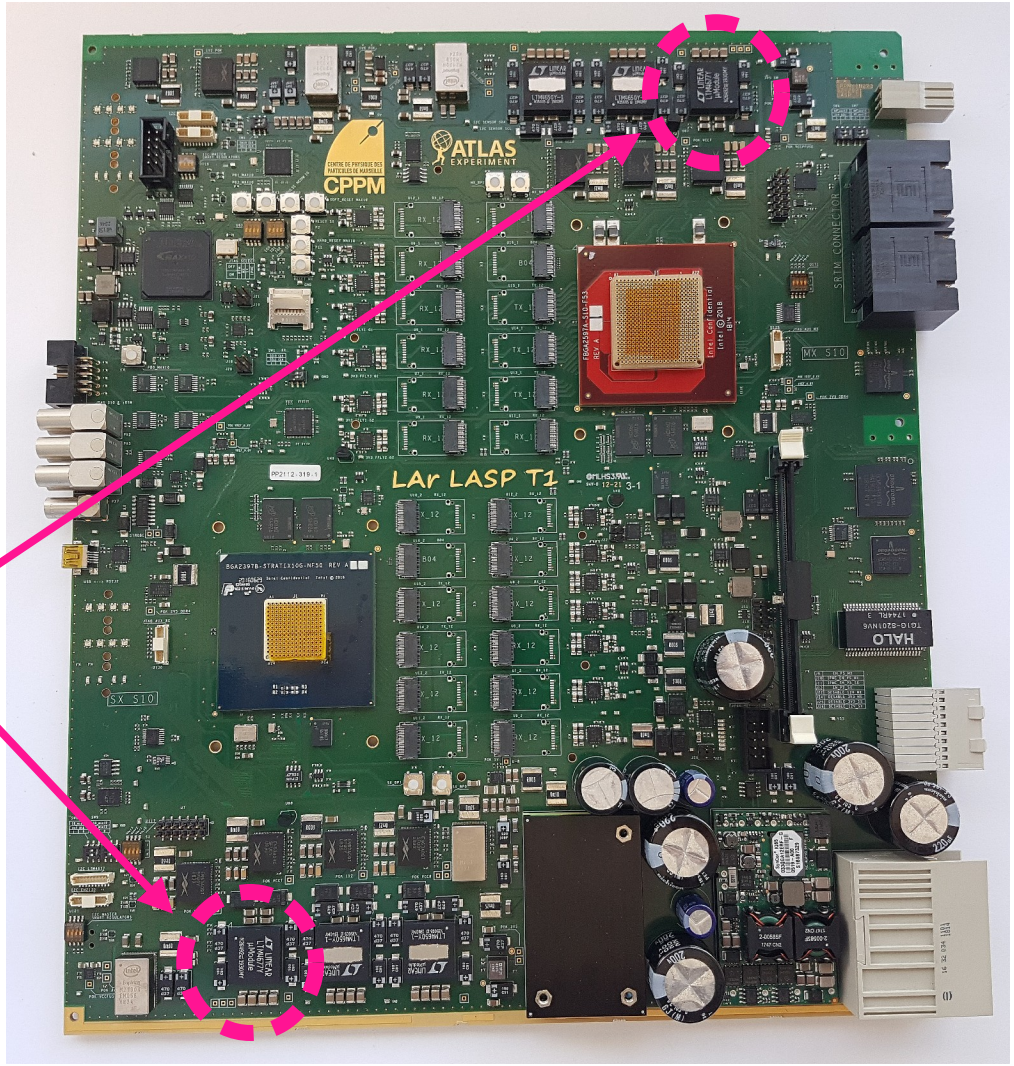
LASP test board : first tests

First tests carried out without FPGAs :

- visual and ohmic
- current regulators
- power sequencing
- static power consumption
- dynamic power consumption
- I2C links
- UART link via GUI

A numbering error in a regulator footprint solved by designing and inserting a custom interposer :

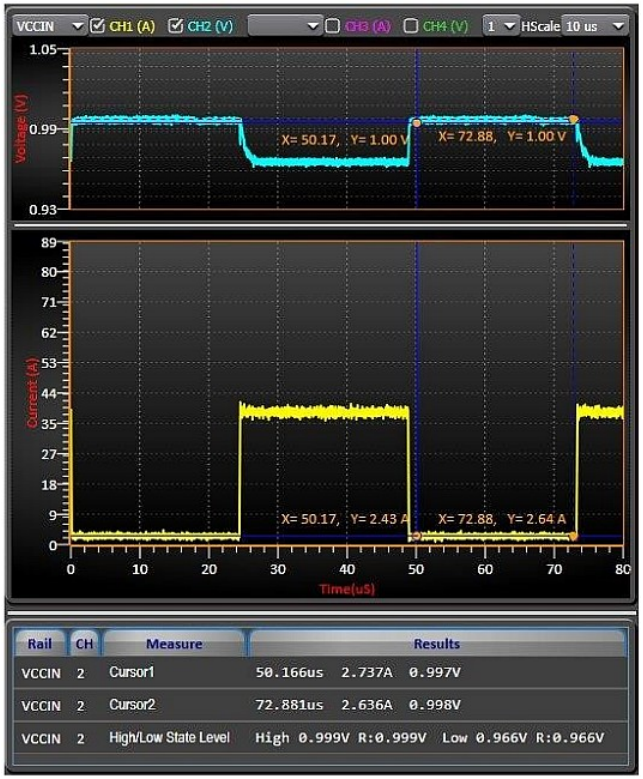




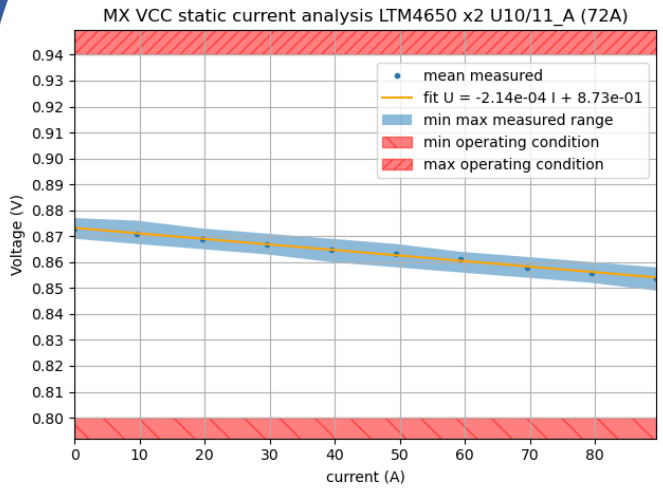
LASP test board : VRTT tests

VRTT : Voltage Regulator Test Tool

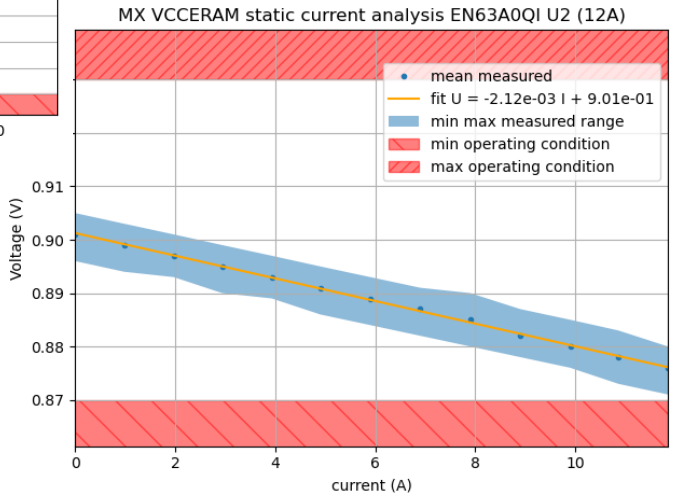
- **Charge emulator designed by Intel**
  - sink currents with given characterics
  - measure voltage variations versus specifications
- **VRTT connects to interposers**
- **Goal : validate the power delivery to the Stratix-10 FPGAs (regulators, decoupling, power planes)**



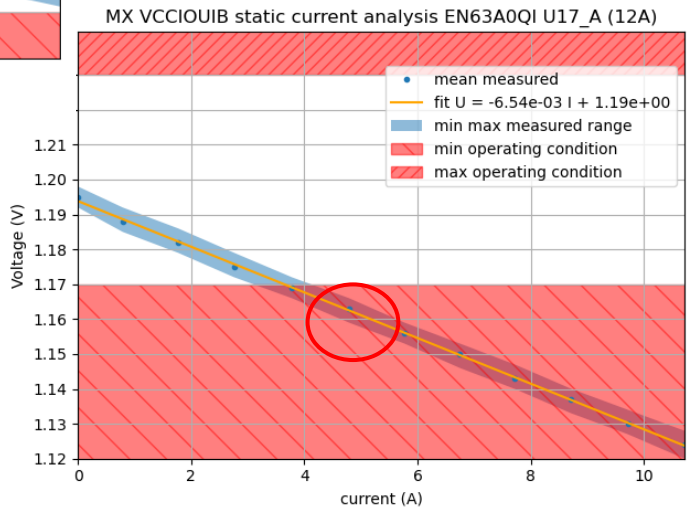
LASP test board : VRTT static tests



VCC core : OK



VCCERAM : OK



VCCIO_UIB core : NOK

➡ new dedicated regulator added (currently shared with VCCIO_1.2V)

➡ power shapes enlarged