The development of the Front-End Boards for the small-strip Thin Gap Chambers detector system of the ATLAS Muon New Small Wheel upgrade

P. Miao,[a] F. Li,[a,1] L. Guan,[b] I. Ravinovich,[c] S. Zhou,[a] N.J. Zhang,[a] Z.L. Zhang,[a] X.X. Wang[a] and G. Jin[a]

[a]*State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China,*
96th Jinzhai Road, Hefei 230026, P.R. China

[b]*Department of Physics, University of Michigan,*
450 Church Street, Ann Arbor, MI 48109, U.S.A.

[c]*Weizmann Institute of Science,*
Herzl St 234, Rehovot, Israel

E-mail: phonelee@ustc.edu.cn

ABSTRACT: The ATLAS experiment at CERN is scheduled to replace the innermost station of its Muon Spectrometer in the forward region during its Phase-I upgrade in order to enhance the capabilities on triggering and tracking of high transverse momentum muons towards high luminosity LHC runs. The New Small Wheel (NSW), a completely new detector system to be built, is composed of two novel gaseous detectors: Micro-mesh Gaseous Structure (Micromegas) and the small-strip Thin Gap Chamber (sTGC). The sTGC sub-system is the primary trigger detector. It will be equipped with radiation-tolerant, low-latency electronics for reading out over 400,000 channels to identify the bunch crossing time of proton-proton collisions spaced by 25 ns, as well as to collect fine strip charge information for the charged track reconstruction. In this paper, we present the design and development of a set of Front-End Boards (FEBs) for the sTGC detector system. The major challenges in the design will be discussed. These include the accommodation of a few hundred readout channels per single board in a very constrained space, a tight requirement for the Electrostatic Discharge (ESD) protection of 130 nm ASICs, and customized analog input circuits to handle the high rate and high charge signals from the sTGC detectors. Moreover, the FEBs have to incorporate a few hundred parallel inter-chip links at 320 Mbps and several low-latency serial links operating at 4.8 Gbps for the Level-1 and trigger data readout. The characterization of the FEBs performance, both off-detector and on-detector, will be shown.

---

[1]Corresponding author.

https://doi.org/10.1088/1748-0221/15/11/P11024

Contents

1   Introduction

After a new era of physics opened by the discovery of the Higgs boson, the Large Hadron Collider (LHC) at CERN will increase its instantaneous luminosity by a factor of five to seven with respect to the originally designed nominal value of $1 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$. This will require a series of upgrades for the ATLAS experiment to precisely study the Higgs boson sector and to extend the sensitivity to new physics in the multi-TeV energy range [1, 2]. To profit from the high statistics, which are expected to be delivered after the LHC collider complex upgrade, the ATLAS experiment is scheduled to replace the current innermost Muon sub-detector system in the End-cap (the current Small Wheel) with the New Small Wheel (NSW) [3] detector system in its phase-I upgrade during the second LHC long shutdown period (LS2). The new Muon detector station, to be built on the surface and delivered as a single 10-m diameter object to the experimental cavern underground, will employ two novel gaseous detector technologies: Micro-Mech Gaseous Structure detector (Micromegas) and small-strip Thin Gap Chamber (sTGC), respectively. The NSW detector system will participate in the Level-1 Muon online trigger [4, 5], a hardware-based first-level event selection, in the forward region, by fast reconstruction of the track segments down to 1 mrad pointing accuracy to the interaction point (IP) to corroborate those segments found at the outer muon detector station, which is behind the toroidal magnet. Additionally, the precision charge and timing information from the fine-pitch strip electrodes laid perpendicular to the muon track bending plane will be read out for a precision off-line muon track reconstruction using several charge-reweighting algorithms. The

NSW system, with the help of novel high-rate capable detectors and custom-designed electronics, is expected to enhance the Level-1 trigger selectivity on high transverse momentum (P_T) muons in the high background environment, with an extrapolated rate of up to about $20\,kHz/cm^2$ [6] in the LHC high luminosity runs, while maintaining the excellent muon tracking capabilities in the forward region of the Muon Spectrometer. The detailed description of the ATLAS Level-1 trigger scheme after the Phase-I upgrade is presented elsewhere [7].

In this paper, we present the design implementation and the characterization of the FEBs for the sTGC detector system in the context of the ATLAS NSW upgrade. Accordingly, the rest of the paper is organized as follows. The NSW detector composition, the sTGC detector technology, and the sTGC electronics complex are reviewed in section 2. The general specification requirements for the sTGC FEBs and the detailed design implementation are discussed in section 3. Following that, results on both the off-detector and on-detector measurements and key performance characterization during full chain electronics integration campaigns and the detector electronics integration studies will be shown in section 4. The summary of the design experiences and conclusion based on crucial test results will be given in section 5.

2 The New Small Wheel detector system and the sTGC electronics architecture

2.1 The New Small Wheel structure and the sTGC detector

The two NSW detectors, one for each Endcap of the ATLAS Spectrometer, are to be built as disk-shaped objects with a diameter of around ten meters. The composition and the detector arrangement for each NSW disk is illustrated in figure 1. Each NSW disk is composed of 16 sectors. There are sixteen active detector layers instrumented per sector, with an eight-layer Micromegas double-wedge sandwiched between two sTGC wedges. The sTGC wedges are assembled with three different-sized sTGC quadruplets.
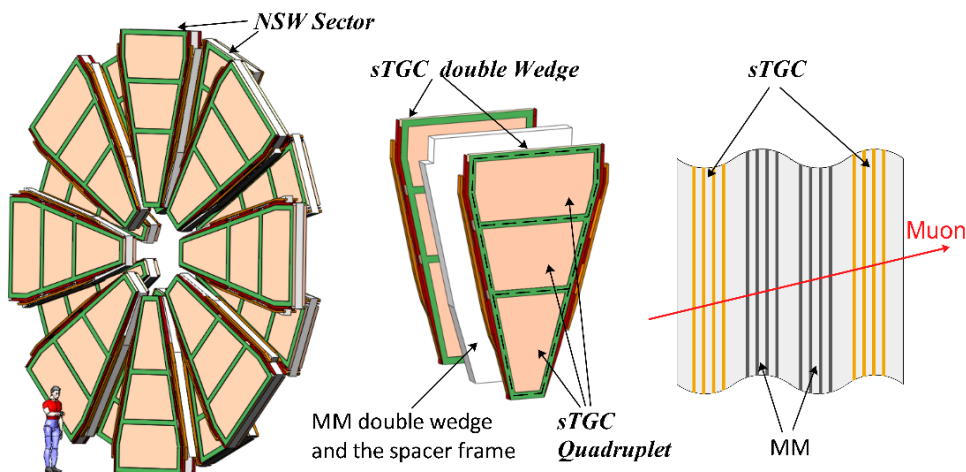

Figure 1. The New Small Wheel mechanical structure, composition of one NSW sector and the cut-view of the NSW sector layer stack.

The basic structure of an active sTGC gas gap is depicted in figure 2(a). A wire plane, constructed with $50\,\mu m$ diameter gold-coated tungsten wires spaced $1.8\,mm$, is laid between two

graphite coated resistive cathode planes at 1.4 mm from the wire plane. The signal pick-up electrodes, separated by about 0.2 mm thick fiberglass laminations, are capacitively coupled to the resistive cathode planes. They are divided into 3.2 mm pitched strips on one cathode plane, in order to precisely measure the hit positions in the bending direction. The readout electrodes on the other cathode plane are segmented into about 8 cm wide and varying length pad patterns, in order to do fast triggering as well as providing coarse second coordinate measurements for the reconstructed tracks. The orientations of the sTGC strips, pads, and wire groups within an NSW sector in the ATLAS coordinate system are illustrated in figure 2(b). It should be noted that muons are bent in the y–z plane by the Endcap magnet in the experiment. The induced current signals from the ionizations and avalanches created by the passage of the charged particle are read out from more than 400,000 Front-End electronics channels. The induced signals from the wires are negative in polarity, whereas they are positive for the strip and pad readout. Thanks to the thin gas gap design with a good timing response for LHC bunch crossing identification, sTGC is the primary trigger detector for the NSW, while both NSW detector technologies provide complementary trigger and tracking capabilities.
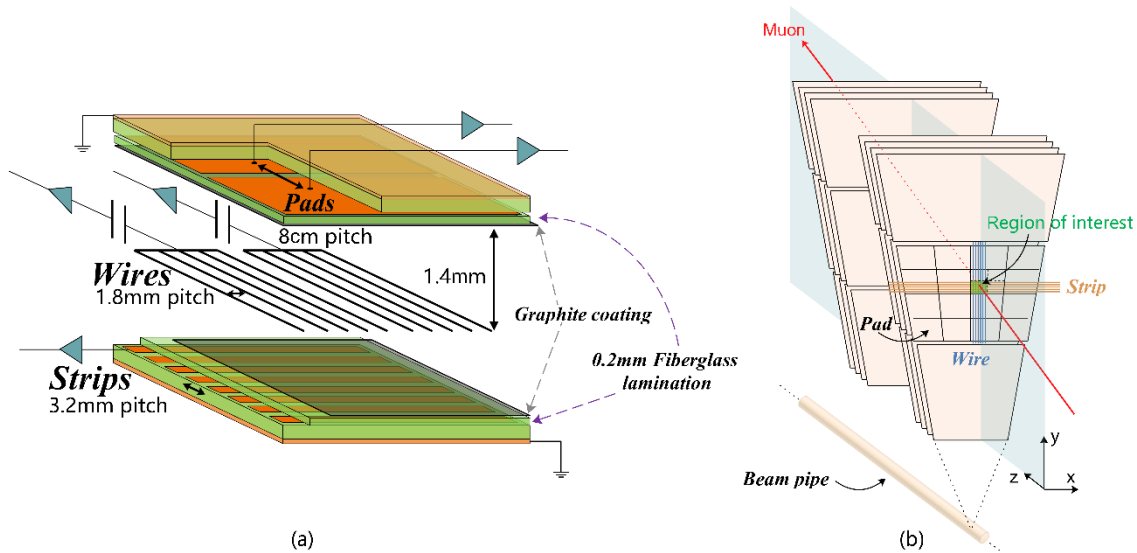

Figure 2. The basic structure of the sTGC gas gap (a) and the orientation of sTGC wire, strip and pad readout electrodes in an NSW sector with the ATLAS coordinate system (b).

2.2 The sTGC readout and trigger electronics

The NSW detector system is instrumented with an electronics system based on a set of application specific integrated circuits (ASICs). In general, the NSW electronics system is designed to handle the data with a granularity of the NSW sector. Such an architecture allows the management of 32 NSW sectors individually. A simplified block diagram of the sTGC electronics complex is shown in figure 3. The entire electronics chain is divided geographically into two sections, with several radiation-tolerant Front-End electronics components installed on or near the sTGC detector wedges and a set of high-throughput Back-End electronics, common to both sTGC and Micromegas, deployed in the underground service area. The demand for the sTGC to perform simultaneous fast

triggering and precision tracking resulted in the establishment of two separate data paths utilizing individual electronics cards or modules as highlighted in blue and purple colors in figure 3. The data path with components highlighted in blue is dedicated to the Level-1 data readout whereas the other is responsible for the construction of the Level-1 trigger at the NSW station. These two data paths are all started from the sTGC Front-End electronics connected to sTGC readout electrodes.

The sTGC Front-End electronics mainly consists of three types of Front-End ASICs hosted on the sTGC FEBs. The VMM [8], a multi-channel mixed-signal Front-End ASIC, provides charge amplification, discrimination, as well as the fast digitization of charge and timing information using novel integrated analog-digital converters (ADCs). It is also capable of generating direct timing pulse output for each channel in low latency trigger applications. Several VMMs on the same FEB is connected to the Readout Controller (ROC) ASIC [9] in which readout data packets are aggregated. The distribution of Trigger, Time, and Control (TTC) signals, used for the readout and trigger electronics synchronization, are also handled by ROC ASIC. The Trigger Data Serializer (TDS) ASIC [10, 11], adapted for operation in pad or strip mode, is connected to the VMM direct output to capture the Time-over-Threshold (ToT) pulses from the sTGC pads or the fast charge ADC data from the sTGC strips. These raw trigger data are processed inside the TDS and sent out via the TDS gigabit transceivers.

The sTGC readout chain is constructed with the FEBs connected to the Level-1 Data Driver Cards (L1DDCs) [12] on the wedge via thin passive copper cables and the L1DDCs communicating with the Back-End readout link exchange system, named as FELIX [13], via optical fibers running over a hundred meters. The L1DDC cards host several GBTx ASIC [14] and radiation-hardened optical transceivers developed at CERN. These L1DDCs act as common hubs to merge a group of low-speed (80–320 Mbps) links, carrying readout, slow control and TTC data from several FEBs per wedge plane, into serial high-speed (4.8 Gbps) links for the Front-End and Back-End communication. The NSW readout data acquisition system needs to meet both the requirements for the ATLAS Phase-I and Phase-II upgrade since the detector system will remain active with limited access until the end of high luminosity runs. The general requirement is the capability to deal with a single level trigger at 100 kHz after Phase-I upgrade and a maximum trigger rate up to 1 MHz at a fixed latency of 10 μs after Phase-II upgrade. Consequently, a deep buffering of hit data at the Font-End to retain hit information is expected in the readout ASIC design, taking into consideration the background hit rate, cluster size, and trigger matching window. Moreover, the FEBs and the L1DDCs are required to handle the subsequent high bandwidth up to the Phase-II scenario.

The sTGC trigger chain is designed to utilize the sTGC pads from eight active layers within the NSW sector to perform "pre-Level-1" coincidences and consequently limit the on-detector trigger electronics to only send out the charge data from a band of strips underneath the region-of-interest defined by the pad coincidences. sTGC pads on different layers are staggered in the direction orthogonal to the strips such that the pad coincidence could locate a region that spans less than fourteen strips. This scheme is illustrated in figure 2(b).

The sTGC trigger chain is composed of the Pad Trigger Board [15], the sTGC Router Board [16], and the sTGC Trigger Processor Cards. Both the Pad Trigger Board and the sTGC Router Board are FPGA-based electronics cards to be installed near the rim of the NSW. One Pad Trigger Board is allocated for each NSW sector to receive pad hits from all eight sTGC layers per sector. Discriminated pad hits from a detector plane are first passed from VMM to the pad-TDS in the

form of ToT pulses and then sampled by the TDS ASIC. Aggregated pad hits are then sent to the Pad Trigger Board at every bunch crossing. Two sets of three-out-four pad coincidences from two sTGC wedges within the NSW sector are performed at the Pad Trigger Board. This "pre-Level-1" trigger information is sent back to the strip-TDS, in terms of the bunch crossing identification (BCID), strip-band ID and a second coordinate (φ) ID, for selecting relevant fast charge data from the covered strip band. The sTGC Router Board is introduced as a high-speed switch to pass up to four out of twelve serial strip-TDS links per detector plane to the sTGC Trigger Processor, as not all strip-TDS links are sending active hit data at the same bunch crossing.

The general requirement for the sTGC trigger path is to generate sTGC Level-1 trigger primitives with a fixed latency of ~1 μs after the bunch crossing, to be in-time with the outer Muon station (named as Big Wheel) for making Muon Level-1 trigger decisions in the forward region of the spectrometer. This places stringent demands on the design of fixed low-latency trigger electronics as well as the handling of a large number of high-speed inter-chip and inter-board data links.
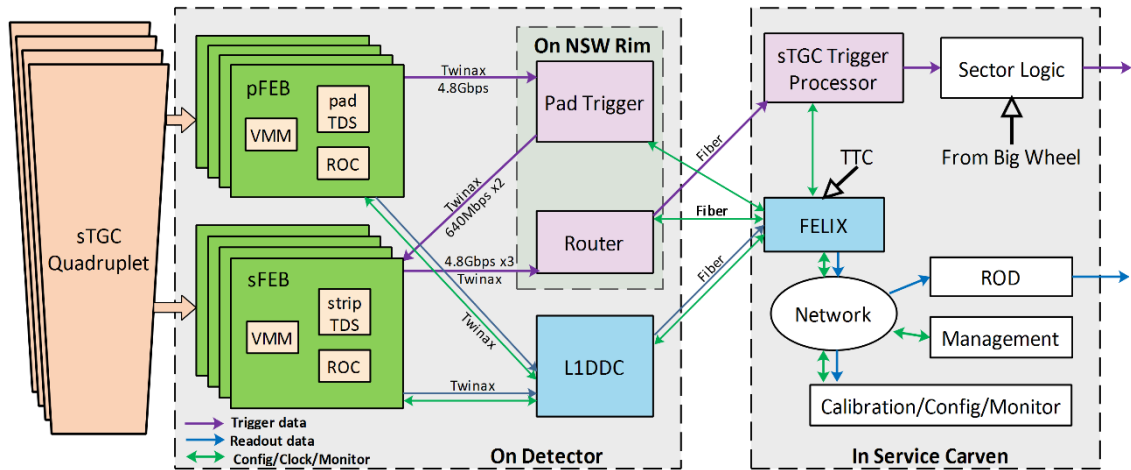

Figure 3. The simplified block diagram of the New Small Wheel sTGC electronics architecture.

3 sTGC FEB design

3.1 Design specifications and functional requirements

The general design specifications and guidelines for the development of sTGC FEBs are listed as following:

- Provide reliable connections with the sTGC readout electrodes as well as interfaces with on-detector service elements, such as cooling plates, data and power cabling, while building mechanical assemblies of FEBs fit inside the global sTGC detector envelope.

- Proper handling of the analog signals from the sTGC readout electrodes and minimize any form of noise aggression from the on-board power regulator or digital circuit to the sensitive on-board Font-End ASICs when integrated with the detector system.

- Appropriate arrangement of interconnections among on-board ASICs, as well as the connection to peripheral sTGC electronics cards, to ensure the synchronization, correct functioning of the readout and trigger channels in view of the full sTGC electronics chain operation.

The first requirement, taking into the consideration of sTGC detector geometry described in the preceding section, implies the need to develop sTGC FEBs with two types: pad-FEB (pFEB) and strip-FEB (sFEB). Each sTGC gas gap within an sTGC quadruplet will be connected to a pair of pFEB and sFEB which could be operated independently from other layers. In total, there are around 30 wire groups, up to 112 pads, and up to 400 strips within the sTGC gas gap. The pFEB will be responsible for the readout of both pads and wires whereas an sFEB will be dedicated to the readout of the entire strip plane. Special considerations in the FEB design to accommodate the mechanical restrictions, noise optimization could not be explained without mentioning the actual board layout implementation details. Therefore, they are elaborated in the succeeding sub-section. The functional design requirements leading to the complete on-board connectivity scheme could be explained with the block diagrams in figure 4 and figure 5 for the pFEB and the sFEB, respectively.

For the pFEB, analog signals from sTGC pads are routed via a high-density connector and a dedicated analog input network before been sensed by two 64-channel VMM3a ASICs [17], the production version of the NSW Front-End ASIC. In the trigger path, these two VMMs have their direct output connected to a 104-channel pad-TDS where ToT pulses are sampled with the 40 MHz bunch clock. This TDS channel count in the trigger path, less than the maximum sTGC pad count per gas gap, is mainly limited by the transceiver bandwidth which could only send out 120 bits per 25 ns bunch crossing with 12 bits allocated for the BCID and additional 4 bit as the data packet header.[1] Nevertheless, it is adequate to provide the required trigger coverage at the NSW with a pseudo-rapidity of 2.4. The output of the pad-TDS is routed to a Serial AT Attachment (SATA) connector which is connected to the Pad Trigger Board via a SATA breakout cable. The sTGC wire groups are connected to a third VMM without the use of its direct output as no trigger function is required.

In the pFEB Level-1 data readout path, two serial data lines running at 320 Mbps and from each of three VMMs are connected to the same ROC ASIC. Upon the reception of the Level-1 acceptance, it is registered by the ROC ASIC in its trigger FIFO and broadcasted by the ROC to all VMMs within the same bunch crossing (BC). A first stage trigger match is therefore done in the VMM with a programmable trigger window of up to 8 BCs. Thanks to the VMM design as a System-On-Chip (SOC), each hit is digitized with three fast ADCs and represented with a 10-bit charge ADC, an 8-bit timing ADC count and the associated BCID. Any hit data buffered inside the VMM latency FIFO that matches the incoming trigger within the predefined trigger window are copied to the so-called Level-0 FIFO where all channel hits associated with the trigger are collected and formatted into a single Level-0 packet. The Level-0 data packet is subsequently transmitted to the ROC by these serial data lines. There are four sub-ROC processing units inside the ROC. Data packets from each VMM are first buffered inside a ROC channel FIFO and then could be flexibly routed to one of the sub-ROCs where a complex state machine searches all the hit data associated with a Level-1 trigger and performs a second-stage trigger match to build the Level-1 event packet. This second-stage is needed due to the long latency required for the Phase-II upgrade, when the data

---

[1]See TDS and ROC ASIC specification documents available at https://indico.cern.ch/event/446382/.

buffered in the ROC could originate from two consecutive LHC orbits. More detailed description of the ROC logic can be found in 1. The Level-1 packets are encoded with the 8b/10 scheme and transmitted off-board from four sub-ROCs each with the capability to operate at 80, 320 or 640 Mbps. Besides the level-1data packets, 40 MHz BC clocks and the synchronous reset or test pulse signals for both the VMM and the TDS are served centrally by the ROC.

For the slow control of the pFEB, such as ASIC configuration and some environmental status monitoring, the radiation-tolerant GBT-SCA ASIC [18] developed at CERN is used. The GBT-SCA ASIC communicates with the Back-End electronics via the High-Level Data Link Control (HDLC) protocol running via three differential pairs at 80 Mbps. It provides the needed I2C, SPI interface to configure the NSW ASICs. In addition, it has an embedded ADC and 32 General Purpose Input and Output (GPIO), which have been used for the monitoring of VMM baseline, temperature and the control of NSW ASIC hard resets.
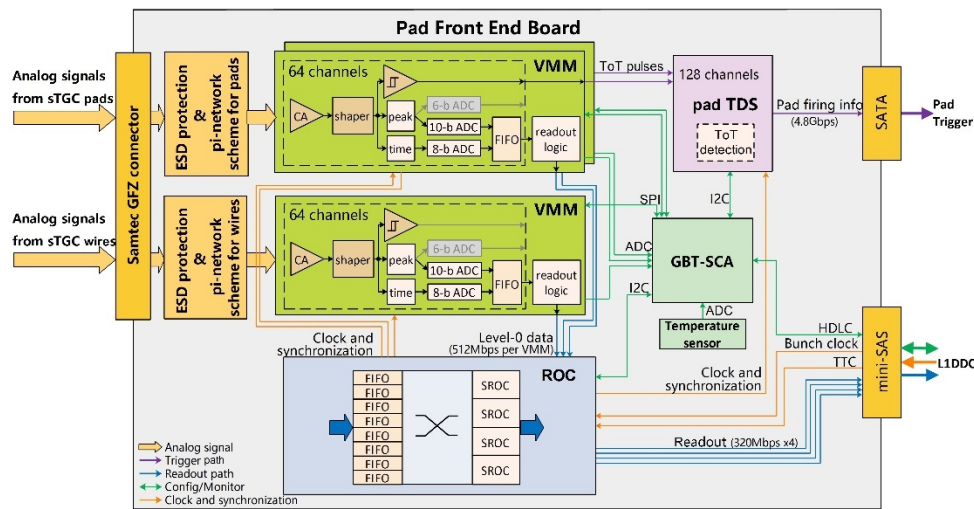

Figure 4. The functional block diagram of the sTGC pFEB and the connectivity on board.

For the sFEB, the Level-1 data readout is based on the same scheme as implemented on the pFEB except the handling over more VMMs. However, the trigger path on the sFEB is much more complex than on the pFEB as a fixed latency pad-strip trigger data match is required. There are 128 differential pairs of direct output from two VMMs connected to a strip-TDS and the 6-bit charge ADC data are transmitted after a peak from the shaped strip input signal is found in the VMM analog circuit. In total, four VMM-TDS groups are populated on one sFEB to handle all strip channels per sTGC gas gap. These coarse strip charge data are sampled by the TDS with its 160 MHz clock and stored inside its ring buffer of 4-BC deep. The sTGC pad coincidence information streamed to the strip-TDS at every BC, utilizing two 640 Mbps lines, are captured by the TDS internal logic. The look-up-table (LUT) translates the incoming strip band ID into a range of strips to be selected. Subsequently, the 6-bit charge data from up to 14 strips, together with the lower 6-bit BCID, the strip band ID, and φ-ID are scrambled and shifted out as four 30-bit packets. Since the pad trigger input is sent to the strip-TDS via the synchronous protocol, four TDSs on the same sFEB are sharing the same 320 MHz clock, BCID and the enable signal lines, but not the line carries strip band-ID and φ-ID information, from the Pad Trigger Board. To save the number of ports used on the Pad

Trigger Board in another constrained space, three Commercial-Off-The-Shelf (COTS) 1:4 fanout chips are used on the sFEB. Since the fanout chip introduces a delay of around 100 ps, trace delay compensation for the pad trigger input data line without passing the fanout chip is needed to avoid the timing violation of the 640 Mbps interface.

The connectivity of the pFEB and sFEB in the NSW system with the peripheral boards is realized with the 8-differential-pair Twinax cables. The number of differential pairs from one cable is enough to accommodate the BC clock, TTC, SCA lanes plus four 320 Mbps E-links from the ROC. Given the calculation in [19] show that the maximum data rate per sTGC gas gap in the ultimate Phase-II scenario would be around 600 Mbps and 1200 Mbps for pad & wire and strip readout, a second Twinax cable is needed to deal with the maximum rate from the innermost sTGC strip planes. Together with the two cables for the connections with the Pad Trigger Board and the sTGC Router, in total, four Twinax cables hence four mini Serial Attached Small Computer System Interface (mini-SAS) connectors are needed for one sFEB.
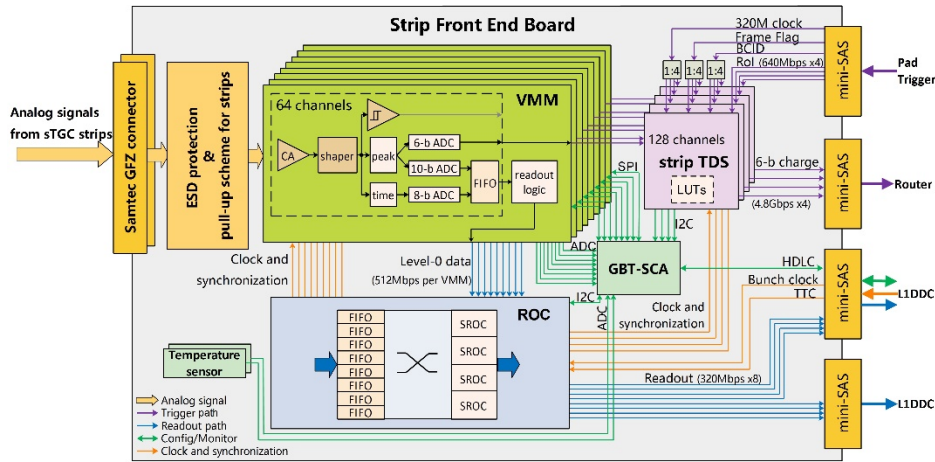

Figure 5. The functional block diagram of the sTGC sFEB and the connectivity on board.

3.2 Design implementation

The actual design implementation of the FEB layout and routing relies on the fact of meeting several demands from the overall detector system point of view, besides those functional requirements mentioned in section 3.1. The following several points are of particular concern and the design implementations are discussed in the following:

- **Mechanical constraints and connection to the detector**: to reserve spaces for the on-wedge power and gas services running along the radial direction of the sTGC wedge on the side, a very tight size restriction is imposed on the FEB in all three dimensions. This restriction poses challenges for the layout of FEBs with large channel counts as well as the selection of connectors for the interface of FEBs with the detector. The connectivity of an sTGC quadruplet with the FEBs are demonstrated in figure 6. Both pFEBs and sFEBs are connected to sTGC strips, pads, or wires with the help of a set of adapter boards. These pad or strip adapter boards are 4–6 layered printed circuit boards (PCBs) soldered on the side of

the gas gap using jumper wires. In the detector depth direction, FEBs after installation must be within the detector envelope of about 40 mm in thickness, to avoid obstructions of laser beams illuminated from the wedge alignment platforms which are glued on the surface of the wedge. The widths of FEBs are restricted to 7.6 cm, merely enough to place three 2 cm × 2 cm sized VMM chips side by side. The length constraints for FEBs could be understood with the FEB placement shown in figure 6(a). The pair of pFEB and sFEB for a gas gap must be installed on two opposite sides of the sTGC quadruplet. The displacement along the side of the sTGC quadruplet is limited for the pFEB and the sFEB which are on the same side but from two adjacent layers. Extensions of the pFEB and the sFEB in the length direction are required to be less than 16.3 cm and 27.5 cm, respectively.

An ultra-low profile (3 mm thickness), high-density board to board connector named GFZ [20] is adopted for the electrical connection between FEBs and adapter boards. This GFZ interposer has a spring-loaded pin array with 300 pin counts, enough for 256 readout channels. Two GFZ connectors are used for an sFEB. The installation of FEBs is done by applying compression forces around the GFZ connector using screws. As shown in figure 6(b), both FEBs are designed with active chips facing outward the wedge surface when installed on the adapter boards. This allows an easier coupling of active chips later to the cooling plates from the outer surface of the wedge assembly while maintaining the lateral profile of one FEB-adapter-board assembly comparable to a gas gap thickness to remain within the allocated envelope.
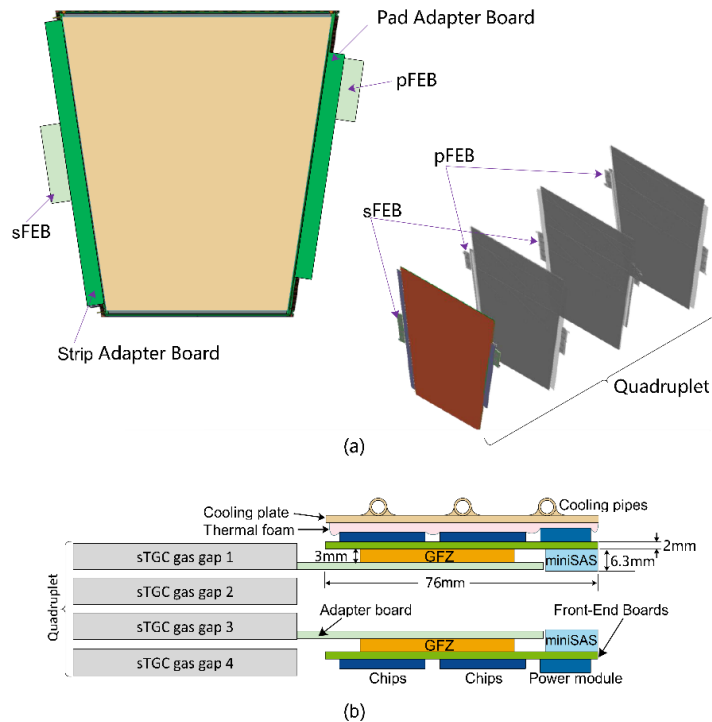

Figure 6. The top (a) and side view (b) of the sTGC detector and FEB connection mechanism.

- **Power and cooling**: the voltage and current for the NSW ASICs and the fanout chip are listed in table 1. The sTGC FEBs should provide several independent power rails to deliver up to a few amperes of current at low voltage. In addition, the VMM analog circuit has a particularly high sensitivity to any forms of conducted or irradiated noise. The traditional method of using DC-DC converters followed by LDOs could provide the desired low ripple and low noise solution. However, the demand for handling large current could be a limiting factor for such an application, as this approach is known to yield low efficiency with a significant amount of heat dumped on board. Moreover, the power supply components should be tolerant to the radiation and the magnetic environment as specified in [21]. Earlier studies shown in [22], considering these requirements, resulted in the design of the FEB power scheme to be based directly on the radiation-hard FEAST DC-DC converters [23] developed at CERN.

The FEAST DC-DC converter takes 10 V input and is capable to regulate the low voltage output with a maximum current of 4 A. sTGC FEBs incorporate the FEAST regulation circuit recommended in its datasheet [24], including both π-filters at the input and the output stage, together with a specially selected main inductor for the output node. The layout of the FEAST module is shown in figure 7(a). This power module is directly implemented on the FEB to minimize the footprint as well as the height. The layout is optimized to minimize the propagations of conducted noise from the switching nodes operated at a 2 MHz switching frequency. This optimization is visible as the placement of filtering capacitors and the main inductor near the FEAST pins, aiming at reducing the impedance for the switching current flow. Due to the FEB height constraint mentioned earlier, air-core COTS inductors are found too bulky to fit. Instead, a shielded 1 µH inductor with iron-powder core is chosen. The lab tests show that the inductor is not saturated at a magnetic field of 0.5 T, an extreme of the fringing field near the NSW where the sTGC FEBs to be mounted. To further limit the switching noise irradiated from the FEAST, a 0.3 mm thick nickel-silver shield is soldered around the module to provide a hermetic sealing.

Table 1. Required voltage level and the maximum current for active chips on sTGC FEBs.

Power rail	Voltage (V)	Maximum current (A)	Maximum power consumption (W)
VMM ASIC analog	1.2	0.75	0.9
VMM ASIC digital	1.2	0.3	0.3
TDS ASIC	1.5	0.63	0.95
ROC ASIC	1.2	0.8	1.0
GBT-SCA	1.5	0.043	0.06
Fanout chip	2.5	0.1	0.25

The FEB cooling in the final system uses 17°C water running over copper cooling loops to extract the heat from the top of the active chips. For the FEAST power module, the top-cooling scheme, shown in figure 7(b), is chosen instead of the default scheme of cooling from the bottom of the chip via thermal vias. This is mainly driven by the demand to minimize the irradiated noise from the FEAST as the FEAST module must be placed on the top side of the FEB, which is far away from the sTGC signal adapter board. The thermal interface for the
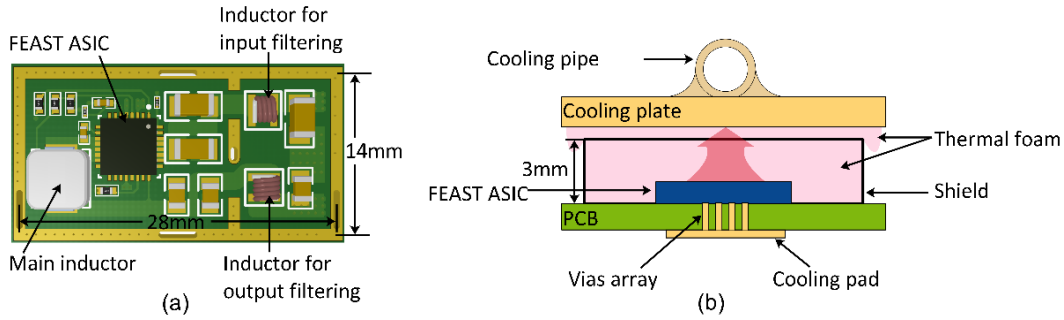
Figure 7. The FEAST DC-DC module layout (a) and the top-cooling scheme (b).

FEAST circuit is provided by filling the gaps among the FEAST circuit, the metal shield, and the cooling pate with electrically insulating thermal gap pas. To reduce the thermal stress and increase the robustness of the power circuit over the long term, several FEAST modules are placed on FEBs such that each module is loaded with less than 2 A current, half of the FEAST rated maximum. Given the fact that the FEAST efficiency in this condition is around 75%, approximately 1 W of heat per power module needs to be absorbed by the cooling system. By using a thin layer of thermal gap pad with 5 W/m·K thermal conductivity, the cooling is experimentally determined to be sufficient to keep the FEAST as well as other on-board chips at a temperature below 50°C and hence a large thermal safety margin exists. Thermal measurement results are shown in the succeeding section.

- **Radiation tolerance**: according to [21], the innermost region of the NSW (R = 1 m) is estimated to be exposed in a radiation environment with 460 Gy of total ionizing dose (TID), 2.3×10^{13} cm^{-2} fast neutron and 4.2×10^{12} cm^{-2} proton fluences (no safety factors included) integrated over 10 years of LHC operation at L = 5×10^{34} cm^{-2} s^{-1}. All NSW ASICs on the sTGC FEBs have been implemented with the 130 nm IBM CMOS process with triple module redundancy protection over the running logic. They have been certified with no issues to survive the TID and cope with the non-ionizing energy loss (NIEL) and single event effect (SEE) at the NSW specified level [25]–[27]. The on-board FEAST and GBT-SCA ASICs are certified at CERN with radiation levels far beyond the NSW requirement.

  The sTGC FEB design has limited to use the minimum number of COTS. Only a 1:4 fanout chip and a precision programmable voltage reference, Texas Instrument TL431, are used for the sFEB in the trigger circuit. For the fanout chip, it is not expected to be sensitive to the single event upset (SEU) as it carries no logic. On the other hand, its use in the trigger path to broadcast the pad trigger data to strip-TDS would not be affected by occasional SEU as the strip-TDS does not rely on the data been transmitted to establish a constant link. For the same reason, the TL431 chip used to provide the 2.5 V to the fanout chip is not necessarily needed for a stringent SEU tolerance. Therefore, the FEB radiation tolerance is automatically satisfied, provided this TL431 chip could survive the expected TID at the NSW. To reassure, the TL431 chip is tested at the Heavy Ion Research Facility in Lanzhou, China using the tantalum beam with the maximum energy of about 1.3 GeV. The test setup and the TID results are shown in figure 8. The top plastic package covering the die was removed

for the radiation exposure. Test results of two randomly selected TL431 chips show that the variation of the output voltage is only about 1‰ during the 90-minute test with a calculated TID of 522 Gy (Si). No SEU event, triggered as a spur of 5% deviation from the nominal voltage, was detected.
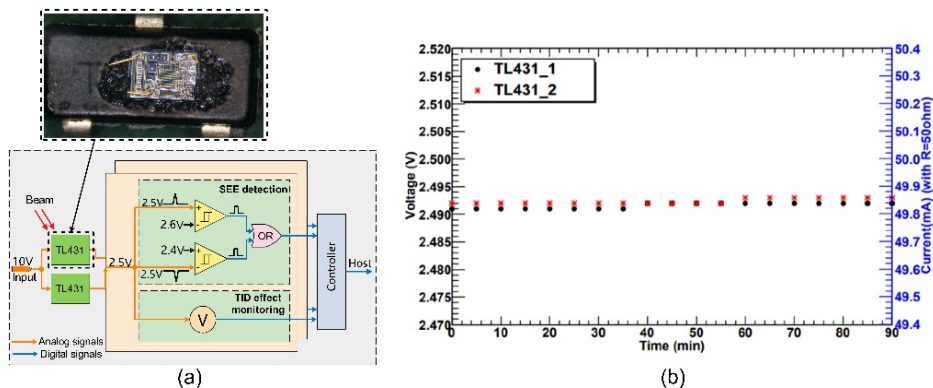

Figure 8. TL431 radiation test setup (a) and TID validation results (b).

- **Front-End analog input circuits**: the introduction of additional discrete components on FEBs as part of the analog circuit is a necessity for the VMM Front-End ASIC to protect the sensitive VMM charge amplifiers from damages caused by the electrostatic discharge in the harsh radiation environment. Additionally, the VMM ASIC requires a special external input circuit to handle sTGC-specific induced signals. The fully customized analog input circuits for sTGC wires, pads, and strips readout are shown in figure 9.

  The ESD protection circuit for each VMM channel is composed of a pair of back-to-back diodes near VMM input pins, a $10\,\Omega$ current limiting resistor connected in series, and a transient voltage suppressing (TVS) diode connected in parallel to the input line. This redundant implementation is deemed essential to adequately protect the VMM which is implemented on the IBM 130 nm CMOS technology, known to have much thinner oxides and thus higher vulnerability to voltage transients comparing with the previous generation ASIC used in the high energy physics experiments. To promptly dissipate the energy from potential discharges generated by the sTGC detector or any space charge accumulation in the high-rate radiation environment, the TVS diode, chosen with a clamp-up voltage of 8.5 V, provides the first stage protection by absorbing up to tens of amperes of instantaneous current of both polarities. The serial resistor and the back-to-back diodes are set to further limit the discharge current and the transient voltage in the range from $-0.7\,\text{V}$ to 1.9 V in most cases. This adopted ESD protection scheme has been developed and experimentally tested against tens of thousands of emulated discharges with both the NSW sTGC and Micromegas detector system [28, 29].

  The sTGC detector is operated with a high gas gain. The exposure of sTGC in the NSW environment with a dominant photon background means the VMM Front-End is subject to the excessive exertion of high induced charge (more than 10 pC) and a high rate. Furthermore, the induced current signals from the sTGC detector have long ion tails [30] which are out of the desired charge integration window of 25–50 ns but carry large portions of the total

induced charge. All these features result in the addition of compensative circuit named as "pull-up" or "π-network" schemes, to keep the VMM amplifier in the safe linear region (up to 2 pC) and reduce its deadtime at high rate operation or due to deep saturation after a high charge event. The pull-up scheme, providing a mild compensation current to correct the bias current and working node inside the VMM, is designed for the sTGC strip readout. A pull-up resistance of 400 kΩ has been determined and used in the final system after a study at the CERN GIF++ facility confirmed its effectiveness for the sTGC high rate operation [31, 32]. For the sTGC pads and wires, the "π-network" scheme is needed. By connecting a small capacitance C_π of a few hundred pF in series with the much larger pad capacitances C_p of up to 3 nF, this effectively attenuates the charge current by approximately $C_\pi/(C_p + C_\pi)$. Ideally, the C_π would be customized for each pad with a different capacitance to maintain a relatively close attenuation factor. Since majority pads on the same quadruplet have similar sizes and it is not practical to implement dozens of different FEBs with completely different parameters, the final system chooses to implement a balanced solution by only making three types of pFEBs, one type for each of the three sTGC quadruplets within a wedge. Since these Front-End networks and the ESD protection components have significantly increased the total component count and the density on board, both small form-factor (0.6 mm × 0.3 mm, 0201 package) surface mount devices (SMD) and integrated multi-channel ESD protective diodes are incorporated on the FEBs at large quantities for the first time in the ATLAS muon detector system.
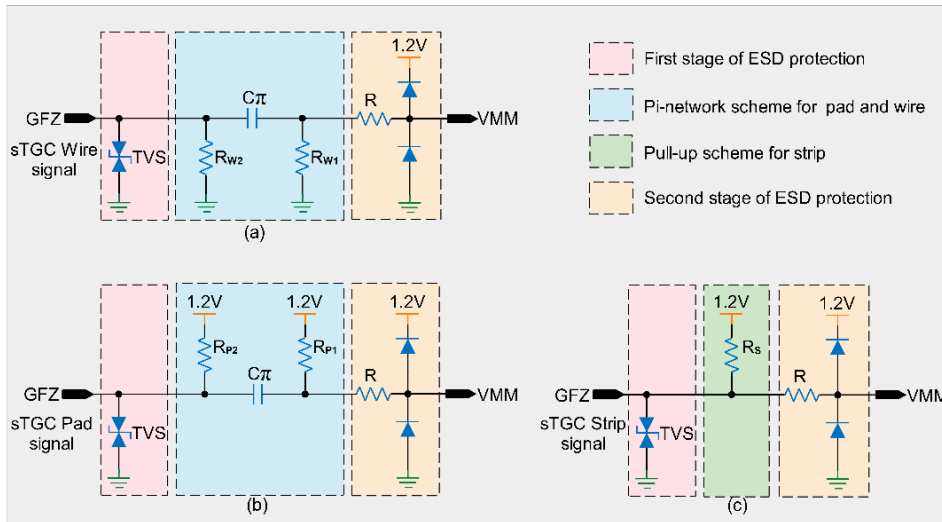

Figure 9. The sTGC FEB analog input circuit which incorporates the ESD protection and the special compensative scheme for VMM to handle the sTGC high rate and high charge signals.

- **Digital circuitry**: although digital functionalities have already been implemented inside the NSW ASICs on board, notable attention is still needed at the board level. For instance, 64 channels of VMM with 320 Mbps 6-bit ADC output are connected to the strip-TDS sharing the common 160 MHz clock. Therefore, trace delay differences among channels are required to be controlled well within 200 ps for the correct and simultaneous sampling of all channels

by the TDS ASIC. In addition, the 4.8 Gbps transmission lines from the TDS are required to retain good signal integrity. This is addressed by running all these high-speed differential traces over the top or bottom of the PCB and avoid the use of stub vias, despite very tight space constraint on board and the complex routing. Finally, all digital signal traces, including clock lines, are kept from the analog traces or ground planes with at least 5 times the gap between the two lines of a differential pair, to avoid cross-talking and aggregation to the sensitive analogy circuit. The FEBs are fabricated with a controlled impedance of $100\,\Omega$ for all the differential lines of digital interfaces.

The full assembled pFEB and sFEB of the final production version are shown in figure 10. Corresponding layer stacks are depicted in figure 11. In total, there are 12 and 14 layers used for the pFEB and sFEB, respectively. To avoid digital noise coupling into the analog part of the circuitry, a separation between analog and digital grounds, as well as different power planes are clearly visible from the illustration. Moreover, the analog and digital ground planes are arranged on separate layers with no overlapping when they are projected vertically on the PCB to the neighboring layer. This also allows analog and digital signals to take their corresponding ground references with the minimum impedance for their return paths. All these implementations deem to be imperative for the low noise required imposed on the detector and electronics system. The summary of the design and implementation requirements for the sTGC FEBs as well as key Front-End operational parameters for the sTGC detector system are given in table 2.
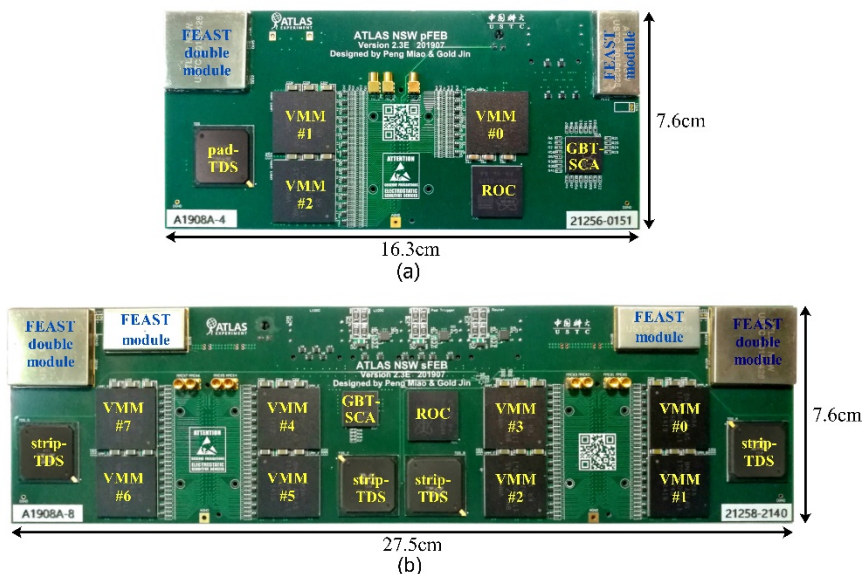

Figure 10. The fully assembled production version of sTGC pFEB and sFEB.

4 Performance characterization

The characterization of the sTGC FEB performance is based on the evaluation of their power, thermal and noise behaviors on the bench, extensive integration tests, and studies with full-size production
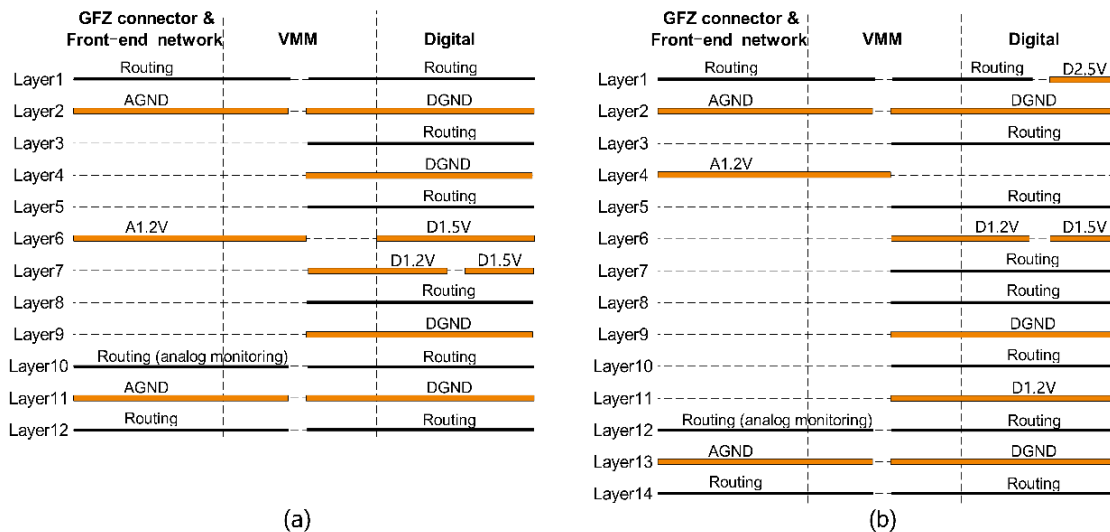
Figure 11. The sTGC pFEB (a) and sFEB (b) PCB layer stack.

sTGC quadruplets and full sTGC electronics chain over several years during the development phase. A summary of the key performance results is detailed in the following sub-sections.

4.1 Thermal performance and powering

The thermal profiles of sTGC FEBs are first studied to precisely locate the hot spots as well as to understand how the heat is dissipated on the board. Thermal images of sTGC FEBs after full configuration and with full power consumption are shown in figure 12. Note that they are taken from the top side of the FEBs without the cooling plates when FEBs are cooled by the 150 CFM airflow at the 22°C ambient temperature. Hotspots created by the VMM and TDS dies are easily visible. One could tell the distinguished VMM die from its rectangular shape and the large size. The hottest point only shows around 50°C at the given condition before active water cooling is applied. The FEAST modules shown as a dark color with low temperatures are due to the infrared-reflective metal shields. Therefore, they have been verified with a thermal couple attached to the shield to be less than 50°C. Areas not occupied by the ASICs show a relatively even low-temperature distribution. No major issues are identified.

A further thermal validation is done by monitoring the VMM temperature with its embedded temperature monitoring circuit when the cooling plates are mounted on the FEBs and the water cooling is applied. One example results for eight VMMs from one sFEB monitored over a day are shown in figure 13. All VMM temperatures are less than 33°C, well below the required upper limit. The zig-zag trend of the temperate change by a few degrees is due to the activation and periodic cycling of the chiller to regulate the water temperature to 17°C. The VMM following the water temperate change confirms a small thermal resistance between the ASIC die and the cooling plate interface.

The reliability of the FEB operated at full power is also evaluated by monitoring the current stability. Figure 14 shows the current from FEBs mounted on four layers of an sTGC wedge. Each curve represents the sTGC layer with 3 pFEBs and 3 sFEBs. One could note that currents remain

Table 2. The summary of sTGC Front-End electronics design parameters.

Front-end analog	Channel density	512 (sFEB), 192 (pFEB)
	VMM gain	1–3 mV/fC
	VMM peaking time	25 or 50 ns
	VMM C_π in the π-network scheme for pad readout at high rate	200 pF (QS1, QL1) 330 pF (QS2, QL2) 470 pF (QS3, QL3)
	VMM $R_{pull-up}$ in the pull-up scheme for strip readout at high rate	400 kΩ
Digital	Maximum trigger rate	1 MHz
	Trigger chain data rate	4×4.8 Gbps (sFEB); 1×4.8 Gbps (pFEB)
	Readout chain data rate	<2560 Mbps (sFEB); <1280 Mbps (pFEB)
	Monitoring	Baseline, threshold, temperature
Power	Power supply voltage	10 V
	Power consumption	21 W (sFEB); 9 W (pFEB)
Board dimensions	Board length	27.5 cm (sFEB); 16.3 cm (pFEB)
	Board width	7.6 cm
	Max height on active device side	3 mm
	Board layer count	14 (sFEB); 12 (pFEB)
	Total component count	2470 (sFEB); 1356 (pFEB)
Operational environment	Radiation background	Up to 50 kRad TID (safety factor not included)
	Magnetic field	Up to 0.5 T
	Cooling requirement	<50°C
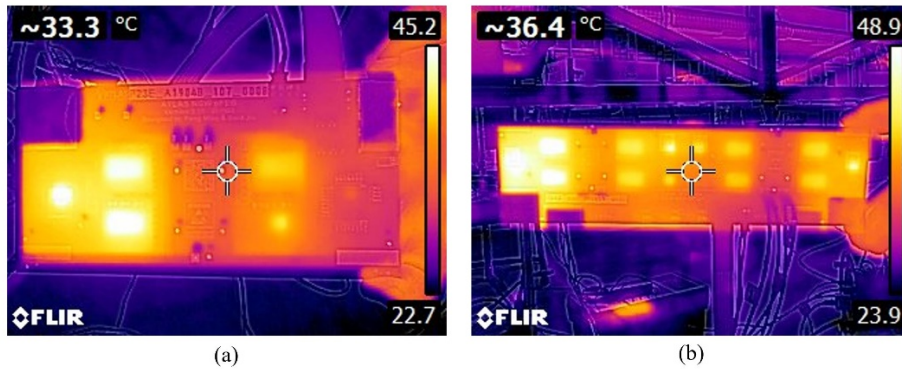
Figure 12. Thermal images of pFEB (a) and sFEB (b) showing hot spots on boards.
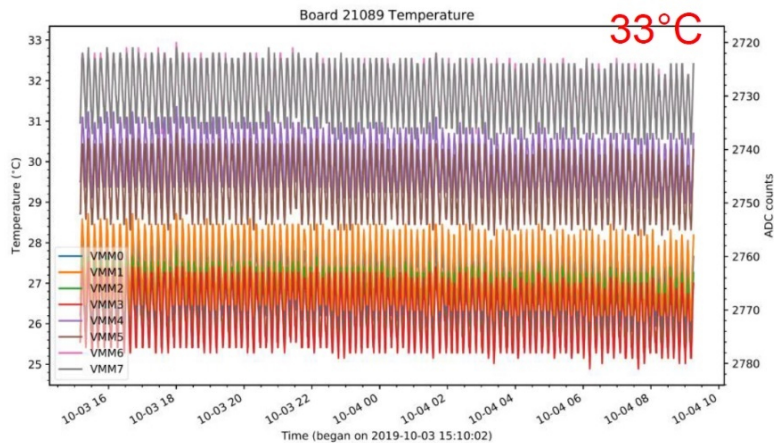
Figure 13. The Monitored VMM temperature of the sFEB operated with full power consumption and the water cooling (17°C water at a flow rate of 0.5 L/min).

stable within a two-hour time window. It is important to point out that the current is very sensitive to the change of the water temperature, as seen in the trend of figure 14 which resembles that in figure 13. This current-temperature correlation could be utilized in the final detector slow control system to monitor and diagnose the healthiness of the Front-End electronics in real-time.
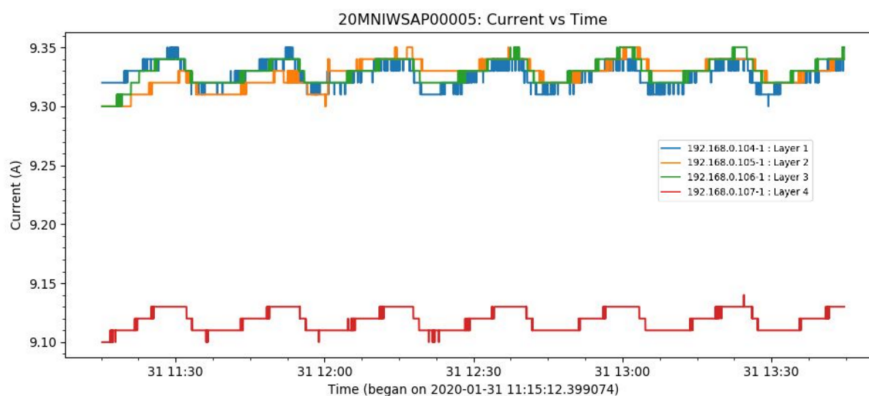
Figure 14. The monitored total FEB current from four layers of a sTGC wedge.

4.2 VMM baseline measurements

The nominal VMM baseline is 160 mV and the dispersion among channels within a VMM is expected to be smaller than 40 mV. It is a key parameter that indicates the correct functioning of the dedicated multi-staged amplifiers and their associated baseline restoration circuit. The introduction of an additional pull-up scheme to the input of the VMM, depending on the pull-up resistance and thus the pull-up strength, could result in the drift of the baseline to a much higher value at a VMM gain of 3 mV/fC. Besides the possible increase of the baseline spread among channels, the pull-up scheme also effectively invites inter-strip channel coupling to some extent. The effect could also be amplified if any unwanted short occurs due to the proximity of tiny SMD components at high

density. Given these concerns, a full scan of VMM baselines with the selected pull-up resistance is carried out on ten preproduction sFEBs. An example of the scan result is given in figure 15(a). All 512 VMM channels per sFEB show stable and nominal baseline with several combinations of peaking time and gain. The statistical summary of the channel baseline variation from one representative VMM is also shown in figure 15(b). The standard deviation of the baseline is only around 3 mV.
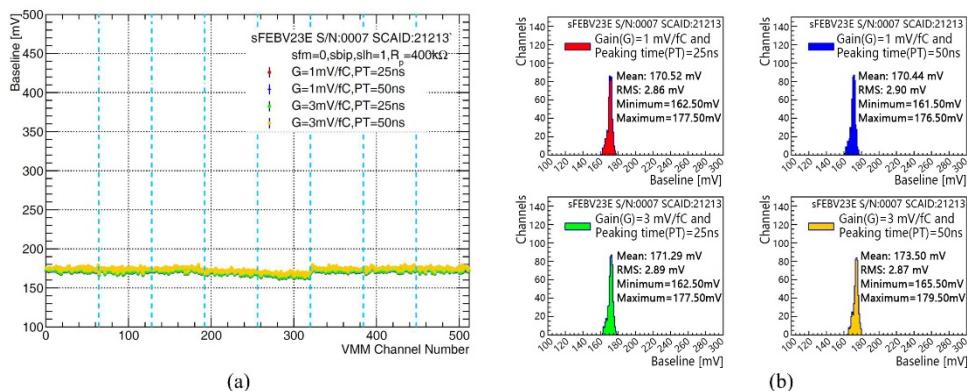

Figure 15. The typical channel baseline of the sFEB.

4.3 Noise performance and FEB-detector integration

The signal to noise ratio is of fundamental importance to the position-sensing and timing in a gaseous detector with readout strips. While the signal amplitude is mainly determined by the detector gas gain as well as a set of predefined amplifier parameters, such as the sensitivity and the integration time, the noise could originate from various sources. Practically, the major contribution as well as the major uncertainty of the noise from a large-scale gaseous detector system, besides the inherent thermal noise, are from the external sources coupled to the Front-End circuit via ground loops or electromagnetic interferences (EMI). As related to the sTGC FEBs, characterization of the noise performances is done with the analysis of the noise fast Fourier transformation (FFT) and the measurements of noise amplitude, both on and off the detector.

The typical noise FFT spectra from the VMM channels with the pFEB and sFEB on the bench without the external capacitive input are shown in figure 16. The VMM sensitivity is set at 3 mV/fC and 1 mV/fC for pad and strip VMMs while the peaking time is kept at 50 ns which is the default setting to be used by the final system. No notable coupling of the 2 MHz FEAST switching noise is observed, contrary to measurements on early FEB prototypes, which displayed clear narrow noise peaks at frequencies associated to the FEAST noise irradiation. As further confirmation, noise was measured using an independent low noise power scheme with all FEAST in the FEB disconnected, resulting in values compatible within 10%. This indicates a very promising implementation of the FEB layout to confine the switching current from the FEAST modules, as otherwise the switching noise would be clearly visible from those analog input circuits connected to the 1.2 V FEAST module.

A further study by measuring the noise amplitude of an sFEB VMM channel with a capacitive load has been carried out to emulate the noise condition with the detector connected. The setup with a surface mount capacitor directly soldered to the GFZ pins on the sFEB could be viewed in figure 17(a). Since the most interesting range of the input capacitance for the sTGC is about 100 pF to 1000 pF, a few capacitors of different values have been mounted to the sFEB. The measurements observe the VMM baseline fluctuation within a 20 µs window using an oscilloscope connected to the VMM analog monitor output. The measured noise amplitude is translated into the equivalent noise charge (ENC) and results are shown in figure 17(b) together with simulated numbers extracted from [8] for comparison. In general, measurements are in a good agreement with the simulated results. Slight differences could stem from the poorer accuracy of the oscilloscope to measure very small amplitudes and deviations of capacitance from the rated one at a large value. It is important to note that the simulated ENC from early studies do not include the pull-up scheme whereas the measurements do. The almost same noise level between the two suggests the contribution of the pull-up resistor to the thermal noise is negligible and further convinces of the feasibility of the introduced analog input circuit.
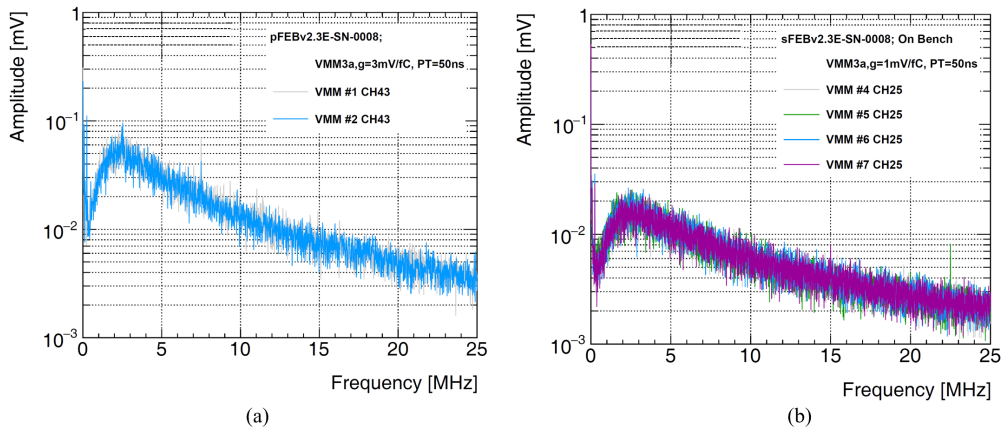

Figure 16. The typical noise FFT spectra for pFEB (a) and sFEB (b) VMM channels.

The study of the Front-End noise on-detector is performed with four pFEBs and four sFEBs installed on a full-size production sTGC quadruplet (named as QL1 for the NSW), which houses the largest number of pads and strips among all sTGC types. Results for the pads are shown in figure 18(a). A reasonably uniform noise level at an ENC of 3000 electrons are observed at a gain of 3 mV/fC and a peaking time of 50 ns, regardless of the pad capacitances when 100 pF is used in the π-network. This insensitivity is as expected and essentially due to the actual capacitances "seen" by the VMM is the same C_π. Given the short peaking time to be used for triggering at the final system, this noise level would be excellent to yield a signal to noise ratio of greater than 50 for sTGC pads when the detector is operated with the nominal high voltage of 2.8 kV. It must be noted that this is already a great achievement as the low noise levels are maintained over an entire detector with more than 400 pads and a surface area of about 9 m^2.

The full scan of the noise level from more than 2000 strip channels with the sFEBs are shown in figure 18(b). The average ENC for the about 1 m length strip is around 5000 electrons. The trend
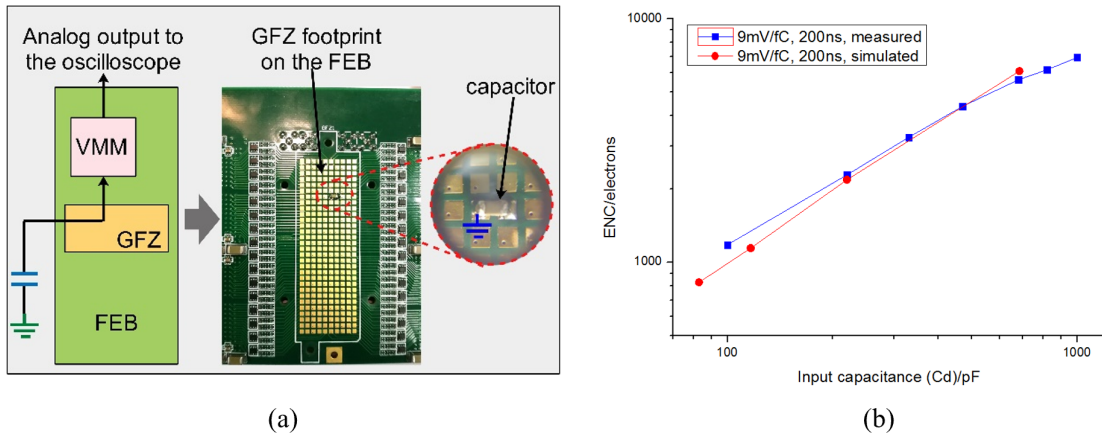
(a)   (b)

Figure 17. The setup of sFEB VMM noise measurements with simulated detector capacitance on the bench (a) and the ENC as a function of VMM input capacitance (b).
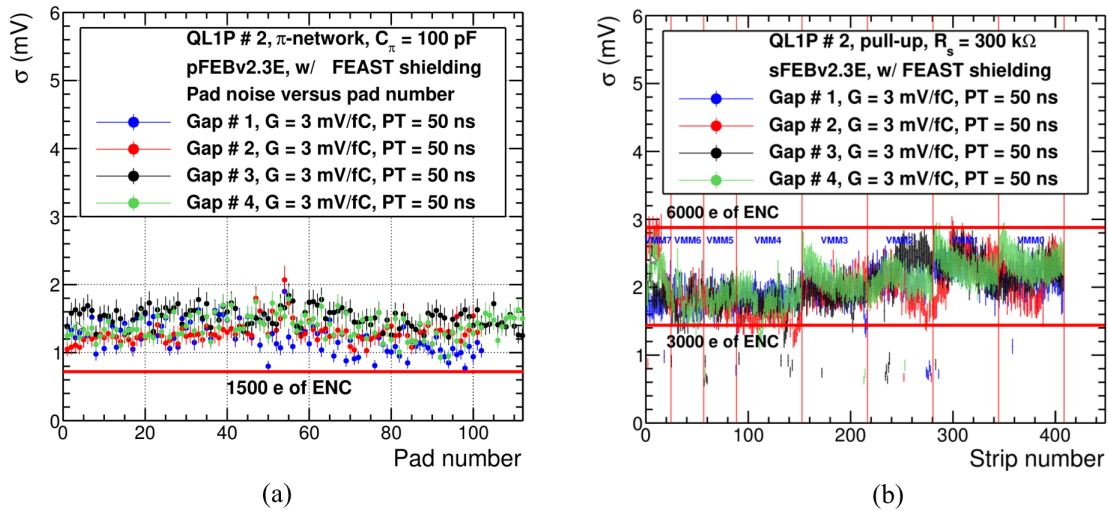

(a)   (b)

Figure 18. The noise measured from pads (a) and strips (b) of the sTGC quadruplet.

of noise increase with the strip number and hence the strip length is loosely visible despite some local variations. This observation triggers a further investigation with the analysis of the noise FFT from those channels. The outcome is that those channels are affected by the external noise pick-up, which is conductively coupled to the entire detector but with unknown reasons of coupling strength difference at different locations. This is especially true for the lower number strips in gap 2 and 4 with much larger than expected noise level, as those strips on the cathode are soldered to the adapter board with long floating jumper wires in absence of companion ground connections nearby. Nevertheless, the noise results obtained are the best achievable over the entire detector surface. No FEAST pick-up noise is found, which suggests the effectiveness of the dedicated FEAST placement trying to avoid the noise irradiated from the FEAST being coupled to the sTGC signal adapter boards. It should be pointed out that the noise results reflect the performance at the system level
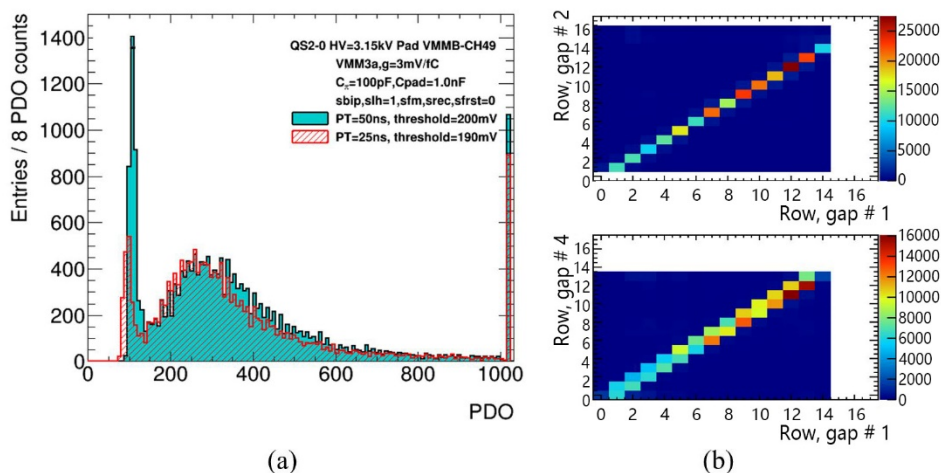
Figure 19. The muon charge spectrum obtained from the pFEB in the readout chain (a) and the cosmic ray hit correlation from pad rows in two sets of layer combination (b).

and could be affected by many other sources of uncertainty. The most important findings, however, are the scalability of the system where the noise does not increase as a function of number of FEBs mounted, and the minimum contribution of the noise from the sTGC FEBs themselves or their on-board chips.

The FEB-detector integration studies are completed with lab and beam tests with several types of sTGC quadruplets to demonstrate the FEB readout and trigger functionalities. A mini-DAQ system have been developed by the NSW collaborators to emulate the Back-End electronics for slow control and data collection from sTGC FEBs. A set of example results are given in figure 19. Figure 19(a) shows the charge spectrum from muons taken by the pFEB. The Peak Detector Output (PDO) is the charge measurement result given by the VMM and the unit is mV. The Landau peak and the noise pedestal are easily disguisable. Validation in the trigger path could be seen in figure 19(b) as the successful readout of pad hits via the VMM-TDS pair. Correlations of cosmic ray hit between two pad rows from two different sets of layer combinations are apparent. In all cases, the synchronization among multiple sTGC FEBs are achieved. Many more detailed detector performance studies are to be presented elsewhere.

4.4 FEB integration with full chain electronics

Both pFEB and sFEB during the development phase must be tested with all remaining NSW electronics to validate the compatibility of their physical and electrical interfaces, running protocols with other boards. The stability of data transmission when operated in the framework of the whole system also needs to be verified. For these purposes, the pFEBs and sFEBs, in the production version, as well as a few early prototypes, have participated in several full chain electronics integration campaigns at CERN. Figure 20(a) shows a photo taken during the integration week when a pair of pFEB and sFEB were connected to the Pad Trigger Board, the sTGC L1DDC, and the sTGC Router. A few compatibility issues on the mini-SAS pin definition between different boards, and several
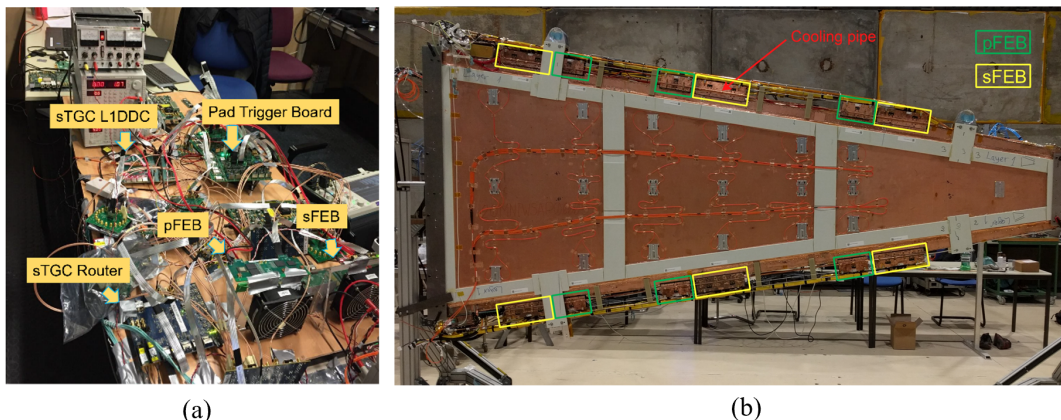
Figure 20. The sTGC full chain electronics integration setup (a) and a fully assembled production sTGC wedge with 12 pFEBs and 12 sFEBs mounted (b).

ASIC to ASIC communication protocols were observed. Identified issues have been resolved by the development of workarounds in the Back-End software and firmware or a slight modification to the production version hardware design.

The system-level integration test for sTGC FEBs also covers the validation of crucial trigger chain data links operated at 4.8 Gbps with the final clock distribution, jitter quality, and the cable length. The full sTGC trigger path with pad-strip coincidence has been successfully demonstrated with the emulated tested pulse patterns. Both pFEB and sFEB have been checked to fulfill the system level requirements on the 4.8 Gbps data transmission via the Twinax cable with a maximum length of six meters when the repeater planned for the final system to relay and the high-speed signal is connected along the Twinax cable path.

The pFEBs and sFEBs have also been mounted with the full-size production sTGC wedge, as shown in figure 20(b). They have been verified to be compatible with the on-wedge low voltage and cooling services. The readout and synchronization of test pulse patterns with all 12 pFEBs and 12 sFEBs on an sTGC wedge have been demonstrated with the FELIX system. More stress testing of the entire NSW readout system with sTGC FEBs at 1 MHz trigger rate is ongoing at CERN.

5   Conclusions

The ATLAS NSW upgrade is a major project to replace the entire innermost station in the forward region of the ATLAS Muon Spectrometer, aiming to enhance its hardware-based Level-1 trigger while maintaining its excellent tracking capability towards high-luminosity LHC runs. The sTGC with more than 400'000 readout channels will serve as the NSW primary trigger detector. In this paper, we presented the design and implementation of the sTGC FEBs. The sTGC FEBs are responsible for the detection of analog signals from the detector and drive the Level-1 readout and the trigger data off the detector with high-speed links up to 4.8 Gbps. They mainly host several NSW-specific ASICs such as VMM, TDS, and ROC. The high demand to accommodate up to 512 analog channels with a dense input network in a very constrained space, minimize the conducted and irradiated noise from the onboard switching regulators and digital ASICs, and handle a large

number of high-speed inter-connects among highly integrated ASICs, all bring orders of magnitude complexity as well as great challenges to the design comparing with the previous generation FEBs used in similar experiments. Moreover, special care is needed for the FEBs to deal with the harsh radiation and the magnet field environments at the same time. Detailed analysis and strategic discussions on how these challenges have been addressed are presented.

The characterizations on the key performances of the production version sTGC pFEB and sFEB show that both types of the FEB meet all design requirements. With the final water cooling, all on-board ASICs are well below the safe temperature set at 50°C when pFEBs an sFEBs are operated at full power consumption of 9 W and 21 W, respectively. The noise study on the bench shows negligible levels of noise coupling from the FEAST DC-DC converters to the sensitive VMM analog circuit. Integration studies with the full-size sTGC quadruplets indicate no noticeable noise coupling from the digital circuit. The pick-up noise from the detector due to the FEAST switching current irradiation has been minimized to a negligible level thanks to the attentive layout and the effective shielding of the FEAST modules. All digital communications on and off FEBs have been verified with the full sTGC electronics chain test. More than 1500 sTGC FEBs are now in series production and the results on mass production will be communicated in a succeeding paper.

Acknowledgments

References

[1] L. Rossi, *LHC Upgrade Plans: Options and Strategy*, CERN-ATS-2011-257 (2011).

[2] https://hilumilhc.web.cern.ch/content/hl-lhc-project.

[3] T. Kawamoto et al., *New Small Wheel Technical Design Report*, CERN-LHCC-2013-006 (2013) [ATLAS-TDR-020].

[4] R. Hauser, *The ATLAS trigger system*, *Eur. Phys. J. C* **34** (2004) s173.

[5] ATLAS MUON collaboration, *Trigger algorithms and electronics for the ATLAS muon new small wheel upgrade*, 2016 *JINST* **11** C01083.

[6] I. Ravinovich, *The New Small Wheel background rates predictions based on CSC and 2 TGC Run-2 measurements*, ATL-COM-MUON-2016-006 (2016).

[7] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2017-020 (2017) [ATLAS-TDR-029].

[8] G. De Geronimo et al., *VMM1 — An ASIC for Micropattern Detectors*, *IEEE Trans. Nucl. Sci.* **60** (2013) 2314.

[9] R.M. Coliban et al., *The Read Out Controller for the ATLAS New Small Wheel*, 2016 *JINST* **11** C02069.

[10] J. Wang et al., *Characterization of a Serializer ASIC chip for the upgrade of the ATLAS muon detector*, *IEEE Trans. Nucl. Sci.* **62** (2015) 3242 [arXiv:1509.06636].

[11] J. Wang, L. Guan, J.W. Chapman, B. Zhou and J. Zhu, *Design of a Trigger Data Serializer ASIC for the Upgrade of the ATLAS Forward Muon Spectrometer*, *IEEE Trans. Nucl. Sci.* **64** (2017) 2958 [arXiv:1707.05451].

[12] P. Gkountoumis, *Level-1 Data Driver Card of the ATLAS New Small Wheel upgrade compatible with the Phase II 1 MHz readout scheme*, in proceedings of the *5th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Thessaloniki, Greece, 12–14 May 2016, pp. 1–4.

[13] W. Wu, *FELIX: the New Detector Interface for the ATLAS Experiment*, *IEEE Trans. Nucl. Sci.* **66** (2019) 986 [arXiv:1806.10667].

[14] P. Moreira et al., *The GBT Project*, in proceedings of the *Topical Workshop on Electronics for Particle Physics (TWEPP09)*, Paris, France, 21–25 September 2009, pp. 342–346.

[15] V. Izzo, S. Perrella and R. Vari, *NSW Electronics Preliminary Design Review. Pad Trigger Logic Board*, talk given at CERN, Geneva, Switzerland, 10 February 2015 and online pdf version at https://indico.cern.ch/event/354058/contributions/832505/attachments/701568/963203/PadTriggerLogicBoard.pdf.

[16] J. Wang et al., *Fixed-latency gigabit serial links in a Xilinx FPGA for the upgrade of the muon spectrometer at the ATLAS experiment*, *IEEE Trans. Nucl. Sci.* **65** (2018) 656.

[17] G. Iakovidis, *VMM3, an ASIC for Micropattern Detectors*, ATL-MUON-PROC-2018-003 (2018).

[18] A. Caratelli et al., *The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments*, 2015 *JINST* **10** C03034.

[19] T. Alexopoulos et al., *Upgrading the New Small Wheel readout to handle a 1 MHz readout rate*, ATL-COM-MUON-2016-026 (2016).

[20] http://suddendocs.samtec.com/catalog_english/gfz.pdf.

[21] J. Ameel, D. Amidei, K. Edgar and L. Guan, *New Small Wheel Radiation and Magnetic Field Environment*, internal communication.

[22] ATLAS collaboration, *Radiation-hard power electronics for the ATLAS New Small Wheel*, 2015 *JINST* **10** C01009.

[23] S. Michelis et al., *DC-DC converters in* 0.35 μ*m CMOS technology*, 2012 *JINST* **7** C01072.

[24] CERN FEAST DC-DC converter, (2020) https://project-dcdc.web.cern.ch/.

[25] F. Faccio and G. Cervelli, *Radiation-induced edge effects in deep submicron CMOS transistors*, *IEEE Trans. Nucl. Sci.* **52** (2005) 2413.

[26] G. Iakovidis, *VMM3a, an ASIC for tracking detectors*, ATL-MUON-PROC-2019-009 (2019).

[27] Ș. Popa, *Readout Controller (ROC) Radiation Testing Report*, internal communication.

[28] V. Polychronakos, *ESD Studies*, internal communication.

[29] P. Gkountoumis, *Prototype board development for the validation of the VMM ASICs for the new small wheel ATLAS upgrade project*, in proceedings of the *2018 7th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, Thessaloniki, Greece, 7–9 May 2018, pp. 1–4.

[30] ATLAS collaboration, *Simulation Studies of Characteristics and Performance of small-strip Thin Gap Chamber for the ATLAS New Small Wheel Upgrade*, ATL-MUON-PUB-2014-001 (2014).

[31] GIF++ collaboration, *CERN-GIF++: a new irradiation facility to test large-area particle detectors for the high-luminosity LHC program*, in proceedings of the *3rd International Conference on Technology andInstrumentation in Particle Physics (TIPP'14)*, Beurs van Berlage, Amsterdam, The Netherlands, 2–6 June 2014.

[32] https://ep-dep-dt.web.cern.ch/irradiation-facilities/gif.