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Gating of charge sensitive preamplifiers for the use at pulsed radiation sources

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ABSTRACT

The development of a switch circuit to gate charge sensitive preamplifiers for use at pulsed radiation sources will be presented. This development was used for the $^{16}O(n,\alpha)^{13}C$ reaction measurement with a Double Frisch Grid Ionization Chamber (DFGIC) at the neutron time-of-flight facility CERN n_TOF in Geneva, Switzerland. Intense instantaneous radiation which is produced in the spallation target of the n_TOF facility (γ-flash) can saturate charge sensitive preamplifiers and prevent signals from being registered in the detection system. The switch circuit made it possible for the first time to perform a measurement with the DFGIC with γ-flash gated off at n_TOF. Nano-second gating of charge sensitive preamplifiers has a wide range of applicability at pulsed radiation sources, where short bursts of radiation must be gated off to avoid saturation, e.g. with HPGe detectors for γ-ray detection. Nano-second gating requires the stray-capacitance of the wideband reflective switch to be compensated to avoid a strong signal during the switch operation. Spectral analysis of the switch circuit shows that additional noise is insignificant.

1. Introduction

The n_TOF facility at CERN [1] uses the CERN PS proton beam ($7 \cdot 10^{12}$ protons per pulse with an energy of 20 GeV) to produce an intense burst of neutrons by spallation in a large lead target. The neutron energy is determined using the time-of-flight method. There are two measurement stations at 20 m and 185 m from the neutron-production target, referred to as EAR2 and EAR1, respectively. The main purpose is to measure neutron-induced reaction cross sections of relevance to science and technology, e.g. neutron capture for nucleosynthesis or neutron-induced fission for nuclear safety [2]. While charged particles are deflected out of the neutron beam using a magnet, γ-rays coming mainly from the in-flight decay of neutral pions, reaching energies up to GeV, can fly up to EAR1 which is at an angle of 10 degrees relative to the proton beam. This generates a prompt flash made of the scattered photons and of the created charged leptons on the window materials of the neutron beam pipe, the so-called γ-flash. This prompt γ-flash can create – depending on the detector – such an amount of charge that the preamplifier electronics are saturated. Especially detectors using charge sensitive preamplifiers (CSP) with high gain suffer from that effect. In EAR2 this prompt flash is not visible because the decay of pions is forward focused due to their relativistic velocity, but a delayed and wider flash is present made of the very intense flux of fast neutrons which produce a piled up signal when they scatter in the sample and detectors. This neutron-flash is also harmful when studying reactions above 1 MeV, but it can also be mitigated with the switch electronics, although to a lesser extent due its wider time spread.

In November 2017 the first detector test using a prototype Double Frisch-Grid Ionization Chamber (DFGIC), has been performed at n_TOF in EAR1 in order to measure the $^{16}O(n,\alpha)^{13}C$ cross-section. The detector was placed directly in the neutron beam. An outcome was that a measurement of MeV neutron-induced reactions was not possible with this detector, even with minimizing the amount of material in the beam. Connecting directly the detector signals to the acquisition system without any amplification, we measured the electric charge pulse induced by the γ-flash which is about three to four orders of magnitude higher than the ionization induced by α-particles [3] in the counting gas. This problem led to the idea to ground the detector

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[2] https://www.cern.ch/ntof.

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during the γ-flash time window and gate off the preamplifier. A switch circuit is inserted between the detector and the preamplifier, in order to drain the charges and isolate the preamplifier while the γ-flash passes through the detector. Switch circuits capable of ns-gating of charge sensitive preamplifiers were developed in a common work at HZDR and CERN and tested in in-beam measurements with DFGICs at n_TOF. The charge induced by the γ-flash was successfully drained to ground and the CSP were not saturated anymore. The ns-gating switch circuit presented in this paper allows to operate charge sensitive preamplifiers at pulsed radiation sources without saturation due to extreme instantaneous intensity. The transient charges while switching the connection are compensated effectively. In this sense the switch circuit solves the problem where transistor reset preamplifier [4–6] and optical feedback techniques [5] used e.g. for high resolution gamma-ray spectroscopy fail to do it [7].

2. Development of the switch circuit

The features which have to be implemented are the following: during the γ-flash the preamplifier should be disconnected from the detector, and the latter should be connected to the ground to drain the charges deposited by the γ-flash. The input of the preamplifier should remain open ended, and not grounded, to prevent a huge noise at the output during this gate off time window. After the flash the switch is gated on, the detector is isolated from the ground and connected to the preamplifier. Therefore the circuit should be based on two elementary switches, the first one connecting the detector to the ground, the other one connecting it to the preamplifier, so that the states of the two switches should be opposite.

2.1. The core chip ADG902

The central component is the wide band reflective switch ADG902 from Analog Device [8] built in complementary metal oxide semiconductors (CMOS) technology. Earlier designs by K. Heidel [9] at HZDR using the absorptive switch ADG901 showed noise transmission due the coupling to ground via the integrated 50 Ω impedance. The working principle of the ADG902 chip is illustrated in Fig. 1. The control voltage G has two logical levels, low and high, in order to control the transmission gates S_1 and S_2 acting as switches. The detector is connected to $RF2$ as input and $RF1$ is used as output to be connected to the preamplifier. The advantage using the chip in that way is demonstrated in Fig. 2:

If the control voltage is set low (typical value is close to 0 V), S_1 is opened and S_2 is closed. In that case the detector is grounded and the CSP is isolated from the detector. That means that the huge unwanted induced amount of charge from the γ-flash in the detector goes directly to ground and cannot reach the CSP. In the following we define this state as ***OFF***.

After the charge collection time of the γ-flash in the detector is over, the control voltage is set high (typical value is close to 2.5 V). In that case S_1 is closed and S_2 is opened which means that the CSP is connected to the detector. This state is defined as ***ON***.

2.2. Compensation circuit

As such the chip does not work satisfactorily due the charges injected into the analog part through the internal gate-channel capacities of the MOSFET pairs when the logic level applied to the gate undergoes sharp transitions as illustrated in Figs. 1 and 2.

For the transition of S_1 from state $OFF \rightarrow ON$ the gate capacitance of S_1 will be charged with the inverted high control voltage during the OFF state, while S_1 is closed. After S_1 opens the most of the charge of the gate capacitance of S_1 will be released to $RF1$, to the preamplifier.

A similar case happens for the transition from state $ON \rightarrow OFF$, where the gate capacitance of S_1 will be charged with the high control

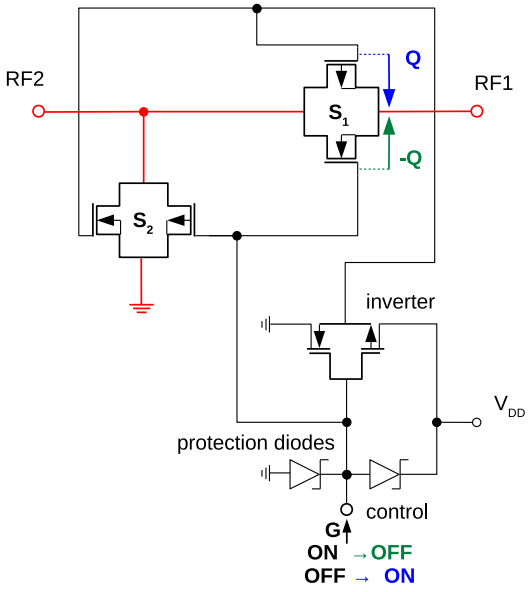


Fig. 1. Scheme of the ADG902 chip. It consists of one CMOS inverter and two transmission gates (S_1 and S_2). In addition, protection diodes are integrated in the circuit before the inverter. $V_{DD} = 2.5\ V$ is the supply voltage of the circuit. The blue and green colors indicate the released charge Q during the transitions. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

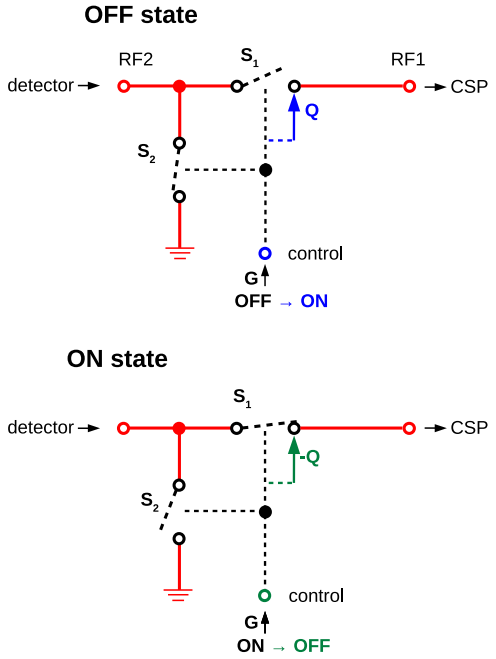


Fig. 2. Block diagram of the ADG902 chip. The upper and lower diagram shows the OFF and ON state, respectively. Furthermore the charges injected to the preamplifier side by the transitions from state OFF to ON and from ON to OFF, respectively are illustrated.

voltage during the ON state. After S_1 closes, most of the charge of the gate capacitance of S_1 will be released again to $RF1$. The amount of charge for both transitions are similar but have different polarities. Considering S_2 for both transitions an equivalent discharge mechanism takes place, whereas the discharge of the gate capacitance goes directly to ground and does not disturb the preamplifier signal.

The actual transition time of the switch when the gate signals changes from state $ON \rightarrow OFF$ or from $OFF \rightarrow ON$, is less than

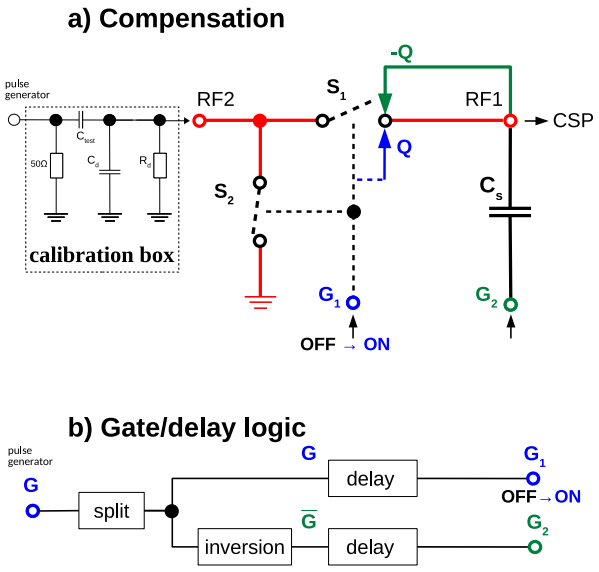


Fig. 3. Scheme of the ADG902 chip during transition with the compensation circuit. (a) contains the compensation circuit using a capacitor C_s=1 pF. The left part contains a calibration box consisting of a pull down resistor R_d=20 MΩ and a capacitor to simulate the (anode-grid) detector capacitance of C_d=80 pF. (b) displays a simplified block diagram of the gate/delay logic consisting of delay units and inverters. The time difference between G_1 and G_2 needs to be adjusted is in the order of tens of ns.

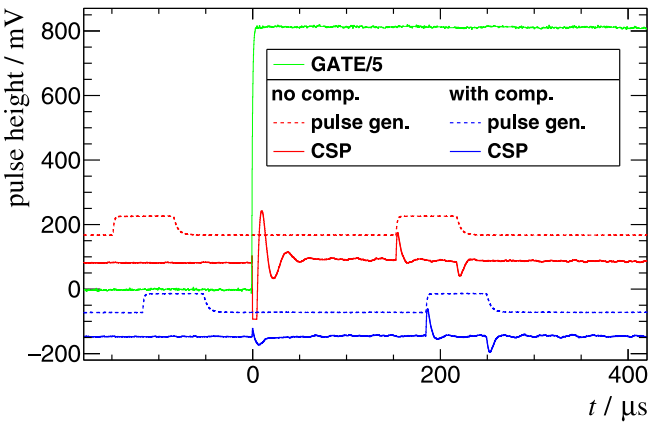


Fig. 4. Wave forms of the pulse generator test of the compensated circuit. The dashed lines are the trapezoidal generated signals which are injected into the calibration box. The corresponding full colored blue and red lines shows the output of the CSP while the compensation on the switch circuit is applied and not applied, respectively. The gate signal is depicted in green. For times t <0 µs the high control voltage and t >0 µs the low control voltage is applied, respectively. At t=0 µs the transition structure of the switch is visible (CSP signals). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

10 ns [8]. However as the internal capacitance of the CMOS components S_1 and S_2 is of the order of 1 pF, the induced charge is of the order of 2 pC, much higher than the physical signals (30 fC), thereby saturating the preamplifier.

The interesting feature is that this induced charge is always the same, as it is produced by transitions of logic levels, therefore it can be compensated by injection of an opposite charge in order to reduce this disturbance or prevent a possible saturation of the CSP.

The solution is to use a capacitor C_s of 1 pF in order to compensate the released charge from S_1. A test setup for the compensated switch is illustrated in Fig. 3(a). C_s needs to be charged with a second gate signal G_2 which is basically the inverted high control voltage $\bar{G}$. Since the capacity C_s is usually different from the real gate-channel capacity of the internal MOSFET, the amplitude of the transition applied to G_2 should be tuned to match the charge injected internally. Also the time delays should be tuned because the original gate signal and its opposite counterpart do not travel through the same chips, so that a shift is introduced by the transit times. This fine tuning of the compensation circuit is schematically represented in Fig. 3(b).

Using a precision pulse generator PB-5 (Berkeley Nucleonics Corp.) trapezoidal signals (rise time=200 ns, flat top=60 µs, fall time=500 ns) with a 500 Hz repetition rate and the logical trigger signals were generated. The rising and falling linear edges of the trapezoidal signals are converted as charge with a terminating low pass (50 Ω and C_d=80 pF) and a differentiating high pass (R_d=20 MΩ and C_{test}=1 pF) which is built into a calibration box as discrete component. This charge signal from the calibration box represents the detector signal of an α-particle with 5 MeV energy, which is expected in a real measurement. As preamplifier an in-house built CSP from HZDR with a time constant of about 2 µs has been tested. All wave forms were recorded with an oscilloscope of type LECROY WaveRunner 8254-MS (2.5 GHzMixed Signal Oscilloscope).

The results of the test with and without compensation are shown in Fig. 4. At 0 µs is the transition from OFF to ON. It can be seen that without any compensation the CSP signal starts to saturate for a few µs. With the optimal adjustment of the compensation circuit (tuned delay and attenuation) the saturation is prevented and only a small residual structure remains. The residual consists of a narrow structure 30 ns wide (FWHM), followed by a smooth exponential tail coming from the response of the CSP to the transient. The time constant of this tail is merely the decay time constant of the CSP. A positive and negative CSP signal is visible corresponding to the falling and rising edge of the pulse generator signal, respectively. Furthermore in the OFF region of the switch circuit where the gate voltage is operated with the low control voltage no CSP signal at the edges of the pulse generator signal is visible which demonstrates that the switch properly isolates the calibration box (detector) from the CSP.

Remarks about the compensation circuit

1. Reduction of the gate voltage:
One naive solution reducing the transition charge could be the reduction of the control high voltage, which is directly proportional to the released transition charge of S_1. The limitation is that the CMOS components working in the ON state are only operational for gate voltages from 1.7 to 2.5 V [8]. That means the transition charge could be only reduced by a factor of 1.5. However, the released charge is about one order of magnitude higher than the expected charges from α-particles.

2. Charge compensation with a second switch:
Also the usage of a second switch instead of C_s was tested in a similar condition, counting on the matching characteristics of the two switches. However the characteristics of the CMOS components are dispersed so that this option would require a selection procedure of ADG902 chips, otherwise a fine tuning of the gate amplitude of the second chip would be needed and the circuitry would become finally more complex than with the single capacitor.

3. Compensation only for transition from state $OFF \rightarrow ON$:
The compensation needs to be mainly focused for the released charge of S_1 for the transition from state $OFF \rightarrow ON$, because this situation is most important for the measurement. The region where signals are acquired is during ON state. When the switch goes in the transition from state $ON \rightarrow OFF$, the discharge appears in the OFF state, where no signals are acquired.

2.3. Coupling of the switch circuit

The coupling of the switch to the preamplifier should be designed in a way that any DC potential mismatch be avoided at the transition

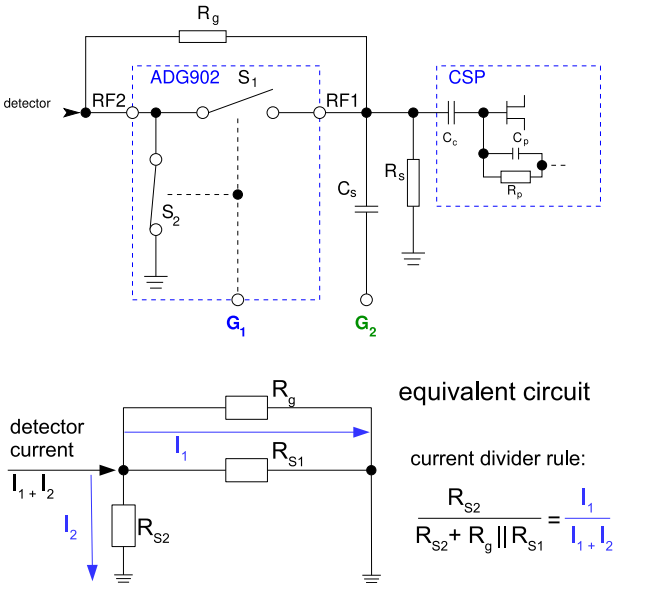


Fig. 5. Scheme of detector-switch-CSP coupling. R_s can be implemented by the HV biasing resistor of the preamplifier, if existing, and grounded on the HV plug. On the bottom part the equivalent circuit for calculation the transmission fraction of the γ-flash during the OFF state – defined as $\frac{I_1}{I_1+I_2}$ – is shown.

$OFF \rightarrow ON$, which would generate a long transient of the preamplifier. A schematic circuit of this coupling is illustrated in Fig. 5. The preamplifier and detector are schematically indicated including the feedback capacitor C_p and feedback resistor R_p.

When the switch is ON (S_1 closed, S_2 open) the charge from the signals accumulates into the coupling capacitor C_c. When the transition $ON \rightarrow OFF$ occurs a fraction of this charge still remains as it did not have the time to flow through the pull down resistor R_s which is high (higher than 20 MΩ) to reduce the noise. The left side of C_c should be grounded to match the potential of the detector, which is grounded in the OFF state, when re-connection will happen. This is achieved through R_g. This resistor can be as low as needed to fulfill the condition $R_g \cdot C_c \ll OFF$ duration. The lower limit is imposed by the acceptable fraction of the γ-flash which is mainly transmitted through R_g. In the OFF state we measured an equivalent resistance of S_2 with a value of R_{S2}=10 Ω and of S_1 with a value of R_{S1}=500 kΩ, respectively. With R_g=100 kΩ, the corresponding transmitted fraction of the γ-flash is defined in Fig. 5 as $\frac{I_1}{I_1+I_2} = \frac{R_{S2}}{R_{S2}+R_g \| R_{S1}}$ and has a value of about 10^{-4} to 10^{-5}, which is definitely acceptable, and even beneficial as it provides a time reference.

The pull down resistor R_s is needed to guarantee the discharge of C_c when the switch is in the ON state for a long time. It plays the same role as the usual HV load resistor in preamplifiers. It should be at least 20 MΩ to reduce its contribution to the noise.

2.4. Full scheme of the switch circuit

The full scheme is given in Fig. 6. The compensation branch is made of an inverting Schmitt-trigger to shape the gate command, followed by a adjustable delay. In the branch connected to the switch gate three inverting Schmitt-triggers are inserted to shape the logical signal, invert it against the compensation signal, and compensate for the minimum delay introduced in the compensation branch. As a result the ON state is obtained by grounding, or leaving open ended, the gate input. Conversely if a high level is applied at this input the switch goes into the OFF state. The acceptable high level voltage range is 5-12 V. A set of jumpers allows to connect protecting diodes, to bypass the switch and connect directly the detector to the CSP. In order to operate the circuits with a low level of noise, their 2.5 V supply is delivered by an ultra low noise regulator of type TPS7A901DGNT. Two versions have been built, one integrated with an in-house built CSP [10], the other one as a standalone switch to be used with any preamplifier.

The latest, integrated switch-CSP version has been built in one printed circuit board (PCB). For the design of the PCB it was critical to minimize the stray capacities, increasing the input capacitance, which couple to analog and logical parts.

For this reason small components with high integration have been used on the PCB. In this sense the logical part is well-shielded with ground planes and no ground plane is closely facing the analog line.

2.5. Limitations of the switch circuit

Although the switch is able to toggle in a few tens of ns, its efficiency in experimental conditions is affected by other parameters.

The first requirement is the availability of a trigger signal to flip the OFF/ON states at the right time. In the case of the γ-flash at n_TOF this signal is provided by the PS accelerator. In other cases when the signal to be reduced occurs randomly, as coming from a particle entering the detector, a prompt signal from a faster detector in the path of the particle should be used. If such an early trigger signal is missing the switch cannot be used.

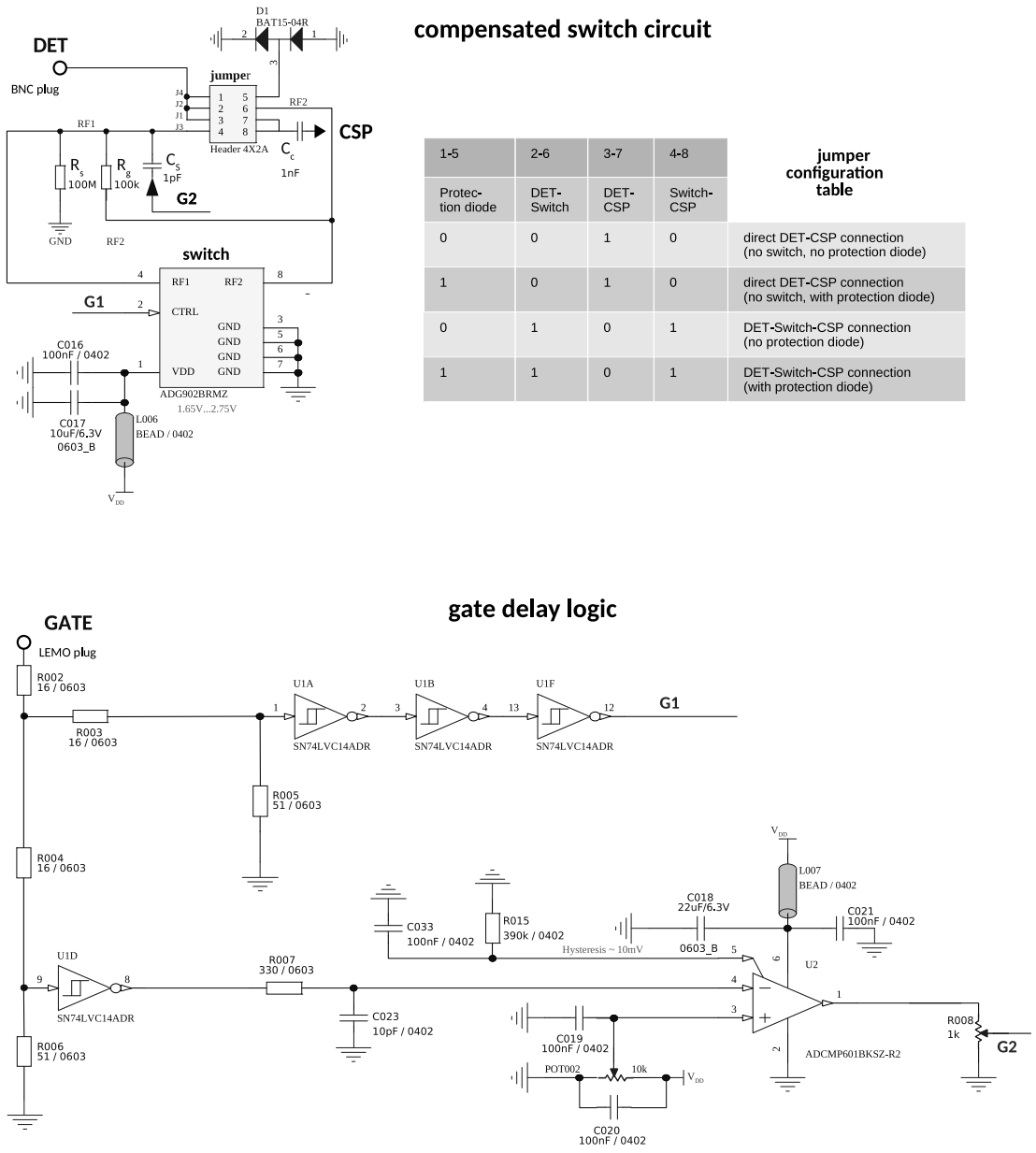
The second parameter affecting the efficiency of the switch is the collection time of the detector, particularly at time of flight facilities. For example if the collection time is 1 µs the switch will have to be in the OFF state during at least that time, thereby limiting the highest energy available in a time of flight facility.

The other limitation is the existence of a strong delayed background. The γ-flash at EAR1 is very prompt, lasting 20 ns. After the collection time of this γ-flash, depending on the detector (1.2 µs for DFGIC, 250 ns for HPGe) the switch can open. If a longer background is present it will not be reduced by the switch. This is exactly the situation in EAR2 where the high flux of fast neutrons produces a large background by scattering in the detector. This delayed component can be reduced by delaying the aperture of the switch, but at the expense of the highest reachable energy. The effect is particularly sensitive at EAR2 due to the short time of flight. This effect, combined with the long collection time, precludes measurements with DFGIC at EAR2. This delayed background coming from the fast neutrons is also present in EAR1 but at a much lower level. Having totally masked the γ-flash with the switch this delayed component becomes visible in the detectors, and it is the main limitation to the resolution when using HPGe detectors for γ-ray detection, even when equipped with the switch.

One should be careful of an important aspect: the coupling circuit. The values of its components are not universal, they should be tuned according to the experimental conditions. We showed already in Section 2.3 that $R_g \cdot C_c$ should be much lower than the OFF state duration. This time is of the order of 1 s at n_TOF, while it is about 2.5 µs at the neutron time-of-flight facility nELBE [11]. At nELBE R_g should be in the order of 100 Ω in order to fulfill the condition for $R_g \cdot C_c$. Thereby the transmission of the γ-flash would be increased to a value of 0.1 (instead of 10^{-4} at n_TOF). However this is not a practical limitation because the intensity of the γ-flash at nELBE is also much lower. This is a general trend linking the instantaneous flux to the repetition rate.

3. Noise figure

The noise spectrum has been investigated for various CSP-switch configurations in order to verify if additional noise is induced by the switch circuit. An oscilloscope of type Teledyne Lecroy (WavePro 254HD, 2.5 GHz High Definition Oscilloscope) with spectral analyzing function has been used to retrieve the frequency components by applying a Fast Fourier algorithm. Both types of switch circuits were investigated in different configurations which are explained below. The most important results are depicted in Fig. 7.



1-5	2-6	3-7	4-8	jumper configuration table
Protec-tion diode	DET-Switch	DET-CSP	Switch-CSP	
0	0	1	0	direct DET-CSP connection (no switch, no protection diode)
1	0	1	0	direct DET-CSP connection (no switch, with protection diode)
0	1	0	1	DET-Switch-CSP connection (no protection diode)
1	1	0	1	DET-Switch-CSP connection (with protection diode)

Fig. 6. Integrated switch-CSP circuit. The DFGIC outputs are connected to DET. A TTL accelerator signal is plugged to $GATE$. The CSP output of the circuit is connected to the preamplifier [10]. For the compensation circuit a single capacitor C_s from Fig. 3(a) is included in the circuit. A set of four jumpers allows to connect or disconnect detector, switch, CSP and the protection diodes. The signal G_1 has a fixed delay (due to the Schmitt-trigger inverters) in respect to G_2. A delay for G_2 in respect to G_1 is created, which can be adjusted with a potentiometer. The amplitude G_2 can be adjusted with a second potentiometer.

First, the comparison between the noise of the oscilloscope and a discrete version of the switch circuit including protection diodes, without preamplifier, directly connected with the $RF1$ output to the oscilloscope has been performed (black curves in Fig. 7).

No additional noise contribution induced by the switch circuit is visible, as expected because this contribution is obviously lower than that of the oscilloscope channel. Then we compared the configuration of the CSP-switch circuit by connecting the switch circuit and the protection diodes (see Fig. 6: jumper positions 1–5, 2–6 and 4–8 are connected) to the configuration where the CSP alone is used (see Fig. 6: jumper position 3–7 is connected). The input of the CSP-switch circuit was left open.

The contribution of the switch and protection diodes to the noise shows up as an increase of about 5 dBm below 1 MHz (blue curves in Fig. 7), as a result of the additional capacities from components or connections of the switch circuit. Apart from low frequencies below 1 MHz (green curves in Fig. 7) no visible additional noise is induced by the switch circuit, because the noise level with the calibration box is much higher due to the capacity of C_d=80 pF, representative of the detector capacity. For a more realistic case the calibration box to simulate the DFGIC is connected to the CSP-switch circuit where the input of the calibration box is open ended.

The last comparison has been performed by simulating a DFGIC signal with a Keithley 3390 (50 MHz Arbitrary Waveform Generator) connected to a calibration box (same like in Fig. 3(a)). The pulse generator produced a 2 kHz periodic saw tooth shaped (rise time=500 ns, fall time=500 ms) signal. This situation corresponds to the actual experimental case when detector signals would be acquired. The spectral analysis was performed over time windows between pulses to probe the noise contribution only (red curves in Fig. 7). No strong difference between using or not using the switch -and diode circuit appears. The increase of the noise between green and red curves can be explained by the contribution introduced by the generator and its long connection cable.

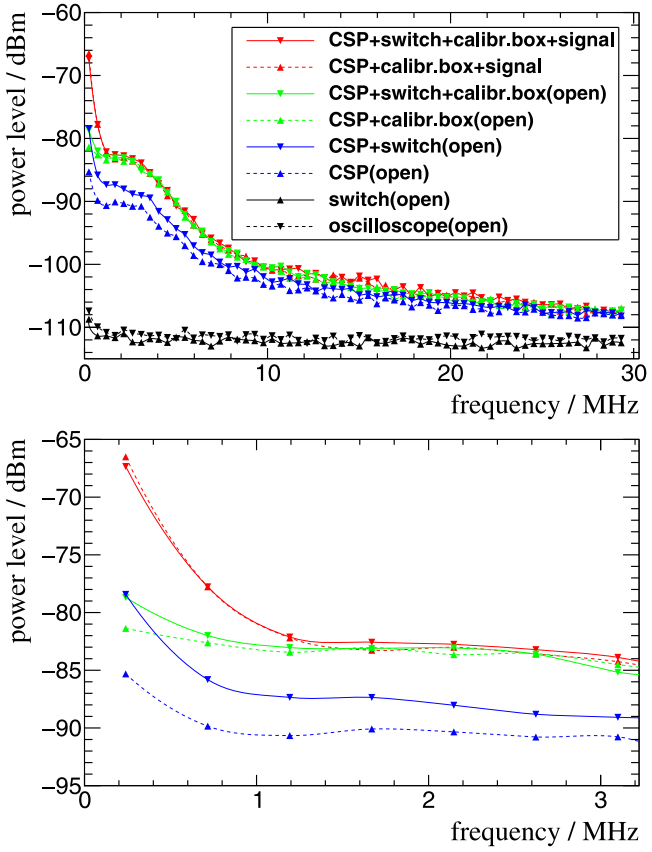


Fig. 7. Noise spectra for different switch-CSP configurations. The upper plot contains the frequency spectra up to 30 MHz. The lower plot is a zoom in the region of the signal up to 3 MHz in order to illustrate the most dominating region of the generated signal and to show the low pass behavior of the CSP. "Open" indicates an open ended, shielded connector at the corresponding input. The colored dashed lines show the configurations of the integrated CSP-switch circuit with using the switch circuit, the solid colored lines without its use, respectively. The voltage scale of the oscilloscope for measuring the black lines was 5 mV/div and for the colored lines it was 50 mV/div. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

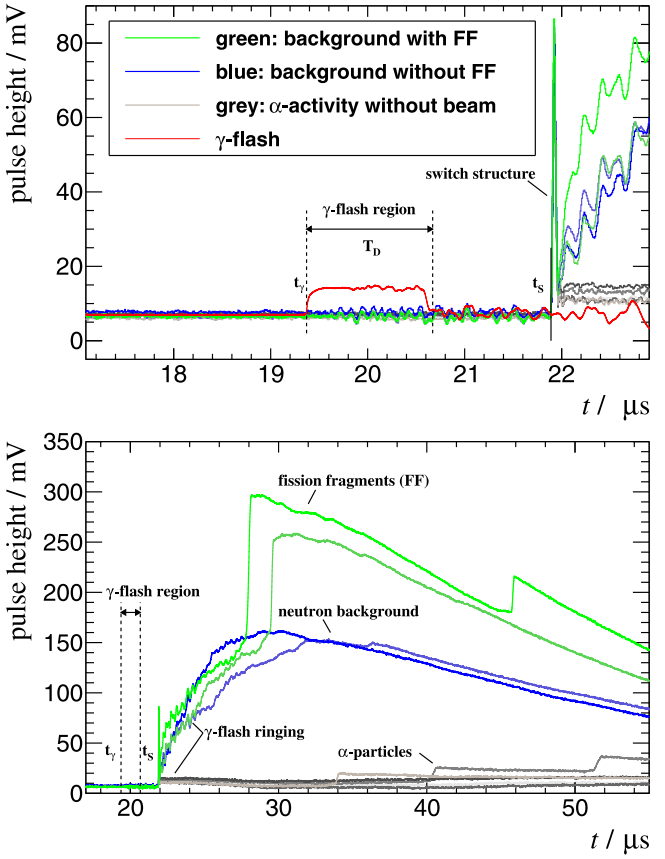


Fig. 8. Typical anode signal trace from a neutron pulse at the CERN n_TOF experiment. The detector is a DFGIC with a 280 µg/cm^2 thin ^{235}U deposit read out by a switch gated CSP (Canberra 2006E). The upper plot shows a zoom around the γ-flash region (dashed black lines). The direct signal from the DFGIC of the γ-flash measured without preamplification is depicted as red line. The γ-flash starts at t_γ=19.4 µs. The charge collection time of the DFGIC leads to a total width of T_D=1.3 µs. The switch allows the signals to pass after $t > t_S$ (t_S=21.9 µs, black line) which is t_S-t_γ=2.5 µs after the start of the γ-flash. The lower plot shows a larger scale of signal traces in order to illustrate signals (α-particles and fission fragments) and background (electromagnetic γ-flash ringing and neutron background).

In conclusion the noise contribution of the switch circuit results mainly from its small capacity addition and it is negligible in practical situations where the detector has an internal capacity of at least 10 pF.

4. Applications of the switch circuit at pulsed beam sources

4.1. The $^{16}O(n, \alpha)$ measurement at CERN n_TOF

In November 2018 the measurement with the switch circuit has been performed at CERN n_TOF in EAR1. The setup consisted of two DFGICs [12] operated with 95%Kr 5%CO_2 at 1.3 bar. One of the DFGIC contained a ^{235}U deposit and is used to monitor the neutron flux. The ^{235}U deposit has a thickness of about 280 µg/cm^2. The α-activity is dominated by the contaminant of^{234}U (atom ratio: $\frac{^{234}U}{^{235}U}$=0.00747, activities: $A(^{234}U)$=20 kBq, $A(^{235}U)$=1 kBq).

All DFGIC-switch-CSP signals coming from the two detectors were digitized with the standard data acquisition system of CERN n_TOF using Waveform Digitizers (SPDevice, ADQ14, 14 bit). The wave forms are recorded up to a maximum time window of 0.1 s with a sampling rate of 250 MS/s. The DAQ is triggered with the accelerator period of 1.2 s by the Proton Synchroton.

At that time the switch circuit was built as discrete circuit connected to the preamplifier of type Canberra 2006E. However the working principle was the same as explained in Fig. 6. The HV is biased by an internal voltage divider integrated in DFGIC [3,12]. The pull down resistor of R_s=20 MΩ and the coupling capacitor typically in the order of C_c=1 nF were used from the former HV biasing components of the preamplifier, while we adopted $R_g = \infty$. The corresponding decay time of 5τ=$5R_s \cdot C_c$=100 ms (decayed to 0.7% of the charge value) is much shorter than the difference of the accelerator period (1.2 s) and the maximum acquisition time (0.1 s). Consequently the charge of C_c can be released during that non-acquisition time of 1.1 s when the switch is OFF.

An example of recorded anode wave forms for the ^{235}U containing DFGIC is displayed in Fig. 8. Approximately 5 MeV α-particles coming from the decay of ^{234}U (4.8 MeV) and ^{235}U (4.7 MeV) are depicted in comparison with fission fragments and neutron background. The red curve in the upper diagram corresponds to the γ-flash signal when the detector is connected directly to the digitizer without any CSP nor switch. In such conditions only the γ-flash is visible, the other physical signals being too small. The collection time of 1.2 µs is well seen while the total deposited charge can be assessed to be 200 pC, corresponding to an energy deposition of about 25 GeV. Obviously any preamplifier having a gain suitable for a few MeV particles saturates when receiving such an amount of charge, thereby confirming the need of the switch circuit to drain. With the optimized compensation of the switch circuit only a narrow Gaussian shaped structure (FWHM=30 ns), which is always constant appears at the transition time t_S. The narrow

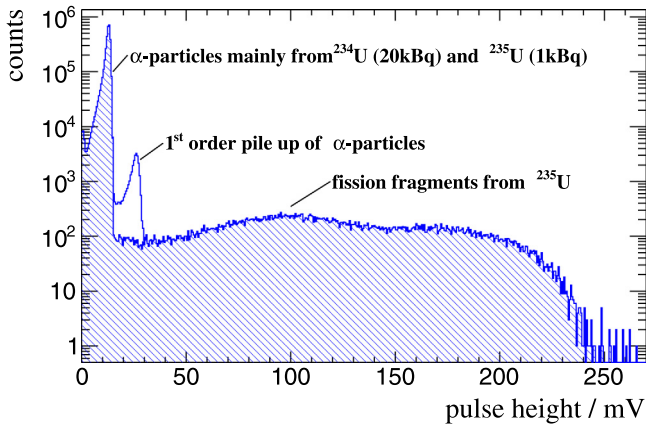


Fig. 9. Pulse height spectrum of DFGIC anode signals from about 3800 neutron pulses at the CERN n_TOF experiment. The detector is a DFGIC with a 280 μg/cm^2 thin ^{235}U deposit read out by a switch gated CSP (Canberra 2006E). The expected counts of α-particles is about 6 million. The measured counts is about 3 million and agrees with the expectation, assuming that the DFGIC has a detection efficiency of about 50% due to absorption effects of backward emitted α-particles in the deposit. About two orders of magnitude less also pile-up of two α-particles appears. That pile-up has been significantly reduced by applying a pulse height dependent rise time cut of for α-signals (hatched area). Above about a pulse height of 30 mV the region of the fission fragments starts.

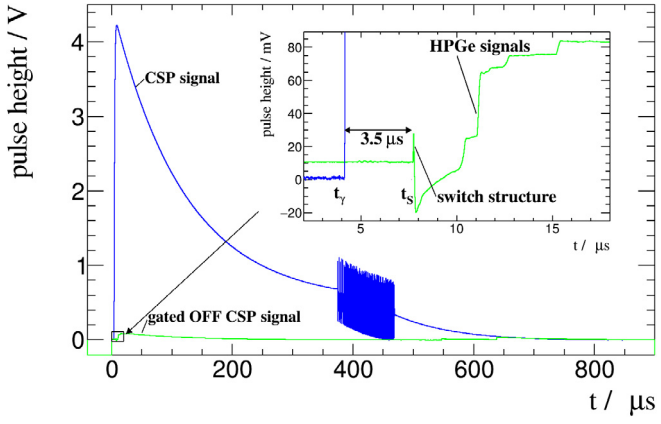


Fig. 10. Signal traces from a HPGe switch test at n_TOF in EAR1 in 2018. The solid blue line shows the CSP without gated-off region. The γ-flash starts at t_γ=4.1 μs. That CSP shows a saturation effect for almost the entire time frame of 1 ms. The CSP misbehaves if the induced charges cause an pulse height close to 4 V. Also strong ringing (here at 400 μs) caused by the CSP appears. The green line shows the CSP gated off to about 3.5 μs after the γ-flash. The switch operates in the ON state after 7.6 μs. HPGe signals in the order of 10 mV are visible. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

structure is followed by a few μs long smooth tail. The switch is in the OFF state from the start of the γ-flash up to 2.5 μs after the γ-flash. That allows to reach neutron energies up to 20 MeV in EAR1.

The typical charge values from this DFGIC test are shown in Table 1. In that measurement the switch allowed to reveal pile-up of neutron induced background reactions which induced charges with up to two orders of magnitude higher than induced by single α-particles. In retrospect it turned out that this background is due to the high instantaneous neutron flux of the facility. The neutrons undergo elastic and inelastic collisions on the nuclei composing the gas inside the DFGIC. Each recoil has an energy lower than 100 keV but they are so numerous that they pile up as a continuous current in the chamber [12]. Signals from 5 MeV α-particles and fission fragments as demonstrated in the pulse height spectrum in Fig. 9 could be analyzed. However at that time the setup was not optimized to detect low energy α-particles (<4 MeV) on that high neutron background. It should be mentioned that this fast

Table 1
Order of magnitudes of charges induced from the DFGIC in the CSP. The charge of the γ-flash without switch is estimated from the current of the γ-flash anode signal of the DFGIC measured without preamplifier. The estimation of the charge of the γ-flash with switch is based on the attenuation 10^{-5} when the switch circuit is OFF. The other charges where estimated from CSP anode signals of the DFGIC.

Type of induced charge in CSP	Charge/fC
γ-flash with switch	1
Residual switch structure	0–10
5 MeV α-particles	30
Fission fragments	10^2–10^3
Uncompensated switch structure	$2 \cdot 10^3$
Neutron background	10^3–10^4
γ-flash without switch	$2 \cdot 10^5$

neutron component is more than an order of magnitude higher at EAR2, due to the higher flux, and narrower in time by a factor 10, due to the shorter path length.

4.2. Direct applications of the switch circuit

For the application of the time-of-flight technique it can be necessary to have the timing information of the γ-flash to extract a reference time in order to calibrate the neutron time-of-flight. By lowering the value of the introduced ground resistor R_g a higher fraction of the γ-flash can pass through the OFF state of the switch. That means the switch can also be operated in a way that it *attenuates* signals in the OFF state.

Frisch-grid ionization chambers

This new technology can be used to measure light charged particle reactions such as ^{14}N(n, α), ^{19}F(n, α), ^{12}C(n, α) and^{10}B(n, α). These reaction measurements using Frisch-grid ionization chambers have been proposed at CERN n_TOF [13] and are relevant for ^{4}He production in nuclear materials as e.g. fuel and structural material components.

HPGe detectors

For two decades several attempts have been pursued at CERN n_TOF to measure on-line γ-rays at neutron energies higher than 1 MeV, in particular to study inelastic and (n,xn) reactions [14]. This was part of the program developed at the commissioning of n_TOF, and the γ-flash problem was already pointed out [7]. Later some electronic solutions have been attempted, using for example an active reset on the first transistor of the CSP [6]. They all failed due to the intense γ-flash saturating the preamplifier, preventing the use of high purity germanium detectors (HPGe) for in-line γ-spectroscopy. We provided Mirion/Canberra with the switch scheme and asked them to integrate the circuit in a prototype of a gated HPGe detector. A successful HPGe detector test using this prototype was performed in 2018 in EAR1 at n_TOF. Fig. 10 shows the HPGe signals induced by fast neutrons. In this test condition the sample was much thicker than for a true measurement, producing a high detection rate. The pulse height steps from the photons are well visible. The resolution is expected to be worse than in a standard out of beam measurement due to the limited separation between the steps in such conditions. In addition, the photon signals sit on a wide and smooth background coming from the elastic recoils in the detector from the fast neutrons scattered by the sample. However the off-line resolution, measured with sources, with the switch inserted is 3 keV(FWHM) at 1.4 MeV.

4.3. Other possible applications of the switch circuit

Hereafter we give some possible applications of the switch circuit in different contexts although the experimental tests have not been performed. They can be considered as guiding ideas and schemes to be implemented and tested in situations where low signals have to be recorded after a huge one leading to the saturation of the CSP.

Micro megas detectors

At CERN n_TOF several fission experiments [15,16] were carried out with Parallel Plate Avalanche counters (PPAC), Fast Ionization Chamber (FIC) and Micro Megas detectors [17]. Although PPACs are not affected by the γ-flash thanks to their very low material density, FIC and Micro Megas are sensitive to it. They could be used up to 20 MeV by using preamplifier working a mode intermediate between current and charge, with a reduced gain, and by applying special methods in the analysis to get rid of the oscillations after the saturation induced by the γ-flash. The methods prevent a continuous measurement of the cross section in energy and only a few energy points can be given. The insertion of the switch would prevent the saturation and by reducing the subsequent oscillations would allow to reach higher energies in safer conditions. Furthermore ^{10}B(n, α) reactions in order to measure the neutron flux could be better performed with Micro Megas detectors. A short test performed with a preliminary version of the switch was promising but it has to be confirmed.

Scintillation detectors

Neutron capture measurements at n_TOF use scintillators (C6D6 [18], BaF_2 [19] detectors) coupled to photo multipliers. Due to the γ-flash the measurements are restricted to neutron energies lower than 1 MeV or even less. The saturation takes place in the last stages of the photo multiplier where the current induced by the flash is large due to the multiplication. Despite the improvements applied to the voltage divider the situation did not improve significantly due the huge ratio between the expected signals and the intensity of the γ-flash. The solution would consist of using only the 6 first stages of the photo multiplier, read out the signal at this dynode and complete the signal amplification with switch-preamplifier assembly. This would create a gated scintillation detector suitable for detecting photons induced by energetic neutrons, without HV bias adjustment or gating.

Application to ion implantation and decay

Another type of application of the switch circuit are decay studies of very exotic nuclei [20]. The typical situation is that exotic nuclei are produced in a target and selected by magnetic fields. The selected ions are implanted into a silicon detector (after slowing down by a degrader). The charge information of the silicon signal is used to guarantee the ion identification. After some time the implanted nucleus decays by β, p or $2p$ emission which leave a signal in the silicon detector. This signal should be recorded to fully characterize the decay. Usually it is small compared to the signal generated by the implantation in the same detector, so that the preamplifier has to be low gain to record correctly the implantation signal, and high gain to do the same for the decay signal. The switch solution can easily solve this situation and would allow to access short lived decays. The scheme is shown in Fig. 11.

Silicon detectors

With the same scheme of Fig. 11 the switch circuit could be integrated for silicon detectors. For example, at n_TOF silicon detectors are used in different fields such as proton-recoil telescopes [21], double differential cross section (DDX) setups [22] and as neutron flux monitor [23]. The benefit using the switch is to reduce the disturbance by the γ-flash and reach higher neutron energies up to several 100 MeV. A project of such a modification integrating the switch circuit in the CSP used for silicon detectors in a DDX setup is currently ongoing [24].

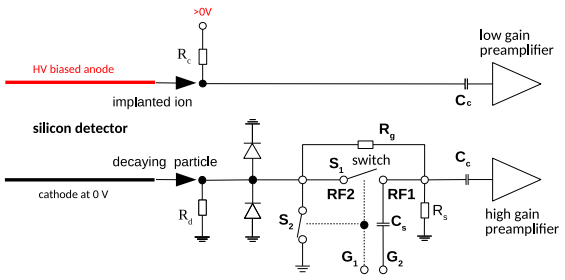


Fig. 11. Scheme of ion implanted silicon detector operated simultaneously in high and low gain. The ion implantation signals are read out by the HV biased anode using a low gain preamplifier. The decaying particles are read out by the non HV biased cathode using a high gain preamplifier. The switch is used to avoid the saturation of the high gain preamplifier when the prompt ion signal induces its charge.

5. Summary

A ns-gating switch circuit has been developed in order to prevent the saturation of the charge sensitive preamplifier by the γ-flash at the n_TOF facility. In-beam measurements using Double Frisch Grid Ionization Chamber with that switch circuit was successful in draining out the charge deposited by the γ-flash and helped to reveal neutron induced background reactions.

The main component is the CMOS reflective switch ADG902 which drains in the OFF state all charges coming from the detector to ground and disconnect the detector from the preamplifier to prevent its saturation. Due to gate capacitance of the internal MOSFET inducing a charge during the transition of the switch it was mandatory to develop a compensation circuit. The compensation was mainly achieved by using a capacitor which injects approximately the opposite transition charge. Furthermore it was required to design a coupling scheme to the preamplifier to avoid any DC mismatch, typical of switching devices, which would trigger transients after re-connection.

The spectral analysis of the noise showed that no significant noise was induced by the switch circuits (including the protection diodes).

In general, the switch allows to gate a preamplifier for detection systems which have a short-time detector response and suffer from a prompt high instantaneous charge collection. It is suited for various applications at pulsed radiation sources, especially at CERN n_TOF having a high instantaneous neutron flux and a high γ-flash background. The circuit developed here can also be used as a gated device for small signals before preamplifiers or behind photo multipliers in order to avoid saturation effects of the electronic chain.

CRediT authorship contribution statement

Sebastian Urlass: Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing. **Arnd Junghans:** Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing. **Federica Mingrone:** Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing. **Paul Peronnard:** Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing. **Daniel Stach:** Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing. **Laurent Tassan-Got:** Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing. **David Weinberger:** Conception or design of the work, Acquisition, analysis, or interpretation of data for the work, Writing - original draft, Writing - review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] C. Guerrero, et al., 49-27, Eur. Phys. J. A (2013) http://dx.doi.org/10.1140/epja/i2013-13027-6.
[2] E. Chiaveri, et al., EPJ Web Conf. 239 (2020) 17001, https://doi.org/10.1051/epjconf/202023917001.
[3] S. Urlass, et al., Springer Proceedings in Physics, 219, 2019, pp. 457–460, http://dx.doi.org/10.1007/978-3-030-13876-9_89.
[4] A. Stamatopoulos, et al., HNPS Proceedings, 26, 2018, pp. 224–227, http://dx.doi.org/10.12681/hnps.1824.
[5] G.F. Knoll, Radiation detection and measurement, fourth ed., Wiley, ISBN: 978-0-470-13148-0, 2010.
[6] C. Boiano, et al., IEEE Nuclear Science Symposium Conference Record, 2006, pp. 357-359, https://doi.org/10.1109/NSSMIC.2006.356175.
[7] Final Report of the n_TOF-ND-ADS Project, FIKW-CT-2000-00107, EC 5th Euratom framework program.
[8] Data Sheet ADG901/ADG902, http://www.analog.com/media/en/technical-documentation/data-sheets/ADG901_902.pdf.
[9] K. Heidel, H. Gude, Technical Information Manual, 2006, HZDR, unpublished.
[10] D. Weinberger, in: TU Chemnitz (Ed.), Dissertation, 62, 2018, Fig. 53. https://www.qucosa.de/api/qucosa%3A20912/attachment/ATT-0/.
[11] R. Beyer, et al., Nucl. Instrum. Methods A 723 (2013) 151–162, https://doi.org/10.1016/j.nima.2013.05.010.
[12] S. Urlass, et al., Int. Conf. on Nucl. Data for Sc. and Tech, in: EPJ Web of Conferences, 239, 2019, 01030, https://doi.org/10.1051/epjconf/202023901030.
[13] A. Goverdovski, et al., CERN INTC proposal, 2015, https://cds.cern.ch/record/1980077/files/INTC-P-430.pdf.
[14] R.Vlastou, et al., CERN INTC-O-015 proposal, 2012, pp. 50-52. https://cds.cern.ch/record/1411635/files/INTC-O-015.pdf.
[15] A. Tsinganis, et al., Physics Procedia 64 (2015) 130–139, https://doi.org/10.1016/j.phpro.2015.04.017.
[16] N. Colonna, et al., Eur. Phys. J. A 56 (2020) 48, https://doi.org/10.1140/epja/s10050-020-00037-8.
[17] Y. Giomataris, et al., Nucl. Instrum. Methods A 376 (1996) 29–35, https://doi.org/10.1016/0168-9002(96)00175-1.
[18] R. Plag, et al., Nucl. Instrum. Methods A 496 (2003) 425–436, https://doi.org/10.1016/S0168-9002(02)01749-7.
[19] C. Guerrero, et al., Nucl. Instrum. Methods A 608 (2009) 424–433, https://doi.org/10.1016/j.nima.2009.07.025.
[20] J. Giovinazzo, et al., Phys. Rev. Lett. 89 (2002) 102501, https://journals.aps.org/prl/pdf/10.1103/PhysRevLett.89.102501.
[21] A. Manna, et al., IL NUOVO CIMENTO, 42 C, 2019, p. 142, https://doi.org/10.1393/ncc/i2019-19142-6.
[22] L. Audouin, et al., CERN INTC-P-507 proposal, 2017, https://cds.cern.ch/record/2263778/files/INTC-P-507.pdf.
[23] S. Marrone, et al., Nucl. Instrum. Methods A 517 (2004) 389–391, https://doi.org/10.1016/j.nima.2003.09.060.
[24] R. Beyer, et al., CERN INTC-I-221 letter of intent, 2020, https://cds.cern.ch/record/2731958/files/INTC-I-221.pdf.