Single Event Upsets in the ATLAS IBL Frontend ASICs at the Large Hadron Collider at CERN

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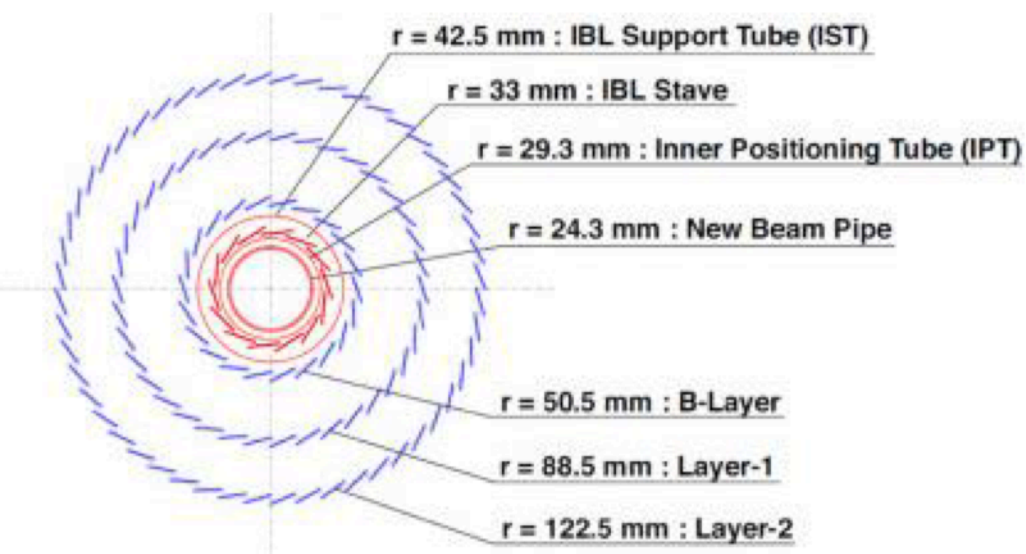
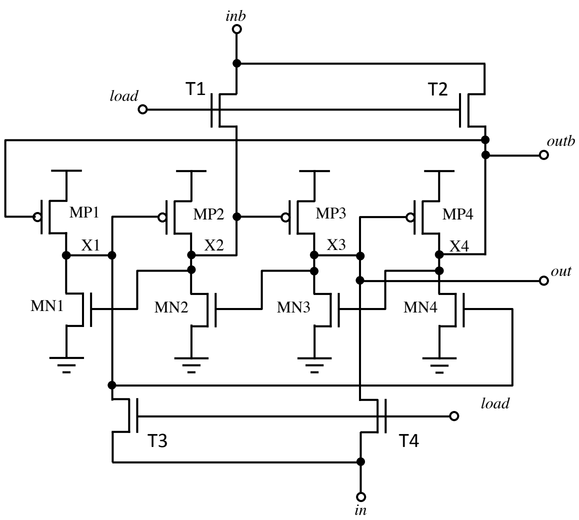
ATLAS IBL Frontend ASICs at the Large Hadron Collider at CERN

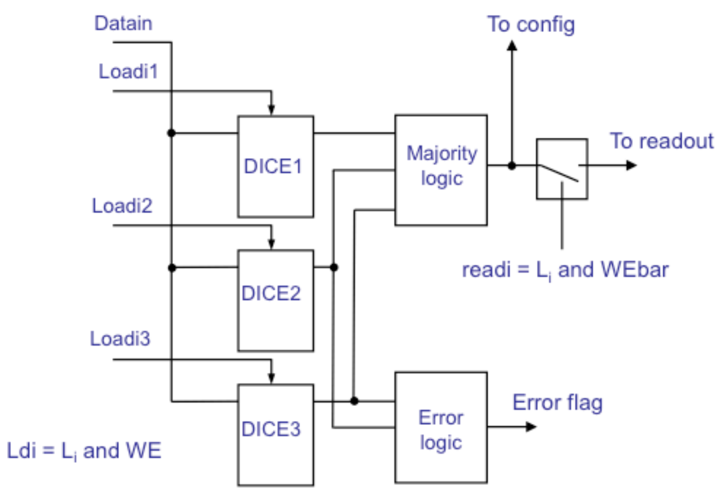
- LHC delivered in 2015/2018 total of 156 fb^{-1} integrated luminosity to ATLAS for 13 TeV pp collisions.
- Maximum of 2.1 10^{34} cm^{-2} s^{-1} peak stable beam luminosity.
- Up to 0.77 fb^{-1} luminosity delivered per LHC fill.
- Pixel detector operated at extremely high-radiation environment, in particular Insertable B-Layer (IBL) at R=3.3 cm received the dose 8.7 10^{14} 1 MeV n_{eq} cm^{-2} .



- For introduction to ATLAS Pixel and LHC see talk Paolo Sabatini
- IBL pixel front end chip FE-I4-B in 130 nm technology was designed with Single Event Upset (SEU) hard configuration memory.
- Inside the pixels Dual Interlocked Cell (DICE) latches were used.

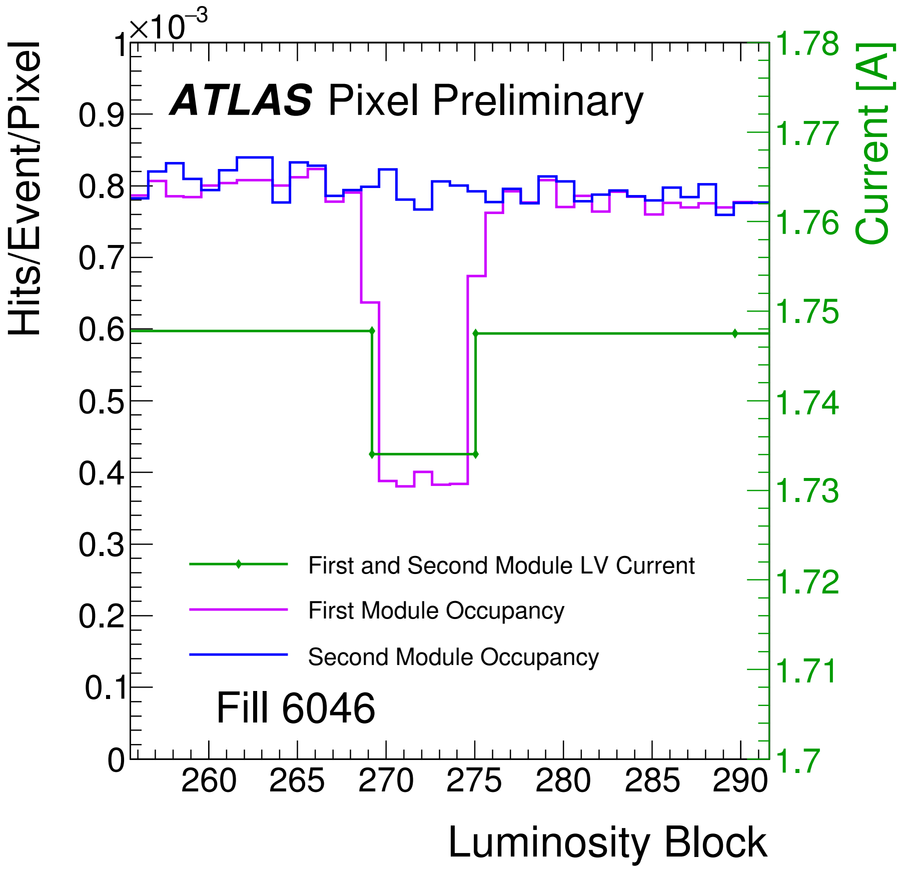
DICE latches





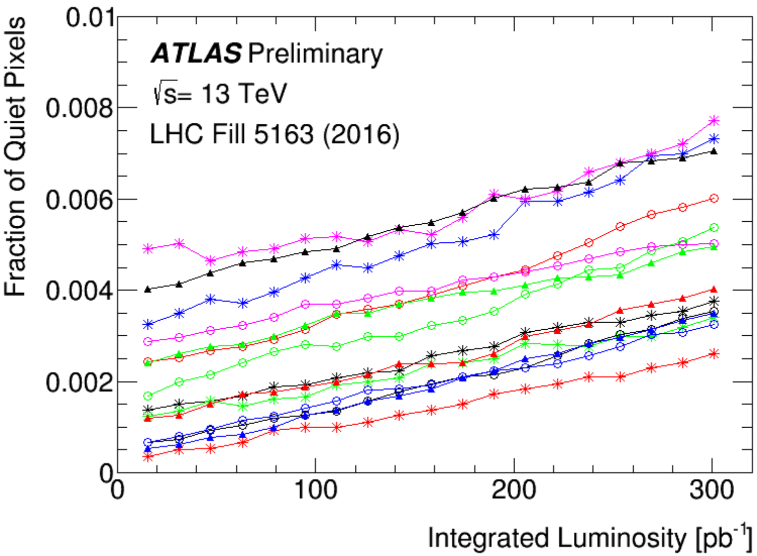
- DICE latches have redundant storage nodes and restore the cell original state when an SEU error is induced in a single node.
- Cross coupled inverter latch structure with four nodes (X1-X4) stores data in two pairs of complementary values.
- If positive upset pulse on X1, than transistor MP2 is blocked, avoiding propagation of this perturbation to node X2.
- The SEU immunity is lost if two sensitive nodes (for example X1-X3) change the state by single particle impact.
- The tolerance to SEU is increased by Hardened By Design (HBD) approach: spatial separation of critical nodes, isolated wells, guard rings and interleaving of cells.
- Global configuration memory is further protected by triple DICE latches with addition of simple majority logic.

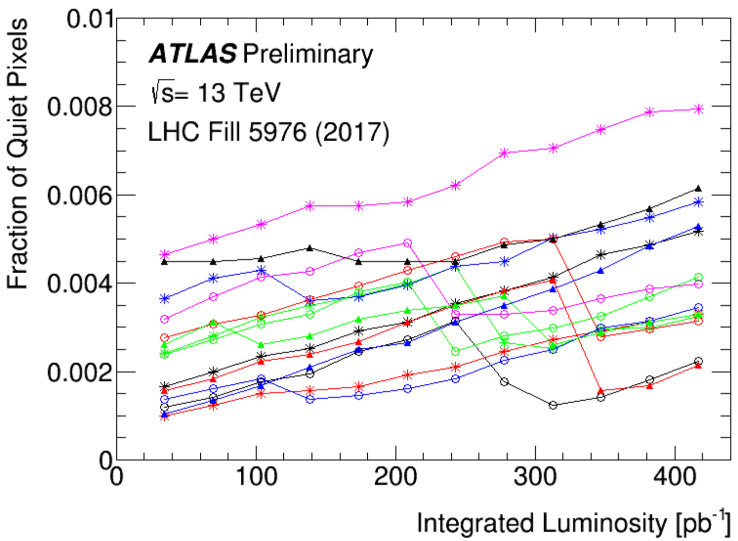
SEU in Global Registers



- Global Registers (GR) corruption has big impact on module operation:
  - change of the low voltage consumption
  - drops in occupancy
  - silent modules
  - desynchronized modules.
- Refreshing of the GR restore proper function of the module.

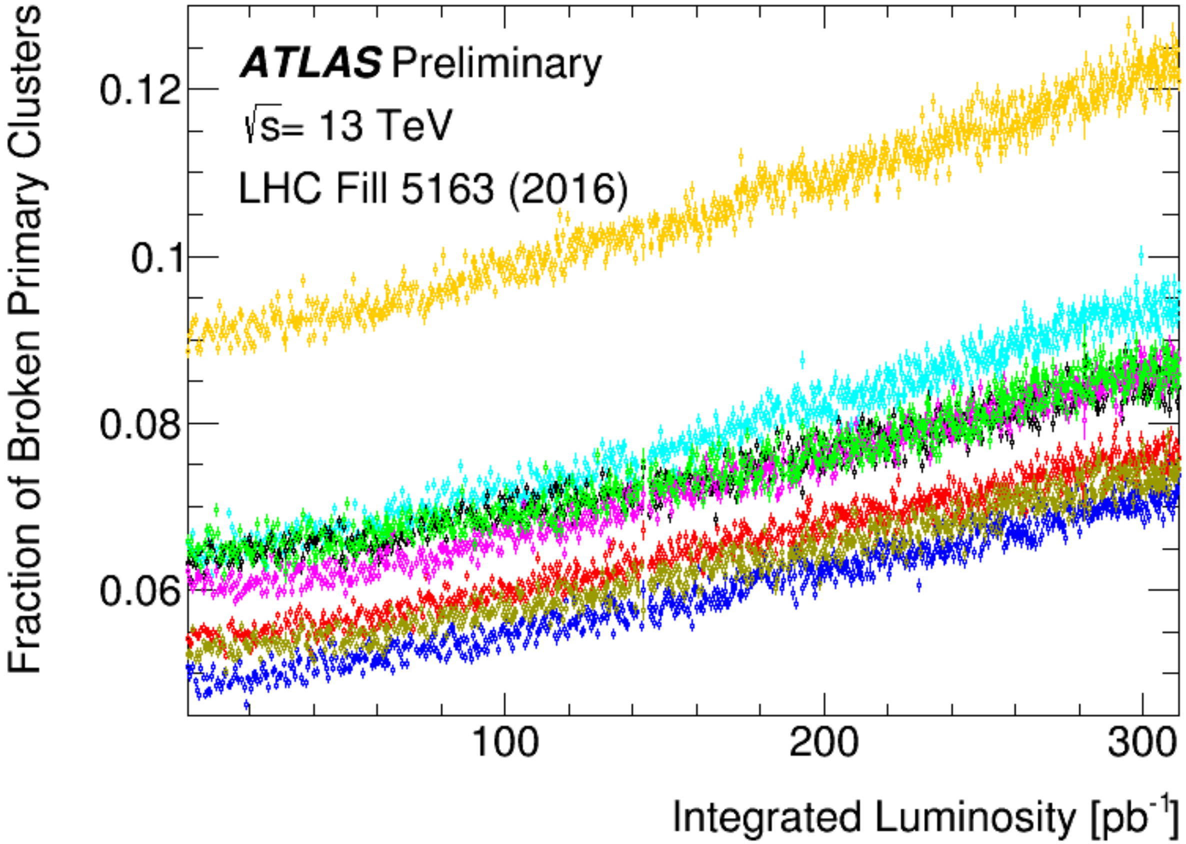
SEU in Local Pixel Memory





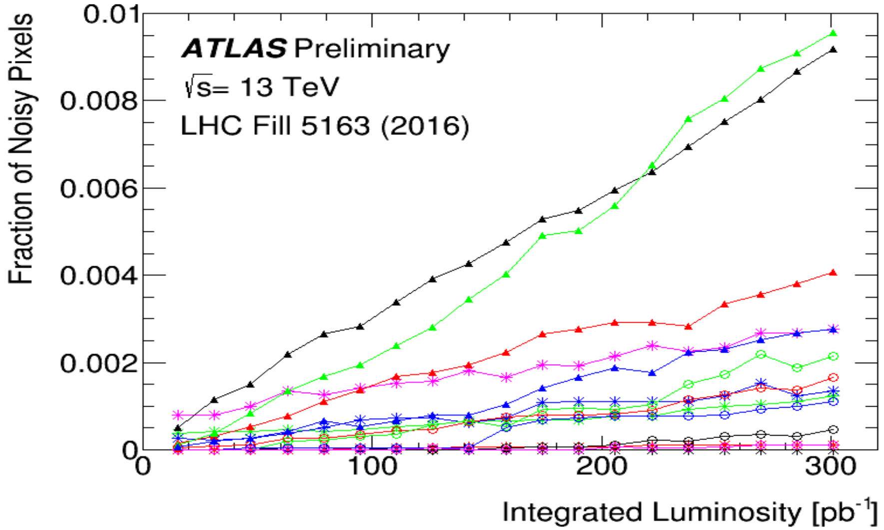
- Pixel local configuration: 13 bits/pixel: Enable, TDAC (thresholds 5 bits), FDAC (feed back current 4 bits), HitBus, Injection Caps (2 bits).
- SEU DICE cross-section measured for FE-I4-A in the 24 GeV proton test beam is 1.1 10^{-15} cm^{-2} (enable bit, 0 ->1 transition).
- Hadron flow at IBL predicted by PYTHIA/ FLUKA simulation tuned to ATLAS data: 91.0 10^{11} cm^{-2} fb^{-1} hadrons with E>20 MeV at planar modules.
- Expect 274 pixels/fb^{-1}/chip SEU flips of Enable bit 0->1
- Enable bit SEU flip 1->0 : “Quiet” pixel.
- 2016: no automatic recovery actions, linear rise of quiet pixels
- 2017: automatic recovery actions drops the number of quiet pixels in the middle of the fill.

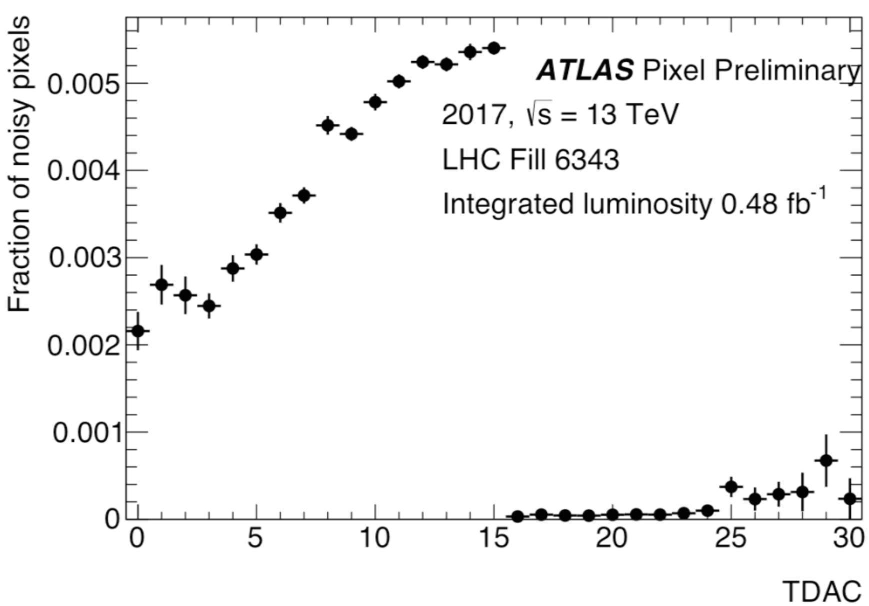
Broken clusters



- Quiet pixels cause clusters to be broken
- In high η modules average cluster length is 9
- Fraction of broken clusters versus luminosity

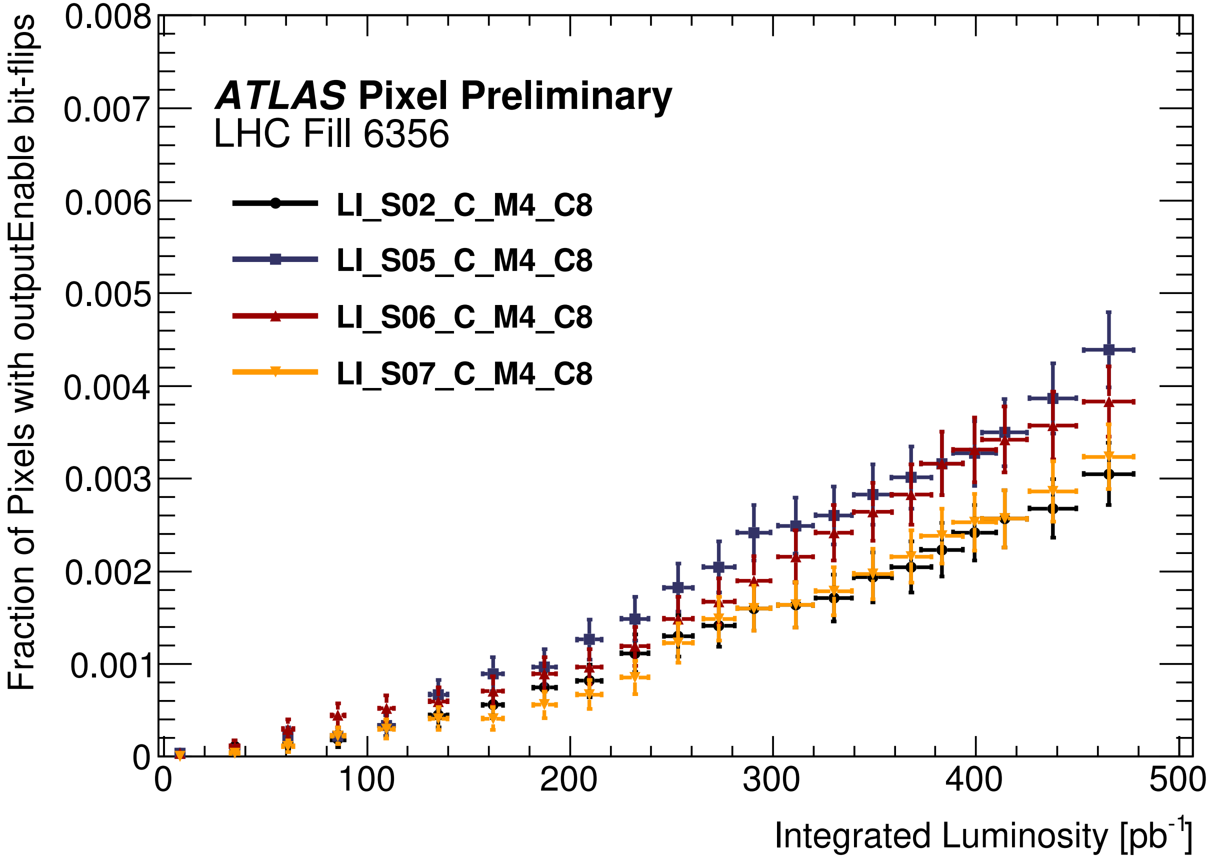
Noise due to SEU in local pixel threshold





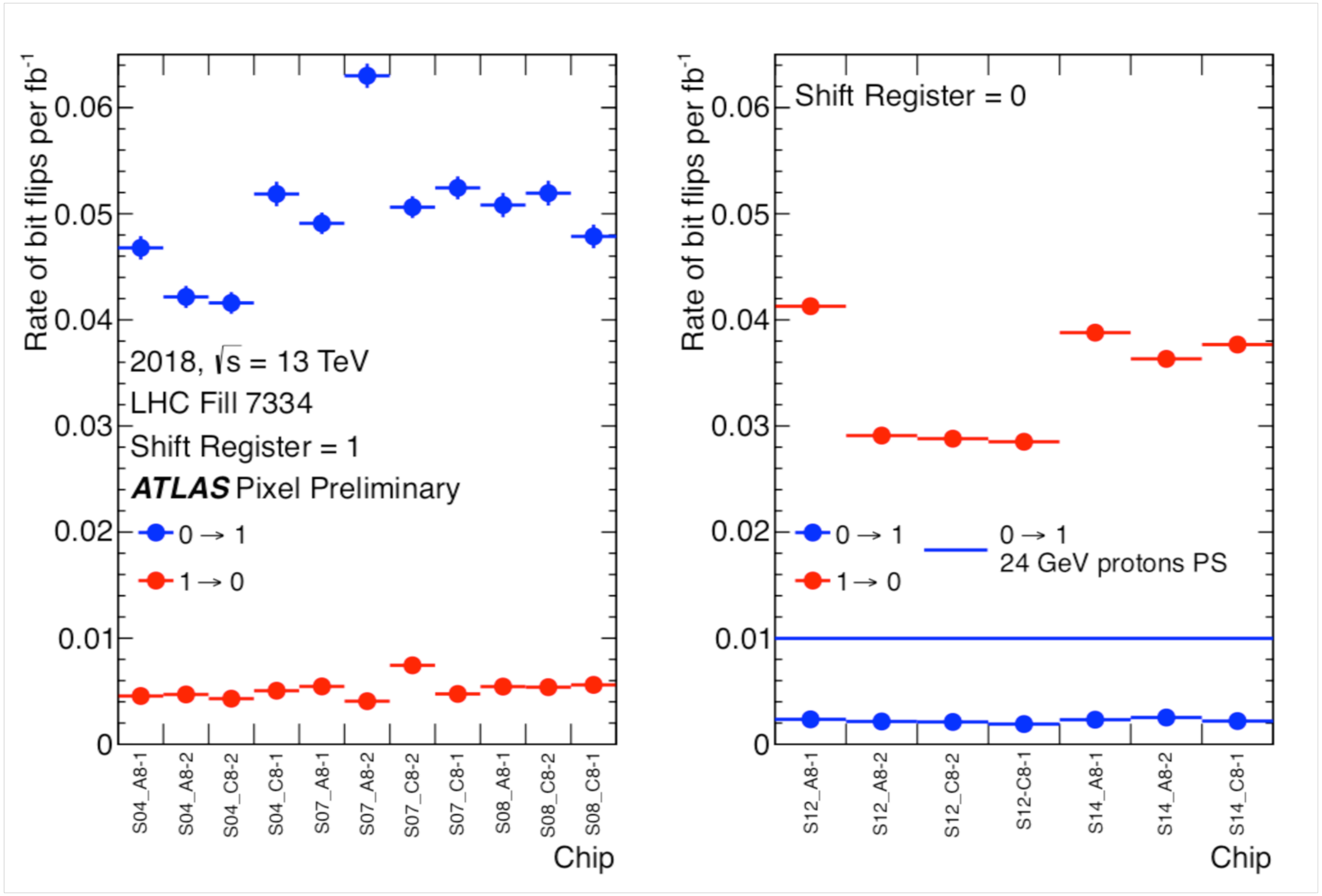
- Correlation of noisy pixels with initial TDAC value.
- Low TDAC values correspond to high thresholds.
- Biggest fraction of the noise happens after SEU flip 0->1 of MSB of TDAC, which sharply reduces the pixel threshold and increases the noise.

SEU in local Enable bit



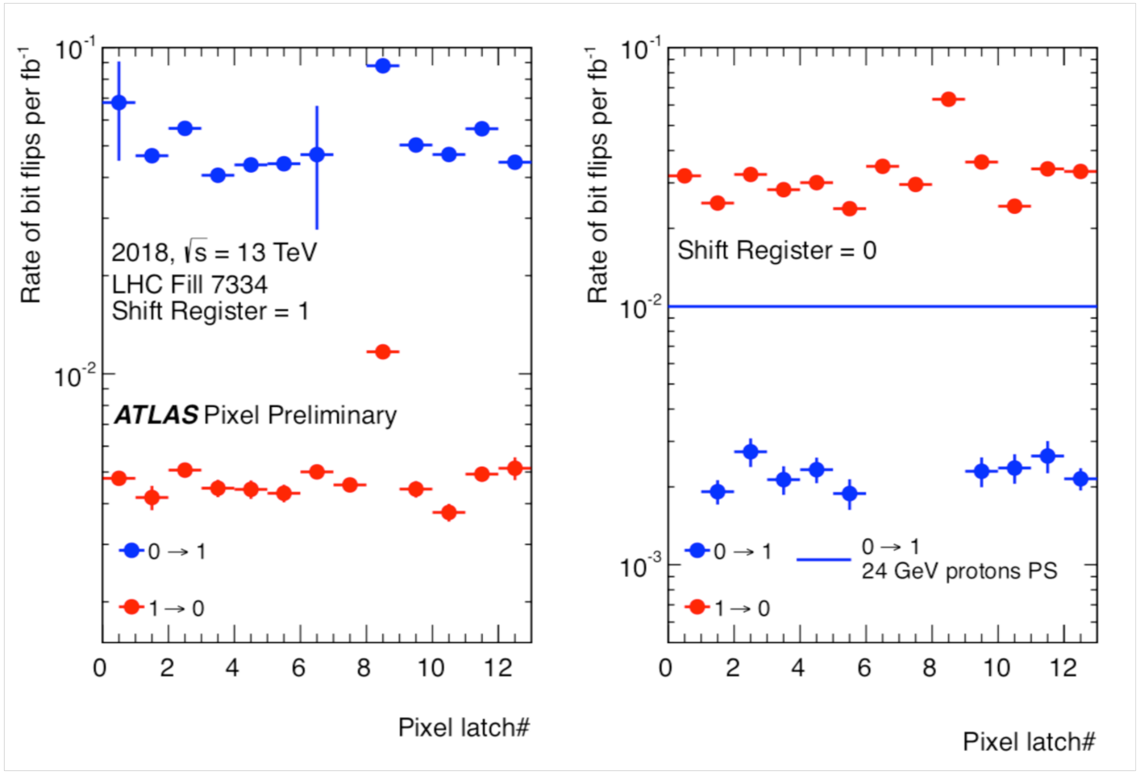
- Test with four high η modules
- Enable bits initially set to “0” (masking all pixels in the module)
- During LHC fills some Enable bits are flipped by SEU to “1”

Distinguish SET from SEU



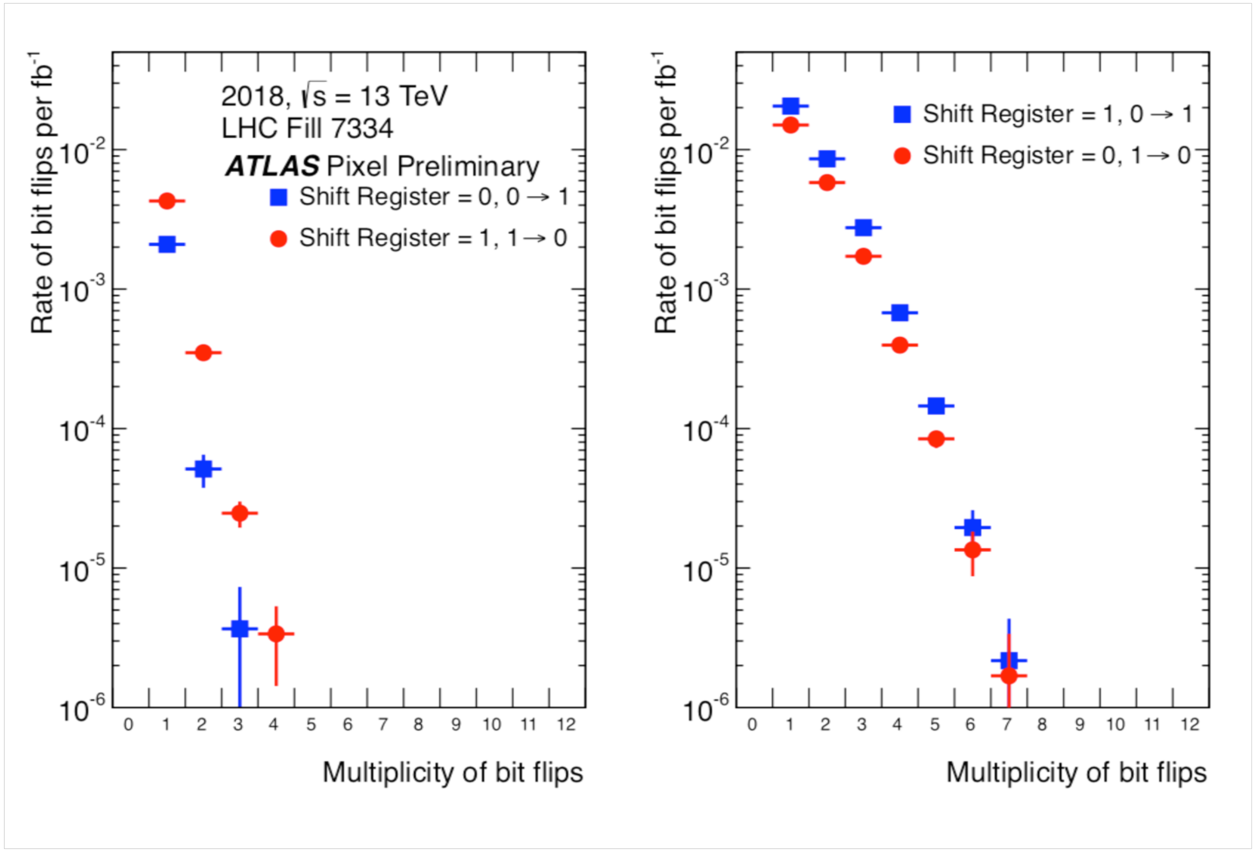
- Read back local memory at the end of fill and compare with initial settings
- Separate modules with Shift Registers (SR) “1” and “0”
- Rate of flip flops versus chip #
- Glitches(SET) on LOAD line dominate 0->1 flips when SR=1
- Glitches(SET) on LOAD line dominate 1->0 flips when SR=0

SET nature of flips for different bits



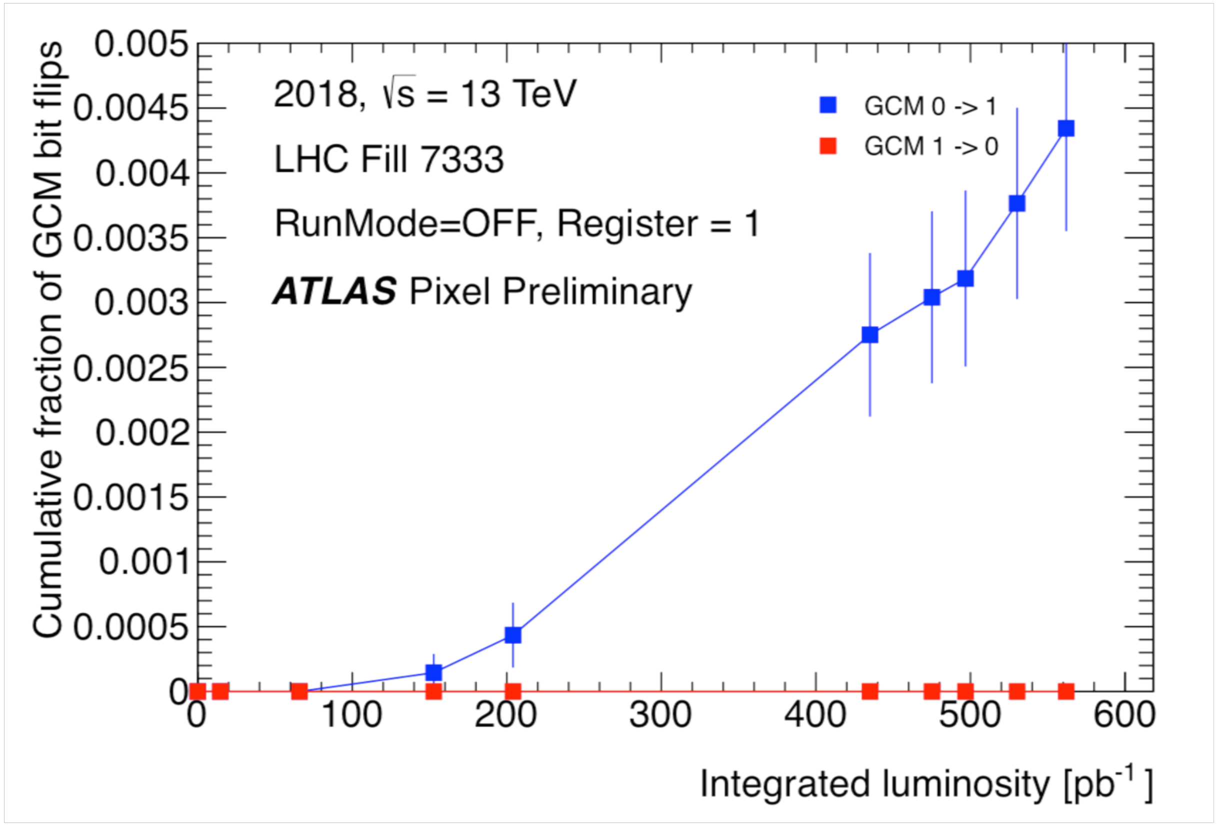
- Rate of flip flops versus bit #
- Glitches(SET) on LOAD line dominate 0->1 flips when SR=1
- Glitches(SET) on LOAD line dominate 1->0 flips when SR=0
- Uniform rate for most of the bits, except HitOr (bit# 8)
- HitOr has very special layout, as interconnection of all pixels
- 24 GeV proton results contaminated by SET due to SR flips

Multiplicity of SEU/SET



- Are the glitches on LOAD line common to several pixels or individual ?
- Multiplicity of bit flips are peaked at “1”, so glitches are mainly individual (pairs of transistors T1-T2 or T3-T4)
- Longer tails in SET may indicate small multi-pixel contribution

Global Configuration Memory

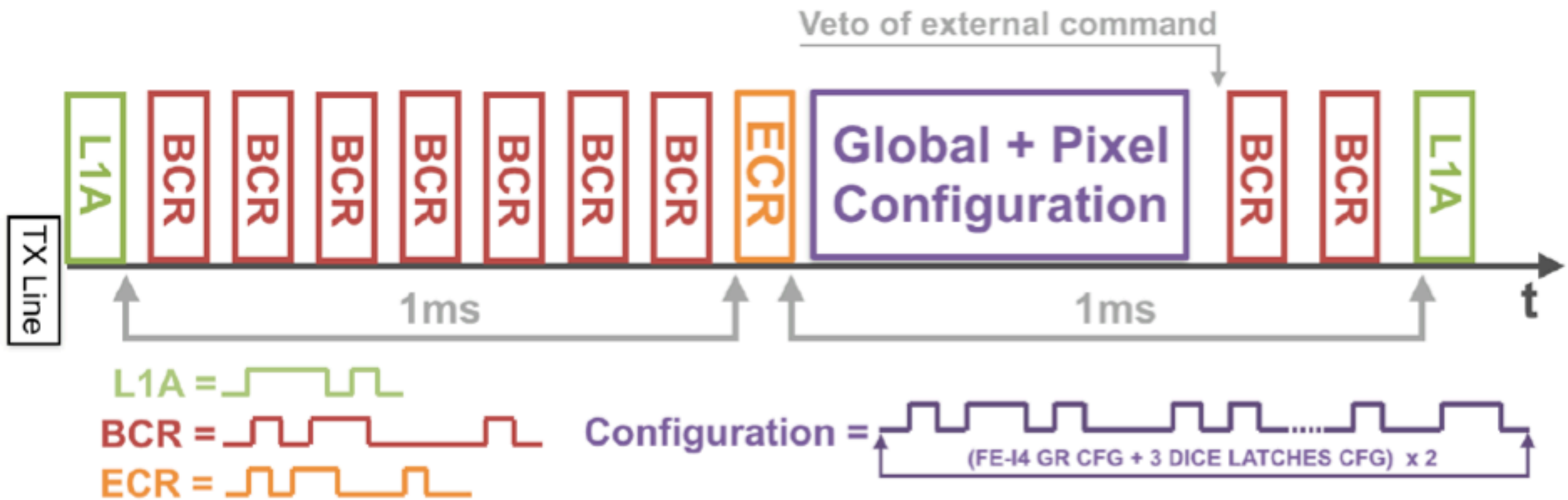


- Read back of the tripled Global Configuration Memory (GCM) during the LHC fill
- 0->1 transitions are dominated by glitches (value of the loaded last register was xFFFF)
- 1->0 transitions not observed, triple memory suppress real SEU

Absolute SEU Cross-sections

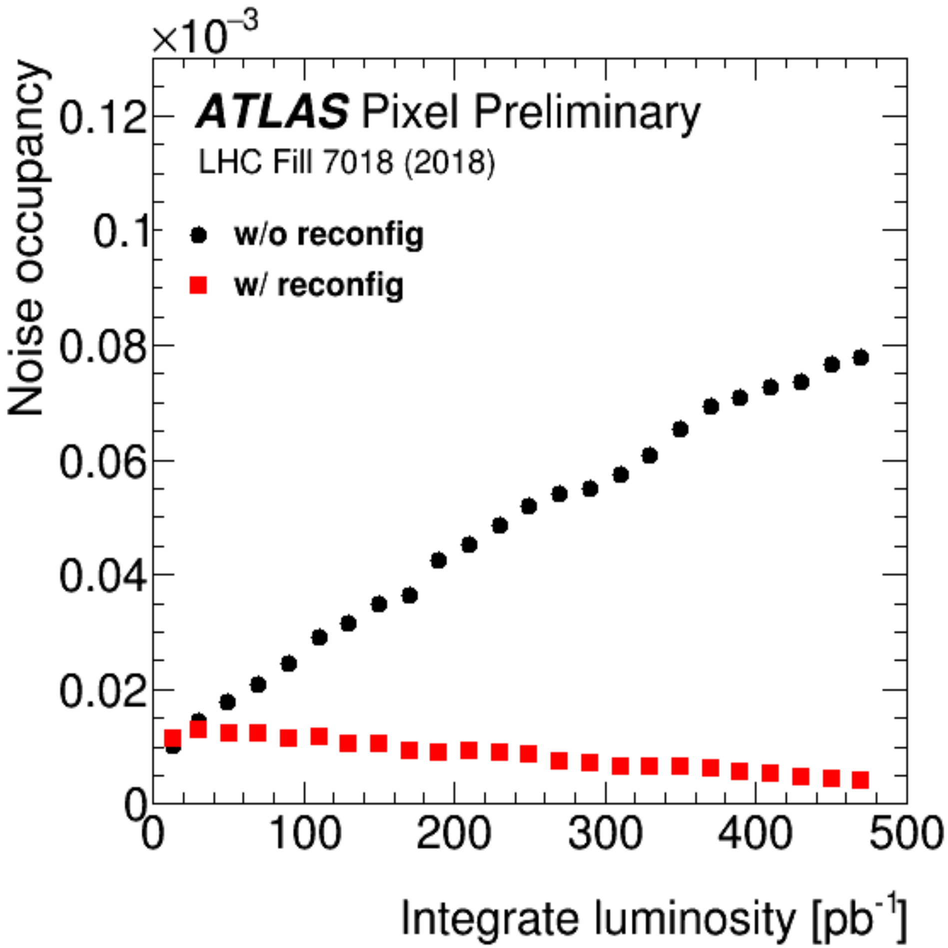
Beam, SEE type	Transition	SR value	Rate per fb^{-1} (stat./syst.)	Cross-section 10^{-15} cm^2
LHC: Mainly SEU	0->1	0	0.22 ± 0.01 ± 0.09 %	0.24 ± 0.13
LHC: Mainly SEU	1->0	1	0.46 ± 0.01 ± 0.19 %	0.51 ± 0.26
LHC: Mainly SET on Load line	1->0	0	3.07 ± 0.02 ± 0.80 %	3.39 ±1.34
LHC: Mainly SET On load line	0->1	1	4.68 ± 0.03 ± 1.21 %	5.16 ±2.04
24 GeV protons: Mostly SEU with some SET admixture	0->1	0	n.a.	1.10

Reconfiguration mechanism



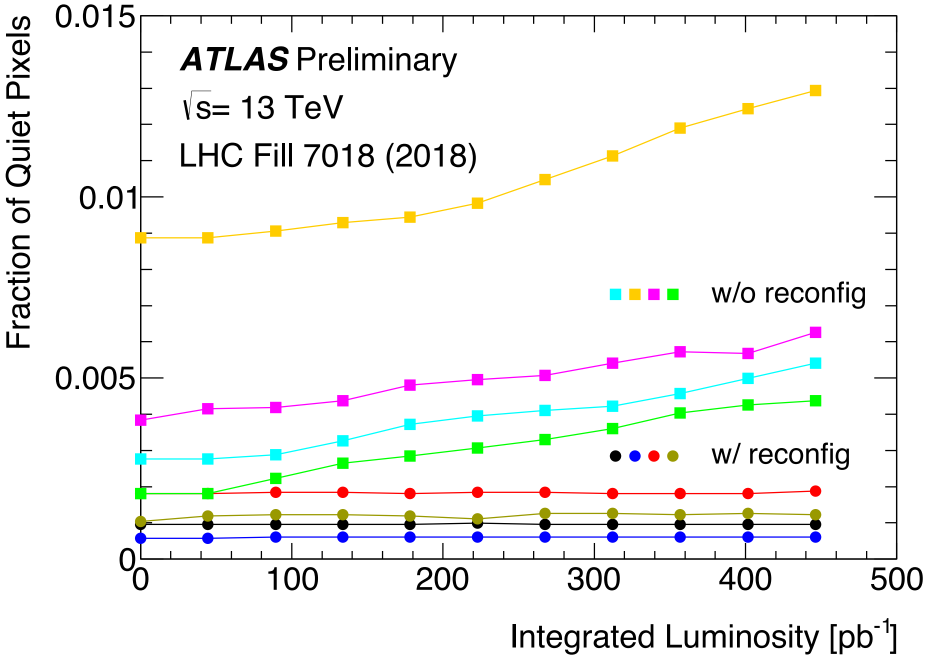
- Global Configuration Memory refreshed periodically since August 2017 : dramatic decrease of silent chips, current jumps, occupancy jumps, de-synchronizations in IBL
- A 2ms time window used by ATLAS to send Event Counter Reset (ECR) signal to detector electronics was exploited to perform such reconfiguration:
  - ATLAS ECR period is 5 seconds
  - Reconfiguration during ECR didn't add any extra dead time to ATLAS
- Bitstreams for local memory reconfiguration are much larger than for Global Configuration Memory => trying by splitting in several ECR cycles => full reconfiguration during 11 minutes
- Local memory refreshing tested in few LHC fills => see results on next slides

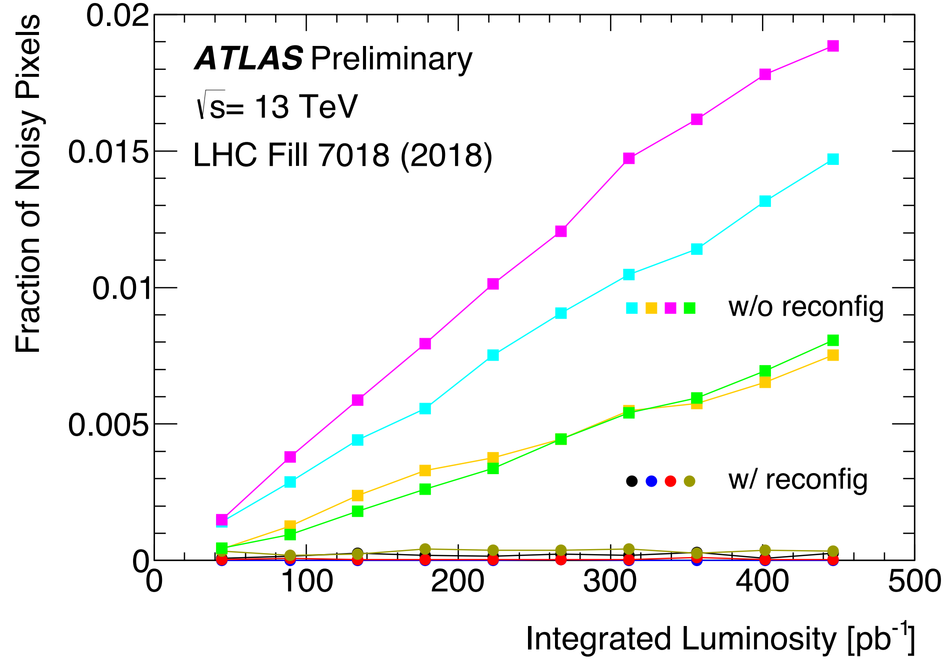
Noise with reconfiguration in test run



- Noise in IBL high η modules with and without reconfiguration
- Decrease of the noise with reconfiguration is due to the more frequent (11 min) refreshing per unit of luminosity

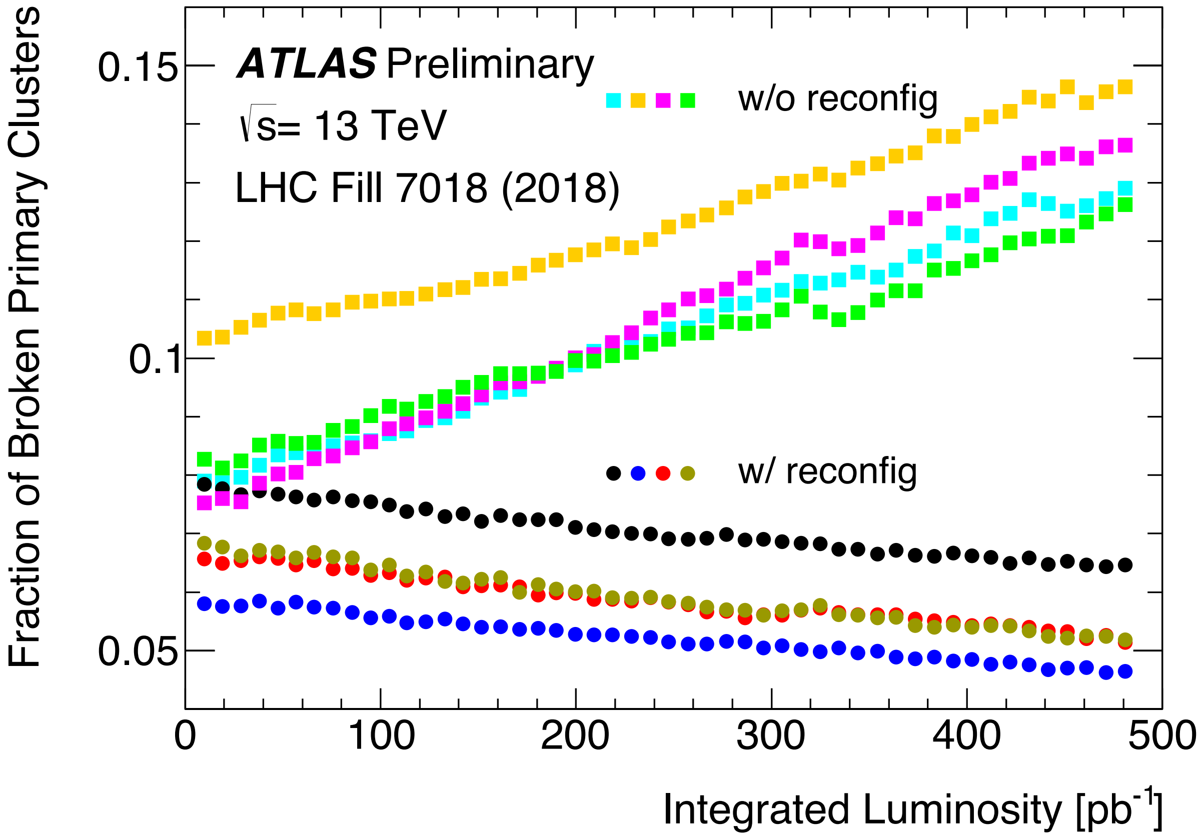
Quite and Noisy with reconfiguration





- Quite and Noisy pixels with reconfiguration in the test run
- Eight high η modules under test: four reconfigured and four not reconfigured

Broken clusters with reconfiguration



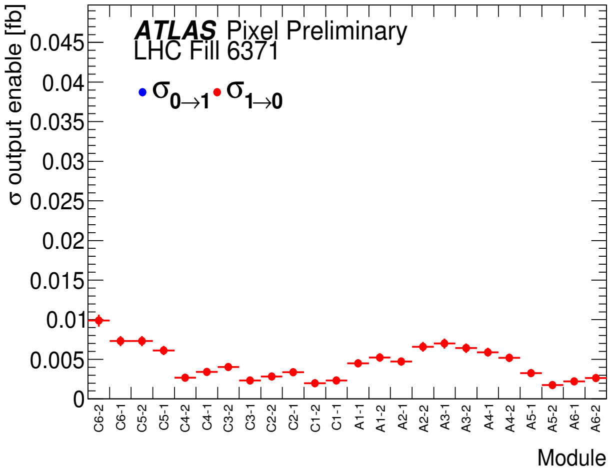
- Fraction of broken clusters with and without reconfiguration

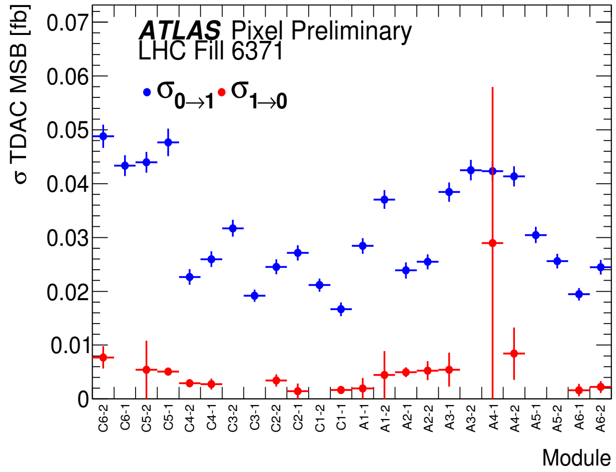
Conclusions

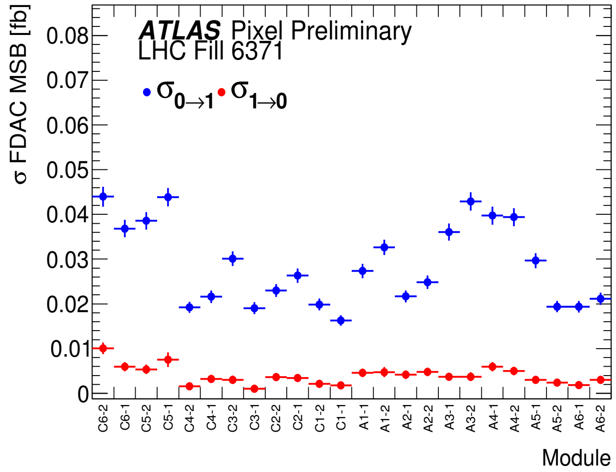
- ATLAS Pixel detector with IBL at R=3.3 cm efficiently operates at high luminosity with expected SEUs.
- SEUs in global memory create silent modules, current jumps, occupancy jumps, de-synchronizations.
- Global Configuration Memory SEUs mitigated in 2017 by refreshing the memory during ECR every 5 seconds without dead time.
- SEUs in Local pixel memory create quiet pixel, broken clusters, noisy pixels.
- Local pixel memory bit flips are dominated by glitches (SET) on the LOAD line of DICE latches.
- During few test runs in 2018 local pixel memory was gradually refreshed during ECRs with the full period of 11 minutes. Complete cure of quiet pixels, broken clusters and noisy pixels due to SET/SEU.
- Plans to fully deploy the gradual refreshing of local pixel memory in IBL FE-I4 during ECR in Run3 in 2021.
- For future pixel FE electronics design: suppression of glitches (SET) could be as important as SEU hardness.
- The tests on 24 GeV CERN PS facility is a good method for SEU/SET measurements and design validation.

Additional

SEU in different local memory bits

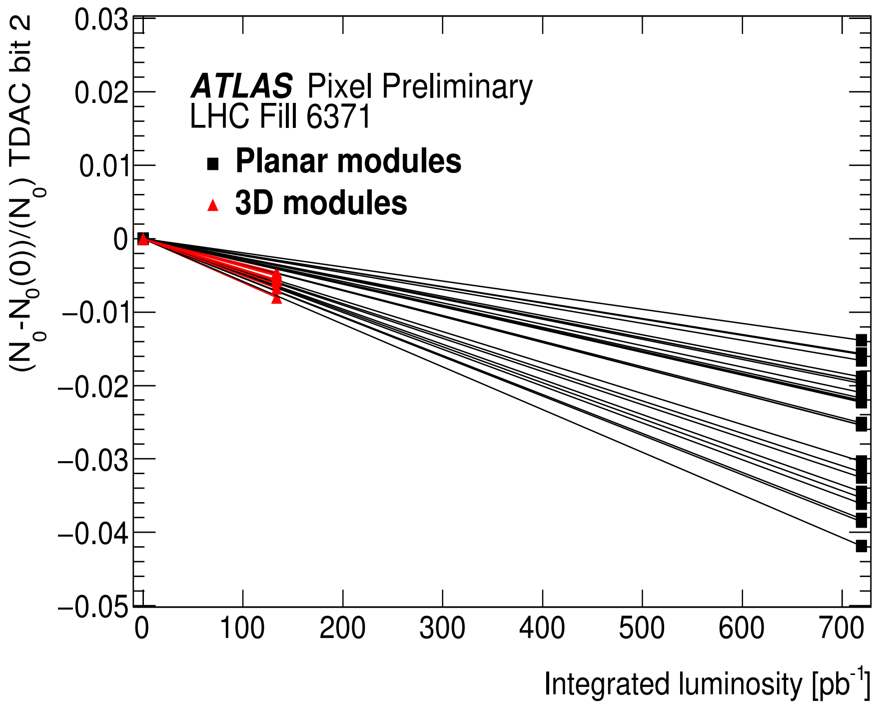


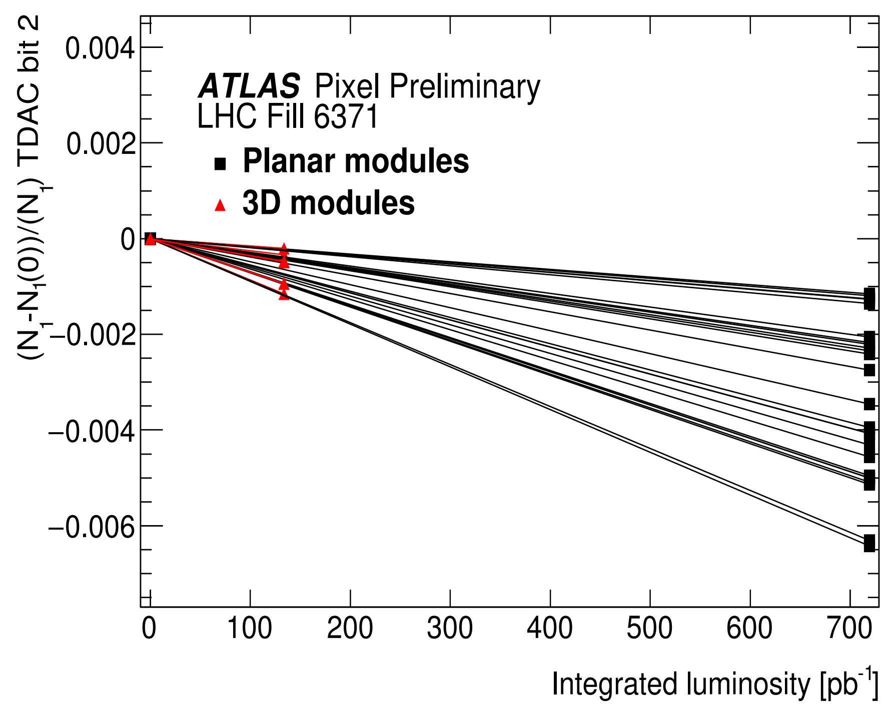




- Variation of SEU in the modules along the stave for “Enable”, “TDAC MSB” and “FDAC MSB” bits with read back method.
- Transitions “1->0” are consistent with test beam results, transitions “0->1” are factor of five higher

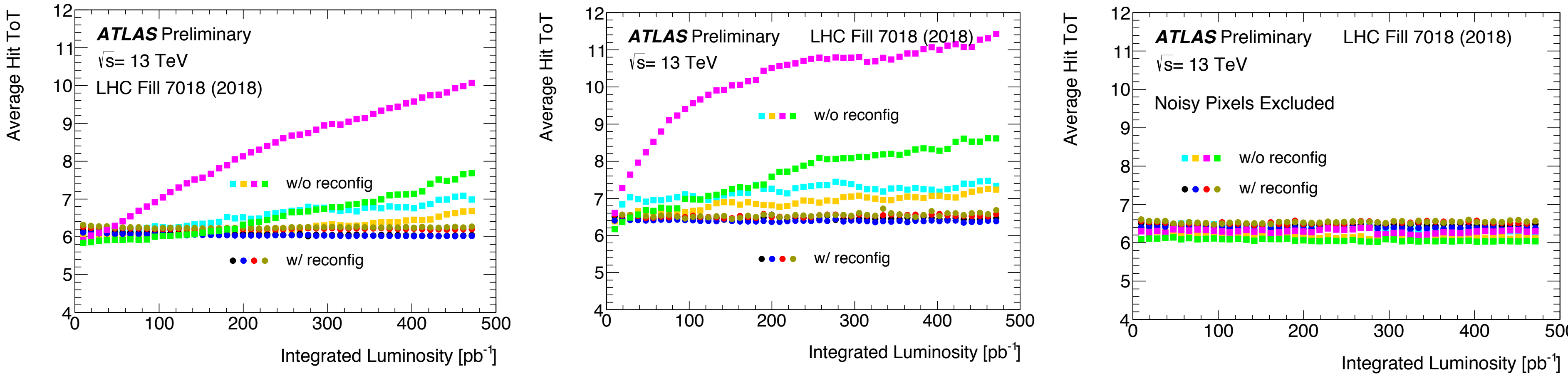
Asymmetry of 0->1 versus1->0 transitions





- TDAC bit#2 transitions 0->1 are more frequent than 1->0 transitions when measured with read back method

ToT vs Luminosity



- ToT vs Luminosity

High η pixel modules used for luminosity mesurements

- Refreshing local pixel memory dramatically reduce the fraction of broken clusters for high η modules.
- Improves the quality of luminosity measurements by counting long pixel clusters