PROCEEDINGS OF SCIENCE

OT-μDTC, a test bench for testing CMS Outer Tracker Phase-2 module prototypes

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The Compact Muon Solenoid (CMS) experiment plans to replace its strip tracker system with a completely new Outer Tracker system to cope with the higher luminosity, compared to Run 2 operation, provided by the HL-LHC. This CMS Phase-2 Outer Tracker will be build up from two types of modules both consisting out of two parallel silicon sensors separated by a few millimetres. To read out the two types of modules four Outer Tracker specific custom chips are required. This proceeding introduces the module concept, goes into more detail on the data path, discusses the test system (OT-μDTC) designed for testing prototypes based on these ASICs and gives examples of test results obtained with this test system.

European Physical Society Conference on High Energy Physics - EPS-HEP2019 -
10-17 July, 2019
Ghent, Belgium

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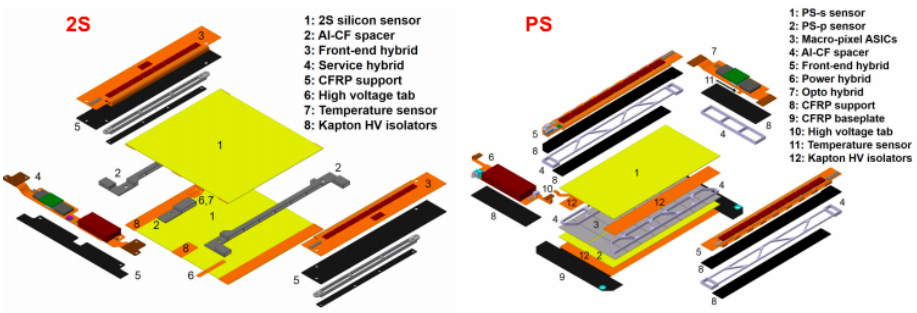
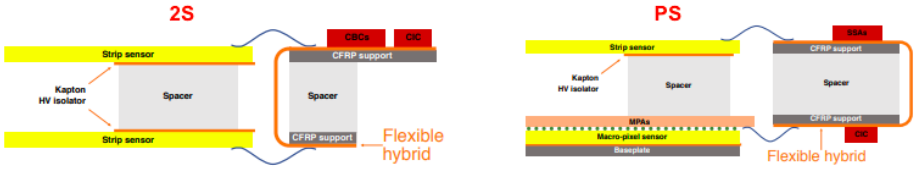
PoS(EPS-HEP2019)170

1. Introduction

The Large Hadron Collider (LHC) at CERN will be upgraded by 2026 to deliver to the experiments a larger instantaneous luminosity by providing a larger number of proton-proton collisions (pileup) per bunch crossing (BX). The CMS tracker system which reconstructs tracks of charged particles needs to be upgraded to provide equal or better performance than the current tracking system in the more hostile environment delivered by the HL-LHC. To attain this a new pixel and Outer Tracker system [1] is being designed and will be installed in the third long shut-down of the LHC. Using a new module design this upgraded tracker will provide trigger primitives for the L1 trigger system.



(a)



(b)

Figure 1: Exploded (TOP) and transversal cut (BOTTOM) of a 2S and PS module.

The Outer Tracker (OT) will consist out of two types of 'p_T-modules': pixel-strip (PS) and strip-strip (2S) modules. The PS modules consist of a macro-pixel and strip silicon sensor. The 2S modules consist of two strip sensors. In both modules the sensors are stacked, separated by a few mm. The PS and 2S modules are shown in Figure 1.

The PS strip sensor is wire-bonded to two flexible boards (front-end hybrids) each hosting eight SSAs (Short Strip ASIC [2]). 8 chips are bump-bonded on a single front-end hybrid. The macro-pixel sensor is read out by sixteen MPA (Macro Pixel ASIC [3]) chips where each of the macro-pixels is bump-bonded to one of the chip inputs. The sensor+MPAs assembly is referred to as MaPSA (macro-pixel sub assembly) and is connected to the front-end hybrids through wire-bonds. In the 2S module the two top and bottom sensors are wire-bonded to one front-end hybrid per side: 8 CBCs (CMS Binary Chip [4]) are bump-bonded on each front-end hybrid.

In both 2S and PS cases a CIC (Concentrator Integrated Circuit [5]) chip which receives data from the front-end chips also sits on the front-end hybrid. Both front-end hybrids are connected to

a single service hybrid in the 2S case or two service hybrids in the PS case. The service hybrids provide powering and optical interface to the back-end through the lpGBT (Low-power Gigabit Transceiver) and VTRx+ (Versatile TRansceiver plus).

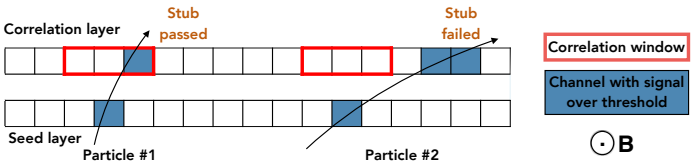


Figure 2: Illustration of the stub concept: particles generating a hit in the 'correlation layer' which is inside the 'correlation window' (indicated by red squares in the figure) will result in a stub being produced by the front-end chip's correlation logic.

The double sensor design gives these p_T-modules the unique ability to correlate hits in the top and the bottom sensor reconstructing a local track 'stub'. The stub concept is explained in Figure 2: when a hit is detected in the 'seed' layer a hit is searched in the 'correlation' layer and when a hit is found within a user defined correlation window a stub data packet is created in the ASIC's logic. For a given sensor separation and magnetic field strength a certain size of the correlation window will correspond to a certain p_T (transverse momentum). Stubs will be sent out synchronously from the module and the stub information from all p_T modules is used in the Level 1 (L1) track finder to reconstruct high momentum tracks and to provide tracking information to the central L1 trigger system. When the central L1 trigger system decides an event is interesting a L1-accept (L1A) is sent back to the tracker modules where the full event information is stored for 512 bunch crossings in the on-chip memory of the front-end chips. When the L1A is received the front-end chips send out the full-event information. This asynchronous data stream eventually goes to the CMS central DAQ (Data AcQuisition).

The full module data path for both PS and 2S modules is shown in Figure 3. The lpGBT is the master of all the ASICs sitting on the module. Each ASIC is controlled by a dedicated link, the 'fast command' line, which can be used to send commands with BX time resolution (e.g. L1A trigger). The ASICs are configured through an I^2C protocol. The data flow is described below for both PS and 2S modules:

- **PS:** Each of the 16 SSAs (8 per front-end hybrid) receive data from 120 channels of the PS strip sensor. The SSA handles the raw signal from the sensor in a dedicated front-end, digitizes the signal if it is above threshold, saves the full event information in a 512 BX deep memory, sends the full event data to the MPA on reception of a trigger, forms clusters and sends these at BX rate to the MPA. The MPA receives data from 1920 macro-pixels, digitizes the hits and correlates these hits with clusters from the SSA to form the stubs. Five stubs can be output by the MPA over two BXs. These stubs are sent to the CIC. The MPA also sparsifies the strip and pixel sensor full event information on reception of an L1A (Level1 accept) trigger. The CIC serialises and forwards the L1 data packets from the MPA to the lpGBT, it selects up to 40 stubs with the highest p_T from eight consecutive BXs and forwards these to the lpGBT.

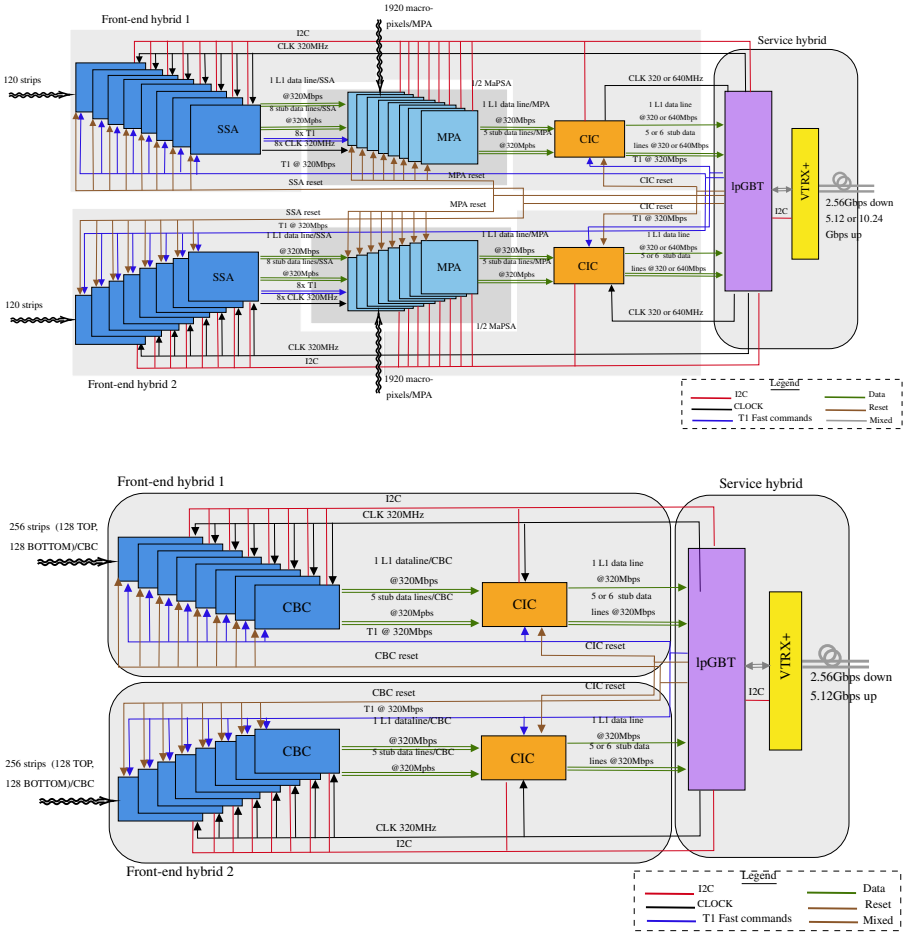


Figure 3: Illustration of the DAQ related inter-chip connections in a PS (TOP) and 2S (BOTTOM) module.

- **2S:** Each of the 16 CBCs (8 per front-end hybrid) receives signals from 127 top and 127 bottom strips. The CBC front-end digitizes the hits and the stub logic correlates hits in the top and bottom sensors. Three stubs can be output by a single CBC per BX. The full event data is stored in the on-chip memory for 512 BXs. The stub data from all CBCs on a front-end hybrid is sent to the CIC which aggregates stub data from eight consecutive bunch crossings and selects the highest p_{T} stubs. In the default configuration the CIC will select the 25 stubs with the highest p_{T} from eight consecutive BXs and forward these to the lpGBT. The CIC furthermore receives the L1 data from eight CBCs. The L1 data can be sparsified or left untouched and is then serialised to be sent out.

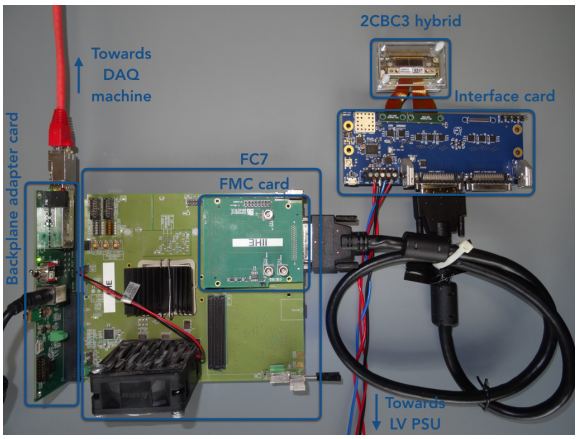
In both modules the lpGBT in the end receives the data from two CICs, one for each side of the module.

During prototyping and production of the p_{T}-modules a test system is required to test and validate (prototype) single chips, (prototype) front-end hybrids and (prototype) modules. This test system, referred to as 'μDTC' (micro Data, Trigger and Control), is based on the μTCA FC7 [6]

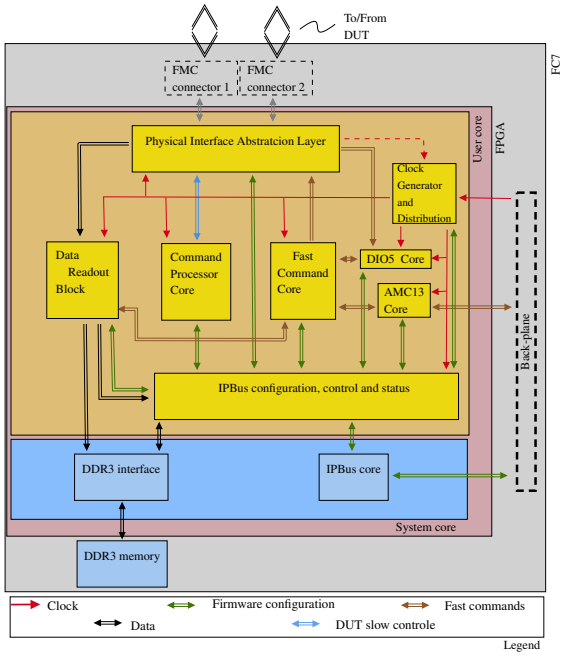
data acquisition and control card with as a center piece a Kintex7 FPGA. The firmware running on the FPGA needs to be adapted for each hardware set-up.

2. OT-μDTC test system

A typical μDTC set-up is shown in Figure 4a where the FC7 is connected through an adapter card with a DAQ PC, and an FMC (front-end mezzanine card) provides the electrical connection to the DUT (Device Under Test) specific interface card. The DUT shown in this figure is a prototype hybrid carrying two CBC chips.



(a)



(b)

Figure 4: LEFT: Example of a typical μDTC set-up for prototype testing. RIGHT: Top level view of the μDTC firmware structure.

The block structure of the μDTC firmware is shown in Figure 4b. The OT-specific firmware is implemented alongside the FC7 system firmware provided by the FC7 team. This system firmware e.g. allows interfacing with peripheral devices on the FC7. The main OT-specific blocks are:

- The Physical Interface Abstraction Layer ('Phy layer'): the last physical border between the firmware and the front-end. In this layer DUT-specific protocols are implemented and the DUT-specific data format is generalised to a data format which can be used cross-DUT and can be handled by the downstream firmware blocks. The presence of this layer allows reusing with minor changes the other firmware blocks for different DUTs. This is a requirement for a firmware project aimed at reading-out, controlling and configuring different devices. A phase alignment procedure is also implemented here: the firmware implements the clock source for the DUT, but the firmware does not know the clock phase of the data from the DUT. Therefore the incoming data needs to be delayed (using IDELAY resources) to sample

the input signals in the middle of their bit period (Unit Interval), avoiding the region around the bit level crossing points.

- Clock Generator and Distribution: generates the clocks for the firmware blocks and for the DUT. Most firmware logic is running at 40 MHz ($\approx$ the BX frequency) the DUTs are clocked at 320 MHz. Some parts of the firmware run at higher frequencies to save on resources.
- IPBus configuration, control and status: the IPBus protocol [7] is a register mapped IP protocol. The μDTC implements IPBus registers which allow for configuration, control and status checks of the firmware and indirectly of the DUT. The protocol is also used to offload the data to the DAQ PC.
- Data Readout block: receives both the stub and the full event data from the Phy layer. The stub data is delayed in this block and only stub data with a programmable time-offset with respect to the L1A trigger is buffered. This allows for the synchronisation of stub and full event data such that an event can be built. The events can be buffered for readout in FIFOs on the FPGA or can be offloaded to an external DDR3 memory.
- Command Processor Core: this block receives and buffers control and configuration commands in the IPBus format, interprets these commands and sends the necessary instructions to the Phy layer where they are translated to device specific protocols e.g. I^2C.
- Fast Command Core: this block is responsible for the generation of the fast commands (fast reset, L1A trigger, orbit reset and test pulse trigger). Several state machines are implemented which allow e.g. sending a certain amount of 'test pulse trigger-L1A trigger' sequences with a well defined time resolution and repetition rate.

3. Test results with the OT-μDTC

This section describes some of the test results obtained with the OT-μDTC test system. Two results from test beams of prototype modules and two results from irradiation testing of ASICs are presented.

3.1 2S mini-module test beam

A 2CBC3 mini-module was tested at the FNAL FTBF test beam area. The OT-μDTC was used to control and configure the device and also interfaces with the trigger and clocking infrastructure in the test beam area. The 2CBC3 mini-module with sensor separation $\approx$ 1.6 mm was tested under several conditions: different data latency settings, different thresholds, different bias voltages and different incident angles. The latter scan allows for testing of the stub reconstruction efficiency with respect to p_{T} as the non-zero incident angle mimics a bend of a particle in a magnetic field. The stub reconstruction efficiency versus p_{T} is shown in Figure 5 where a correlation window of $\pm$ 5 strips was used. The p_{T} is calculated for a module placed at a radius (R) of 71.5 cm using the following equation:

$$p_{\mathrm{T}}[\mathrm{GeV}] \approx \frac{0.57R[\mathrm{m}]}{\sin(\alpha)} \tag{3.1}$$

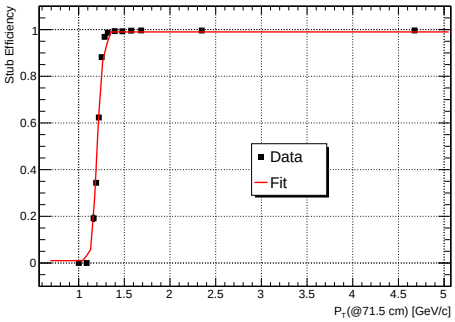


Figure 5: Stub efficiency turn on curve for a 2CBC3 mini module.

for a particle with an incident angle α and unit electric charge in the CMS magnetic field with a strength of 3.8 T. A sharp turn-on curve can be seen: below a p_{T} of about 1.2 GeV particles do not generate any stubs.

3.2 MaPSA test beam

A 'single MaPSA' was tested at the CERN North Area. The single MaPSA consists of a baby PS pixel sensor bump bonded to a single MPA chip. The test beam allowed for testing of the sensor layout, the chip's functionality and the DAQ. Figure 6 shows the efficiency map for four macro pixels. Along the middle of the long pixel dimension an inefficient region can be seen. This inefficiency is related to the bias rail at this location. The additional 'dots' of inefficiencies in each macro-pixel are due to the punch-through regions which are present to bias the macro-pixels. New sensor layouts are under investigation [8] for which these inefficiencies are minimised. Furthermore these inefficiencies get reduced for non perpendicular particle incidence.

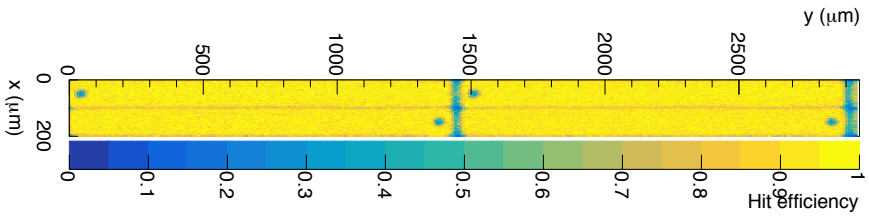


Figure 6: Inpixel efficiency for 4 macro pixels of a single MaPSA assembly. This is obtained by folding the data from the studied part of the single MaPSA assembly to increase the statistics inside the pixels.

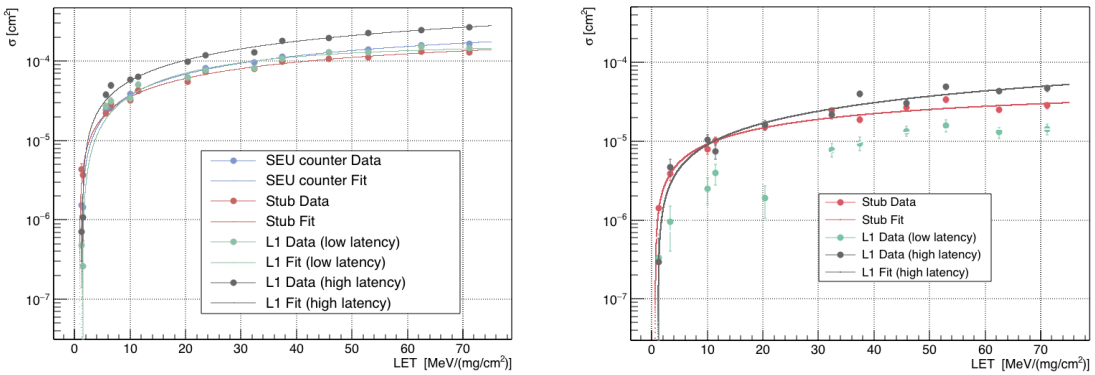
No stub information was available in this test beam as only one sensor is used. A dedicated MPA+SSA test card on which an MPA and SSA are interconnected was used to validate the fact that the MPA and SSA can operate together.

3.3 SSA and MPA SEU testing

In order to be used in an LHC experiment, the ASICs have to be validated for operation in a

high radiation environment. The ASIC's sensitivity for single event upsets (SEU) and Total Ionising Dose (TID) (see section 3.4) have to be tested.

The MPA and SSA adopt triplicated control and configuration logic to mitigate the effect of SEUs. No triplication is applied on the data path. SEU sensitivity of the MPA and SSA was tested at the UCL cyclotron facility using a heavy ion beam. During irradiation of the MPA and SSA with different types of ions, all having a specific energy deposit in silicon, the error rate on both data streams (full event and stub data stream) and upsets in the configuration logic were checked. Given the limited IPBus bandwidth it is not possible to transfer the full stub and full event data streams to the DAQ PC. To take full advantage of the time available in the beam the incoming stub and full event data were compared to user defined reference patterns in a specifically designed firmware block. This allows to verify the stub data at 40 MHz rate and the L1 data at 1MHz. If a data packet does not match the reference pattern the packet is stored and the faulty packets can be read out at the end of a run. Using test pulse injection at the input of the ASIC's digital logic the user can configure different output patterns. To test all the ASIC logic the firmware also supplies emulated data from neighbouring SSA chips to the SSA under test and it provides emulated SSA-like stub and full event data to the MPA under test.



(a) (b)

Figure 7: SEU cross sections at different LET for the MPA (LEFT) and SSA (RIGHT) chip

The results of the SEU tests are shown in Figure 7a and 7b where the SEU sensitivity is expressed as a cross section in function of the Linear Energy Transfer (LET) of the used ions. The data points are fitted using a Weibull distribution. This result can now be used to calculate the upset rate in the LHC environment by convoluting the Weibull distribution with computational distributions provided in Ref. [9]. These distributions give the probability to have, within a volume of $1\times1\times1\ \mu m^3$ of silicon, an ionizing deposition greater or equal than a certain LET for the particle spectrum at the LHC. This then allows for an order of magnitude estimation of the expected bit error rate due to SEU in the LHC radiation environment. The bit error rate on both data paths for both the MPA and SSA were estimated to be in the range of $\mathcal{O}(5\times10^{-4})$ bit-upset/s/chip for HL-LHC operation.

The heavy ion irradiation also revealed some improvements to be implemented in the triplication of the control and configuration logic. These improvements will be implemented in a future

iteration of the MPA and SSA.

3.4 CIC1 TID testing

As stated in the previous section the sensitivity of an ASIC to Single Event Upsets is only part of the work of validating it for usage in the LHC environment. The ASIC also has to be validated for the total integrated dose it will receive and the damage this can induce on the operation of the transistors.

TID testing of the CIC1 was performed in an X-ray beam. The CIC1 was tested stand-alone in the beam and was stimulated with CBC-like full event and stub data from the OT-μDTC. However, before being ready to receive this data an initialisation procedure, consisting of phase, word and BX0 alignment, has to be performed. The phase alignment guarantees that the CIC1 will be sampling the incoming data at the 'middle' of the bit Unit Interval while the word alignment procedure guarantees that the CIC selects the correct start of the byte (the CIC receives 8 bits on each input data line every BX). The BX0 alignment procedure verifies the CIC1 feature to identify the BX it will use as the first one (BX0) after the issuing of a resync. The routine of phase, word and BX0 alignment followed by data playing is repeated throughout the irradiation and results are saved to the DAQ machine for later analysis.

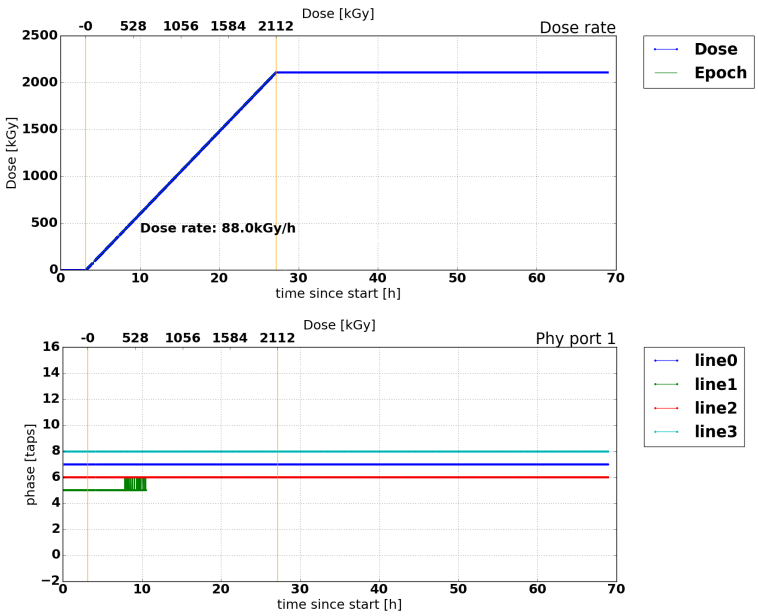


Figure 8: Optimal phase taps found for four out of 48 input lines of the CIC1.

A result of the CIC1 TID test is shown in Figure 8 where the left figure shows the dose acquired by the CIC1. The total dose attained was 2.1 MGy, which is well above the 1 MGy maximum expected dose for HL-LHC operation. The right figure shows the result of the optimal tap found by the phase tuning algorithm throughout the irradiation for four out of the 48 input data lines to the CIC. The phase shift observed on line 1 is only one phase tap which corresponds to 390 ps. Shifts like this can be expected and are also seen when the CIC1 is not under irradiation. The phase,

word and BX0 alignment was successful throughout the irradiation for all input data lines. Also no radiation dependent upsets in neither of the data streams was observed.

4. Conclusion

CMS is preparing for the construction of a completely new tracker system for operation at HL-LHC. The Outer Tracker will consist out of p_{T} modules which will provide full event information and input to the L1 trigger system. In order to accomplish this several ASICs will be used which will buffer the full event information as well as generate the primitives for the L1 track finder. The Outer Tracker specific ASICs (MPA, SSA, CBC and CIC) and module prototypes require a dedicated test bench for testing single chips, prototype assemblies and components and final objects during production. The first interface to these DUTs is the OT-μDTC firmware which controls and configures the DUT and handles the DAQ. Results from test beams with a CBC based mini module and with a single MaPSA as well as results from irradiation tests of MPA, SSA and CIC obtained with the OT-μDTC were presented.

References

[1] Collaboration, CMS, "The Phase-2 Upgrade of the CMS Tracker", CERN-LHCC-2017-009. CMS-TDR-014, https://cds.cern.ch/record/2272264

[2] A. Caratelli et al., "Short-Strip ASIC (SSA): A 65nm Silicon-Strip Readout ASIC for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC", PoS(TWEPP-17)031

[3] D. Ceresa et al., "Design and simulation of a 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector at the HL-LHC", PoS(TWEPP-17)032

[4] D.G. Cussans et al., "Tests with the CMS Binary Chip (CBC)", 2012, JINST 7 C03016

[5] B. Nodari et al., "A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC", PoS(TWEPP2018)099

[6] M. Pesaresi et al., "The FC7 AMC for generic DAQ & control applications in CMS", Journal of instrumentation, 10.03 (2015), pp. C03036-C03036, https://doi.org/10.1088%2F1748-0221%2F10%2F03%2Fc03036

[7] C.G. Larrea et al., "IPbus: a flexible Ethernet-based control system for xTCA hardware", Journal of instrumentation (2015), https://doi.org/10.1088%2F1748-0221%2F10%2F02%2Fc02019

[8] D. Schell, Development of a Macro-Pixel sensor for the Phase-2 Upgrade of the CMS experiment, Doctoral Thesis, ETP-KA 2016-6, KIT, 2019

[9] M. Huhtinen et al., "Computational method to estimate Single Event Upset rates in an accelerator environment", Nuclear Instruments & Methods in Physics Research, section A, https://doi.org/10.1016/S0168-9002(00)00155-8