The Prototype Hardware Design of Global Common Module for Global Trigger System of the ATLAS Phase-II Upgrade on HL-LHC

Shaochun Tang

Onbehalf of the ATLAS TDAQ Collaboration

2020 NSS/MIC Conference

BROOKHAVEN NATIONAL LABORATORY

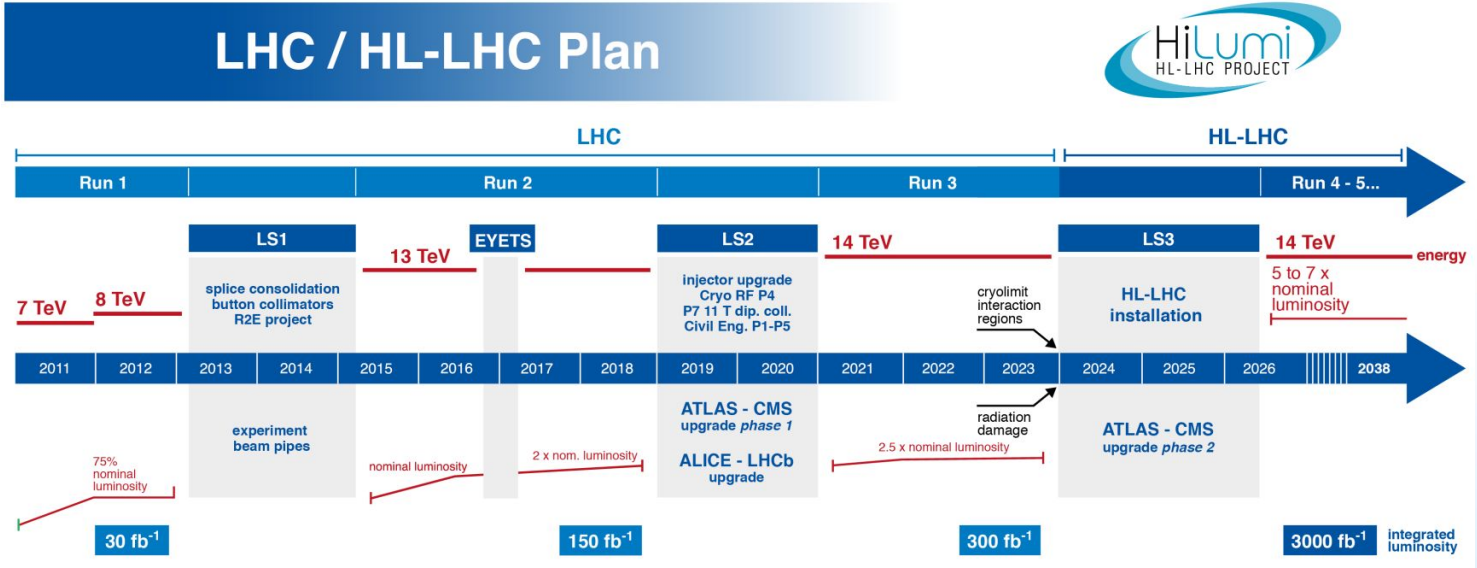
a passion for discovery

U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- *An Introduction of LHC/HL-LHC*
- *An Overview of ATLAS Experiment and Level-0 Trigger System*
- *Global Trigger System*
- *Global Common Module Hardware Design*
- *Global Common Module Status*
- *Summary*

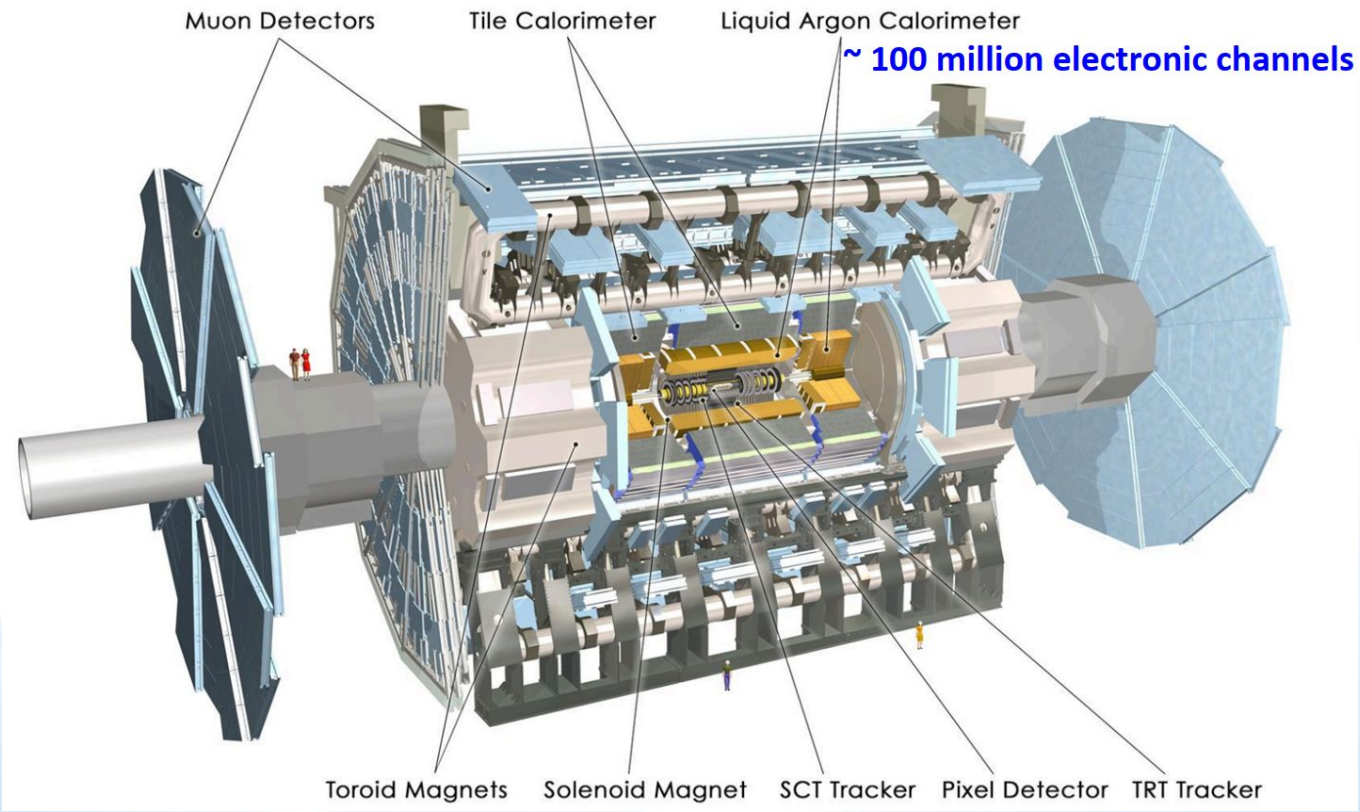
The Large Hadron Collider: LHC/HL-LHC



- *The world's largest and most powerful particle accelerator*
- ***Physics motivation**: Higgs particles (2013 Nobel Prize in Physics)/Dark matter and dark energy/Supersymmetric particles*
- *The **Phase II upgrade will be installed in the Long Shutdown 3 (2025-2027)**, and operating in Run 4-5 (2027 to 2039). **5-7 x nominal luminosity**.*

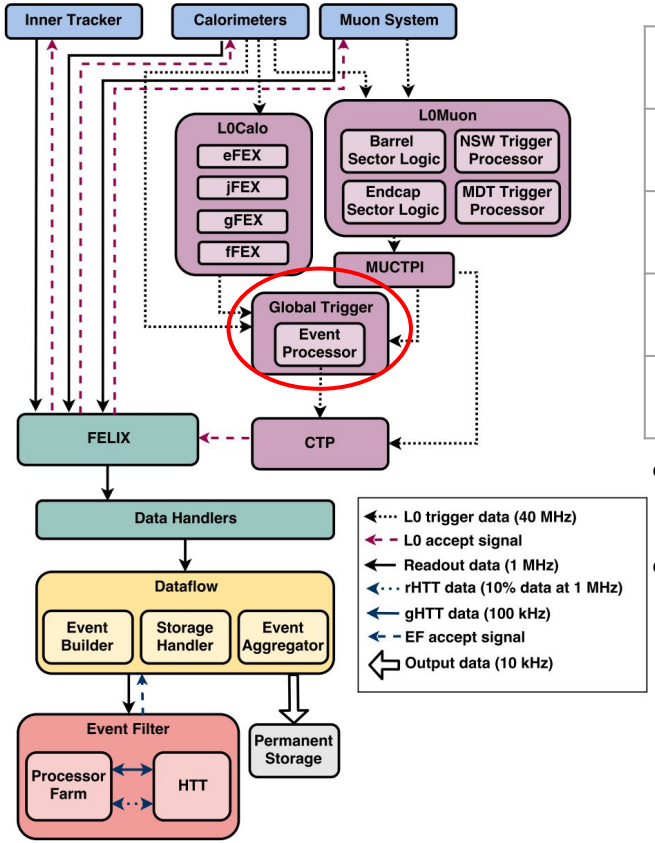
Quoted from :https://hilumilhc.web.cern.ch/content/hl-lhc-project

The ATLAS Experiment



- *ATLAS consists of several sub-detectors.*
  - Inner Tracker
  - Tile Calorimeter
  - LAr Calorimeter
  - Muon

ATLAS Trigger in Run 4 (After Phase-II Upgrade)



Level-0 trigger data	40.08 MHz (BC=25 ns)
Level-0 accept trigger rate	1 MHz
Level-0 accept trigger features	≤4 in 5 BC; ≤4 in 20 BC
Level-0 latency	10 μs
Deadtime	< 0.1%

- The Level-0 Trigger utilizes custom hardware featuring large FPGA for the calorimeter, muon, and central systems.
- The **Global Trigger** is a new subsystem
  - perform offline-like algorithms on full-granularity calorimeter data
  - identify topological signatures, replace and extend the functionality of the Level-1 Topological (L1Topo) system
  - receive all trigger information from legacy systems
  - send processed trigger information to Central Trigger Processor (CTP) for final decision

Quoted from :https://cds.cern.ch/record/2285584/files/ATLAS-TDR-029.pdf

Global Trigger System - Nodes

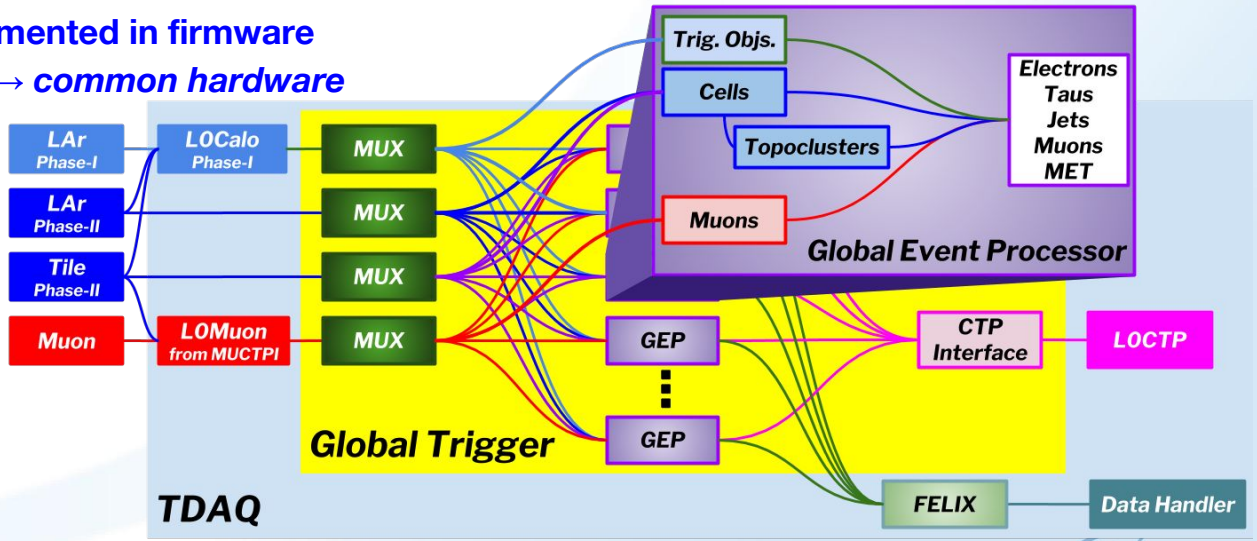
- ***Concentrates data for full event onto single processor for analysis at 40 MHz***
  - approx. **60 Tb/s** into Global Trigger
    - exploits data aggregation and **time multiplexing**
  - **primarily a firmware project**
    - **different functions implemented in firmware rather than in hardware → *common hardware***

GCM: Global Common Module

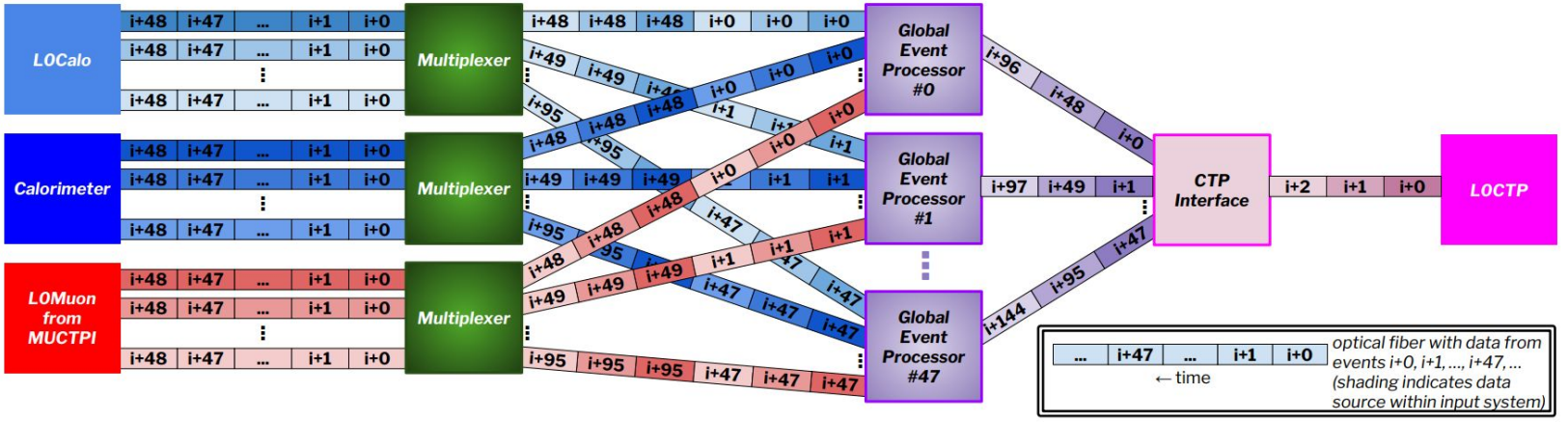
MUX: GCM Node for data aggregation & time multiplexing

GEP: GCM Node for event processing & trigger algorithms

CTPi: GCM Node for CTP Interface (runs on a MUX Node)



Global Trigger System - Data Flow



- With the basic configuration of 48 GEP.
  - All the trigger event of the same bunch crossing from different detectors will be send to the same GEP for processing.
  - All the processed trigger information will be sent to CTP for final decision.

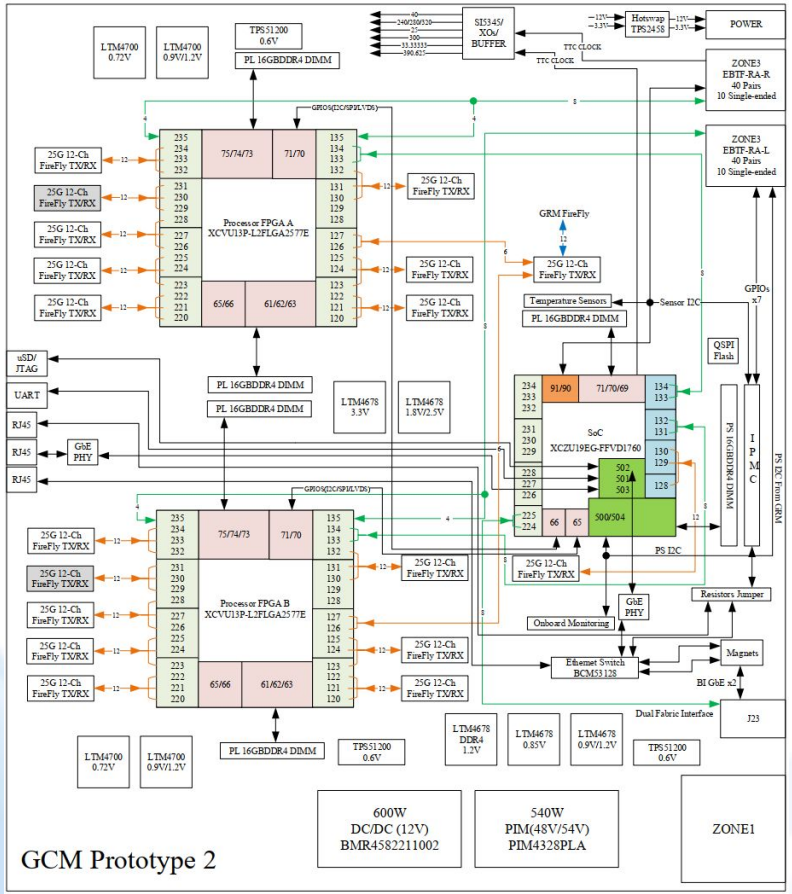
GCM Hardware Requirements

- Based on successfully experience in Phase-I projects in ATLAS, ATCA platform is adopted.
- Power limitation from ATLAS ATCA chassis. Front board <350W, RTM < 50W
- Each Node needs at least 84 MGT links @ 25.78125 Gb/s.
- Large FPGA resources are required for GEP node
- >25Gb/s Optical modules are required

Input/Output Connections for GCM			
Node	**MUX**	**GEP**	**CTPi**
Input (per Node)	72 Rx detector	72 Rx from MUX	72 Rx GEP
Output (per Node)	Up to 72 Tx to GEP	1 Tx CTPi	12 Tx CTPCORE
Internal (per Node)	8 x 25 G	8 x 25 G	8 x 25 G
Command/Control/Readout (per blade)	4 Rx from FELIX 4 Tx to FELIX	4 Rx from FELIX 4 Tx to FELIX	4 Rx from FELIX 4 Tx to FELIX

- Based on the number of MGTs, resources, and power consumption, etc. The Xilinx VU13P is chose as the MUX/GEP/CTPi node; the ZYNQ UltraScale+ FPGA is chosen as Command/Control Unit (CCU).
- To mitigate power risk, a RTM named GRM with one SoC FPGA is being designed.

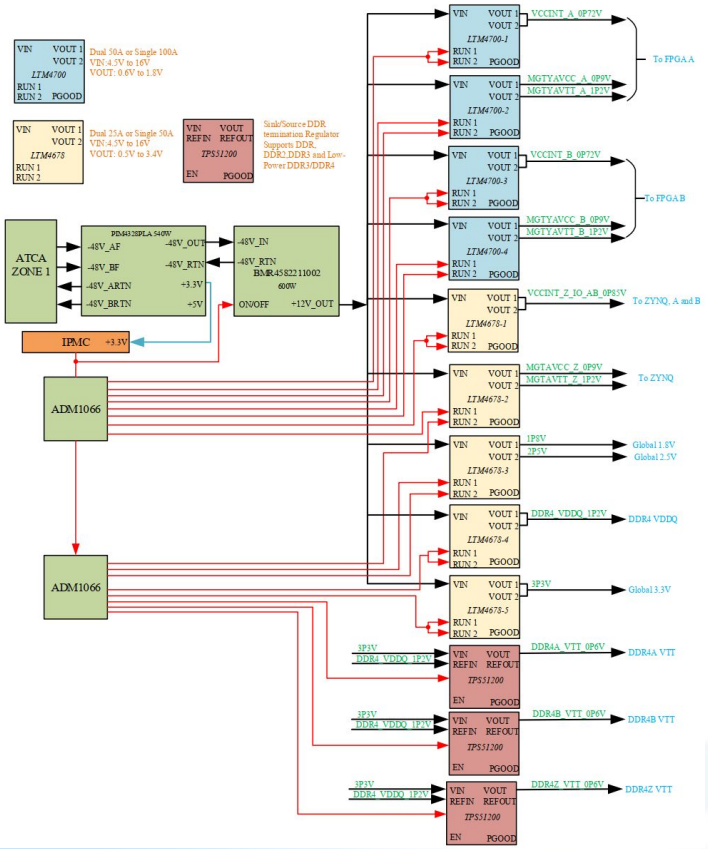
Block Diagram of GCM Hardware Design



Main components/functions:

- **2** XCVU13P-L2FLGA2577 FPGA (Processor Node) and **1** ZU19EG-2FFVD1760 (CCU)
- **1** J23 at ZONE 2 for GbE and Fabric interface
- **1** GbE Ethernet switch
- **1** RJ45 to IPMC/GbE SW/ZYNQ+ PS (Total **3**)
- **1** SD/ **2** QSPI/ **1** UART to ZYNQ+ PS
- **8** Pairs of Firefly to each Processor Node
- **1** pair Firefly to ZYNQ+ GTY
- **1** pair Firefly to RTM for backup
- **2** DDR4 VLP DIMM to each FPGA (Total **6**)
- **1** Power/**2** EBTF-RA connector at ZONE 3
- Hot Swap support for GRM (by defaut **8A** is maximum)
- **1** CERN IPMC is planned to be used
- **2** SI5345 are used for LHC clock and 156.25MHz clock respectively

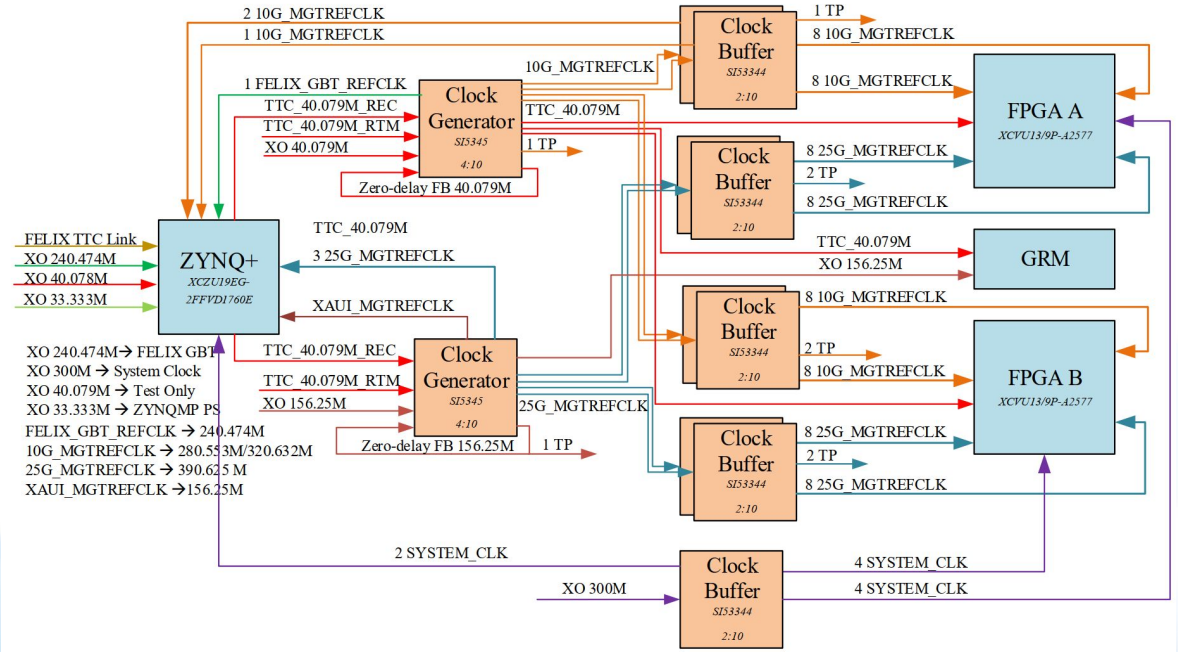
Power Design of GCM



Power on sequence of GCM Demonstrator				
First	Second	Third	Forth	Fifth
VCCINT_A_0P72V	VCCINT_IO_A_0P85V	1P8V	2P5V	DDR4_VDDQ_1P2V
VCCINT_B_0P72V	VCCINT_IO_B_0P85V		3P3V	DDR4A_VTT_0P6V
VCCINT_Z_0P72V	VCCINT_IO_Z_0P85V			DDR4B_VTT_0P6V
MGTYAVCC_A_0P9V	MGTYAVTT_A_1P2V			
MGTYAVCC_B_0P9V	MGTYAVTT_B_1P2V			
MGTAVCC_Z_0P9V	MGTAVTT_Z_1P2V			

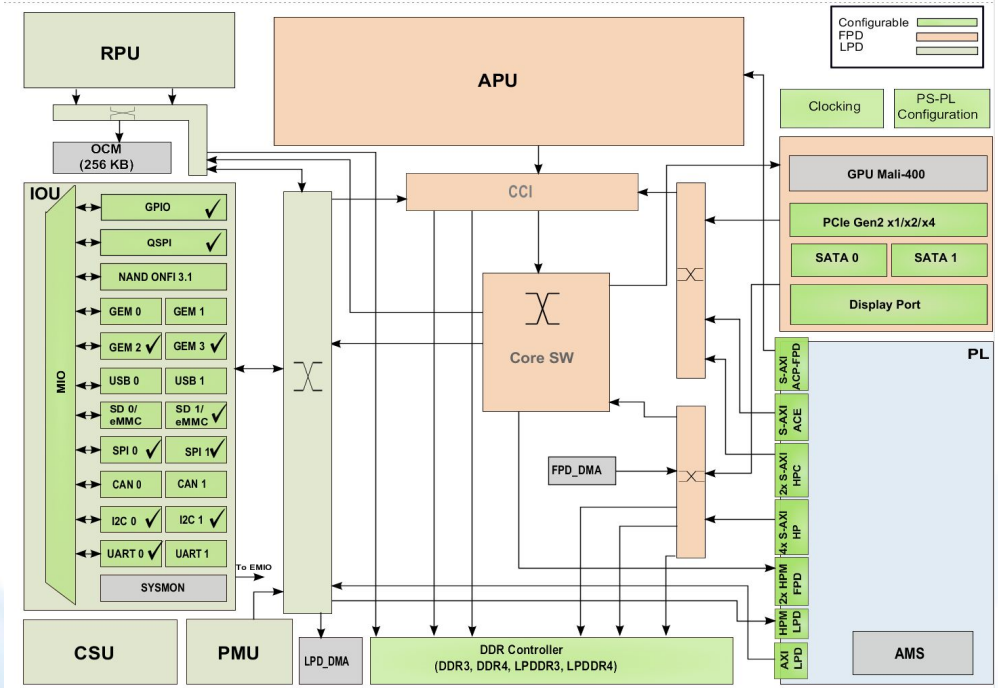
1. Separate core power rails for three FPGA
2. ADM1066 is used to monitor UV/OV and control the power sequence required by VU13P/ZYNQ+ FPGAs
3. IPMC and ADM1066 are used to control the +12V together

Clock Distribution



- **2** SI5345 used to generate different required clock frequencies from different clock sources. Clock sources can be LHC clock from ZYNQ+ or GRM or XO156.25MHz
- **9** SI53344 used to buffer the clocks
- Clock frequencies should support different data rate for Processor Nodes/FELIX (Possible 9.6/10.24/11.2/12.8/14?/25.78125 Gb/s)
- 300M XO for system use, like DDR4 DIMM controller, IDELAY, etc.
- 33.333MHz for ZYNQMP PS
- 240.474MHz XO for FELIX TTC receiver links
- 156.25MHz XO for 25.78125Gb/s reference clock source

ZYNQ+ PS Interfaces

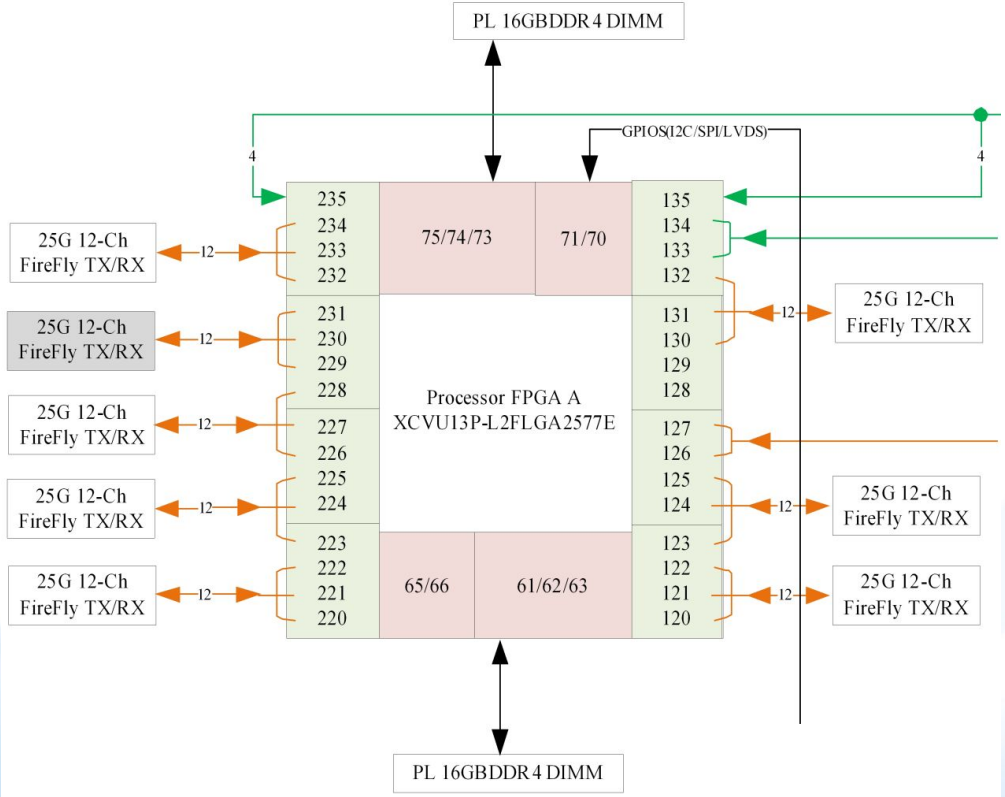


- As shown in the left configuration, the PS side interface includes:
  - **2** QSPI
  - **1** SD1 3.0
  - **2** I2C Master
  - **2** SPI Master
  - **1** UART0
  - **2** GEM2-3
  - **1** DDR4
- A common Linux from CERN will run on this SoC to provide control, and monitoring.

Optical Module - Firefly

- 25Gx12 and 14Gx12 module will be installed on GCM for different configurations.
- These two different type of modules are pin compatible. The same connectors are used for both of them
- The Firefly can come with Y cable of 24 channels, which can be configured as 24 TX, 24RX or 12 TX+ 12 RX.

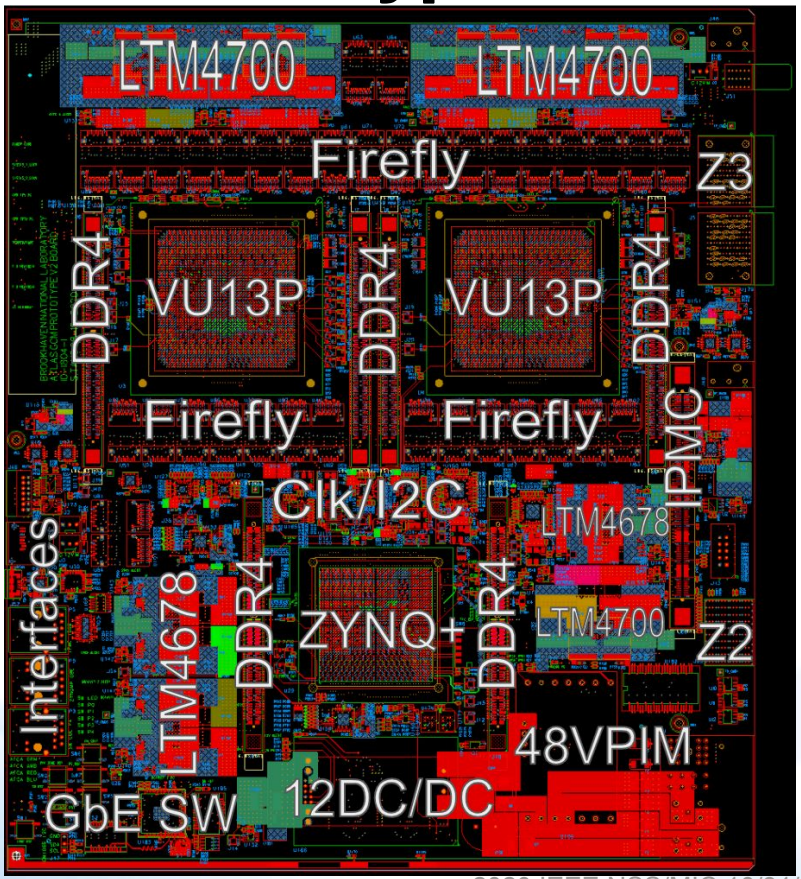
Floor Plan on GCM Hardware



As shown in the left connections for the Processor Node FPGA design:

- **8** piars of Firefly x12 are connected to 96 GTY links, covers all the floor plan of different Nodes.
- **2** DDR4 connected to SLR0/3
- **8** GTY links from/to GRM
- **8** GTY links from/to ZYNQ+

GCM Prototype Stack-up and Layout



TTM Technologies
Time-To-Market Interconnect Solutions

Date: May.04.2020

Customer P/N: Part REV
Internal P/N: SJ5969A_RMSCircuits_BNLGCMPrototypeV2_26LYRS
Contact: Yadira Gutierrez Phone:
Customer Req Thk: 100+/-10 mils Measured:Over mask on plated copper

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	1.80	.5 oz			Foil .5 oz
			3.04	3.25	Prepreg Tachyon 100G 1078(70.5) 18.25Gx24.25
2	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 1 oz VLP2 18.25Gx24.25
3	1.20	1 oz			
			3.04	2.95	Prepreg Tachyon 100G 1078(70.5) 18.25Gx24.25
4	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
5	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
6	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
7	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
8	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
9	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
10	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
11	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
12	0.60	0.5 oz			
			3.07	4.00	Core Tachyon 100G 4.00mils 2x1035 0.5 oz / 1 oz VLP2 18Gx24
13	1.20	1 oz			
			3.04	2.80	Prepreg Tachyon 100G 1078(70.5) 18.25Gx24.25
14	1.20	1 oz			
			3.07	4.00	Core Tachyon 100G 4.00mils 2x1035 0.5 oz / 1 oz VLP2 18Gx24
15	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
16	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
17	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
18	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
19	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
20	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
21	0.60	0.5 oz			
			3.02	3.10	Prepreg Tachyon 100G 1078(72) 18Gx24
22	0.60	0.5 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 0.5 oz VLP2 18.25Gx24.25
23	0.60	0.5 oz			
			3.04	2.95	Prepreg Tachyon 100G 1078(70.5) 18.25Gx24.25
24	1.20	1 oz			
			3.09	3.00	Core Tachyon 100G 3.00mils 1078 0.5 oz / 1 oz VLP2 18.25Gx24.25
25	0.60	0.5 oz			
			3.04	3.25	Prepreg Tachyon 100G 1078(70.5) 18.25Gx24.25
26	1.80	.5 oz			Foil .5 oz

94.80	Thickness over Laminate
98.40	Thickness over Copper
99.40	Thickness over Soldermask

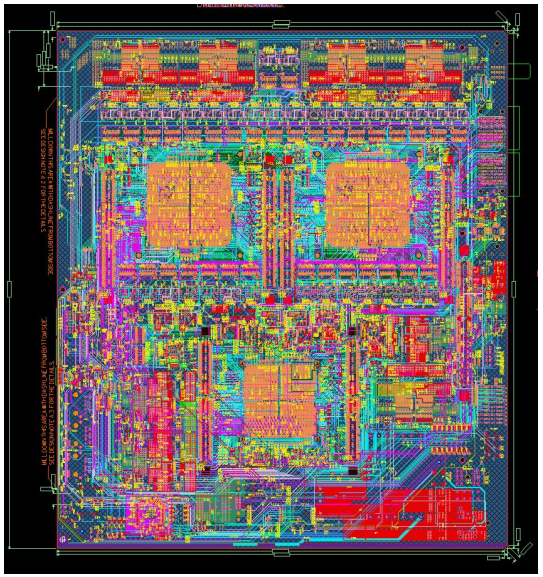
Thermal Consideration

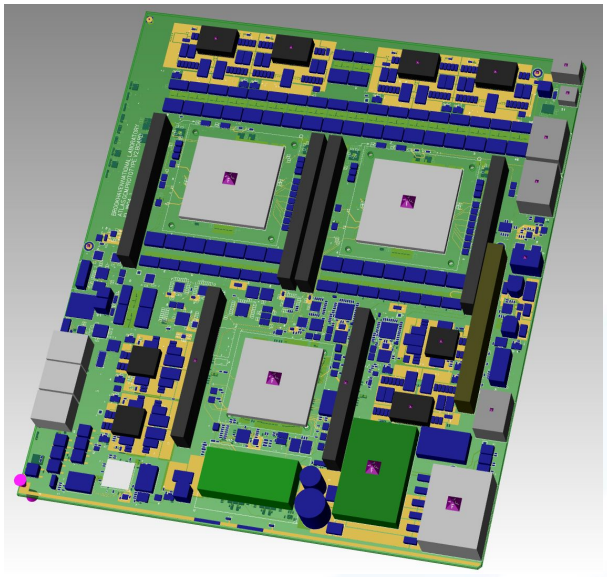
- ATCA airflow is around 500 LFM when setting the fan in middle range.
- The ATS and ALPHA models are compatible with PCB design.

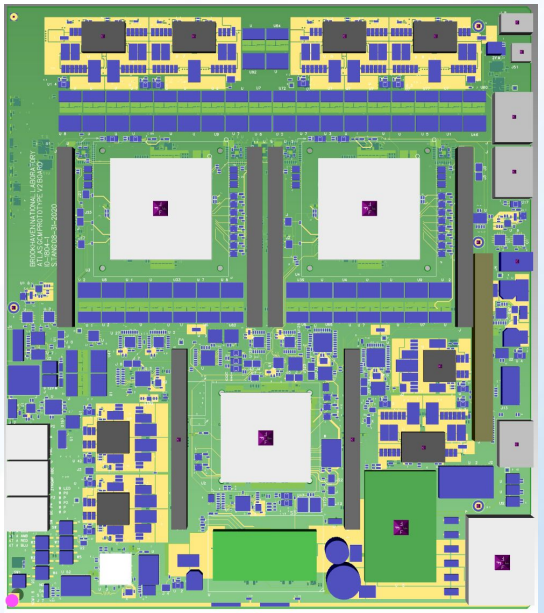
FPGA	Vendor	Heat-Sink Part Number	WxLxH (mm)	Install type	Rt(C/W @500LFM)	Target Temp. (C)
ZU19EG	ATS	ATS-FPX054054013-17-C2-R0	54.0 x 54.0 x 12.7	Push-Pin	0.8	41.0 @ 20W
ZU19EG	ALPHA	UBH54-12BP	54.0 x 54.0 x 12	Push-Pin	1.2	49.0@ 20W
VU13P	ATS	ATS-FPX070070015-28-C2-R0	70.0 x 70.0 x 15.0	Push-Pin	0.5	66.5 @ 83W
VU13P	ALPHA	UBM70-15B	70.0 x 70.0 x 15.0	Push-Pin	0.6	75.0 @ 83W

https://www.qats.com/Search/HeatSink/3283.aspx

GCM Hardware Design Status







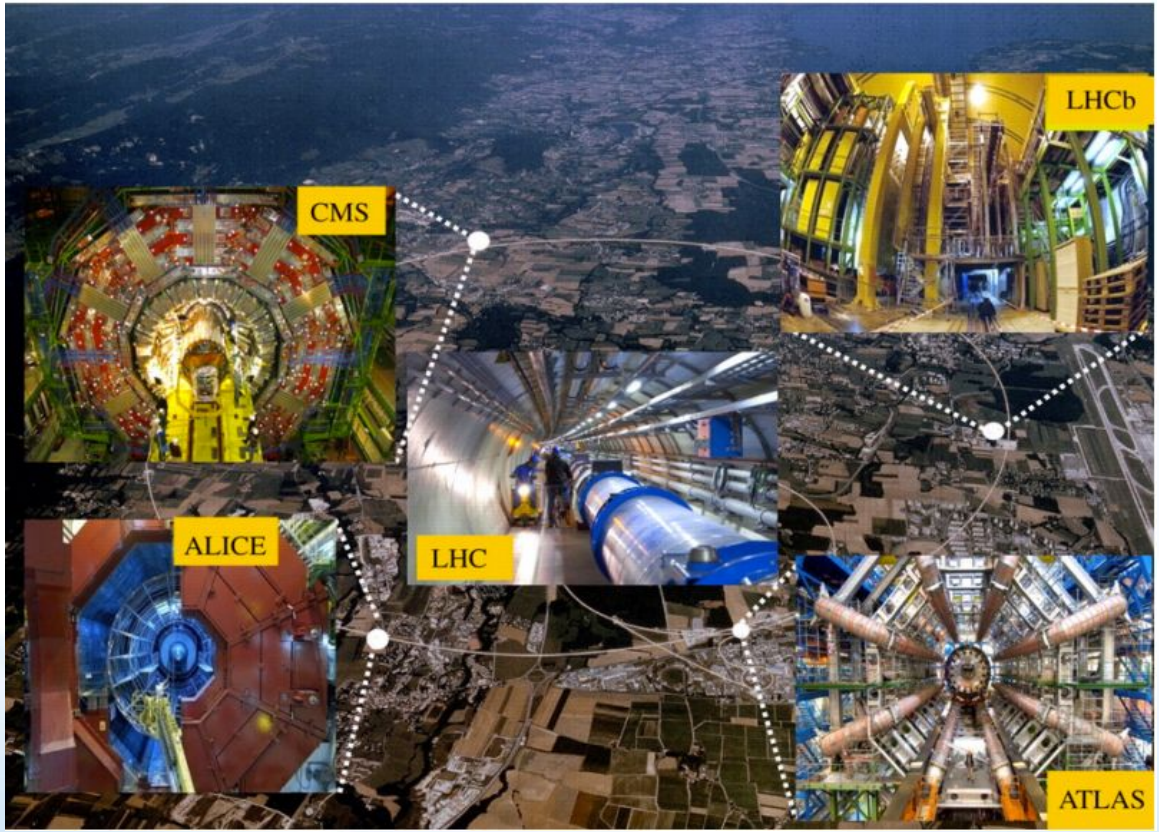
Hardware design has been finished and gone through internal and external reviews. Then it has been sent to **fabrication house on Sept. 9th**.

Summary

- Level-0 Trigger system is very critical for the HL-LHC to meet the significantly increased luminosity in the Run 4.
- Global Trigger is a new subsystem designed to meet the trigger requirements.
- Global Trigger consists of MUX, GEP and CTPi.
- A common hardware design is proposed for all these three nodes to simplify system design and long-term maintenance, and minimises the complexity of firmware development
- The GCM prototype has been submit for fabrication in September this year. It will be tested around December this year, and results will be included in the paper which is planned to be submitted to TNS.

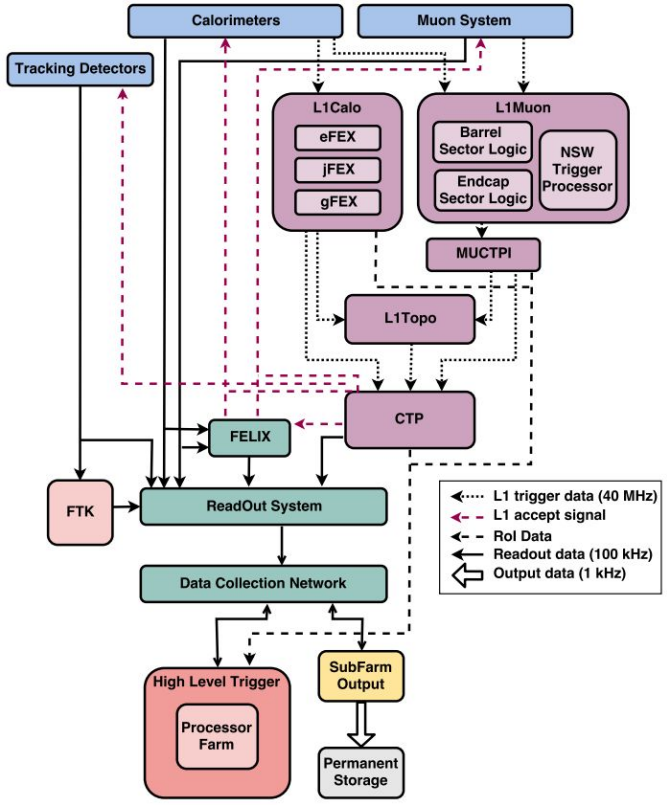
Thanks

The LHC/HL-LHC Experiments



- *Four main experiments*
  - **ATLAS**
  - CMS
  - LHCb
  - ALICE

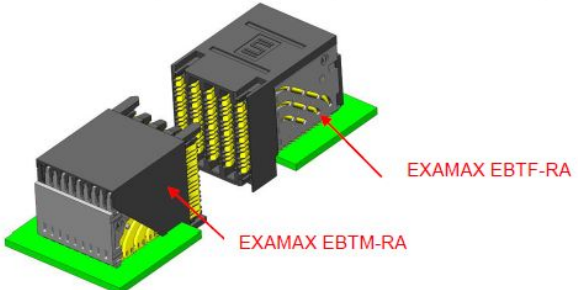
ATLAS Trigger in Run 3 (After Phase-I Upgrade)

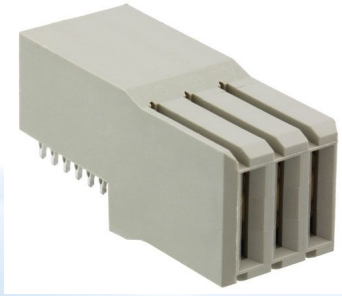


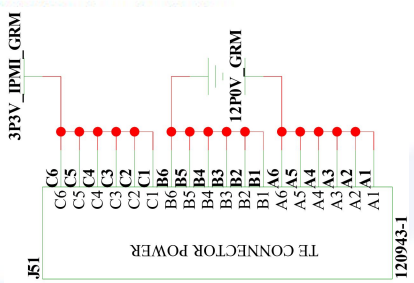
- Overview of the TDAQ system after the Phase-I upgrade
  - Level-1 trigger data is about 40MHz
  - Level-1 trigger acceptance (L1A) rate is around 100 kHz
  - L1A latency is about 2.5 μs.
  - Approx. 1000 event/s for recording to permanent storage (O(1) Pb/s observed to O(1) Pb/year recorded).
- Limitations of the Run 3 Level-1 Trigger System
  - Front-end electronics systems were built at the time of their construction
  - Current hardware restricts rate to 100 kHz
  - Maximum latency 2.5 μs
  - Limited acceptance and reduced efficiency
- Without a higher rate or longer latency, the Level-1 Trigger algorithms **cannot be improved enough** to cope with HL-LHC conditions.

ZONE 3 Design

Table 2: ExaMAX EBTM-RA Connector Configuration Offerings			
Signal pairs per column	Number of Columns	Column Spacing	Number of Positions (Including Grounds)
4 pair	6, 8 and 10	2.0mm	84, 112 and 140
6 pair	6, 8, 10, and 12	2.0mm	120, 160, 200, and 240



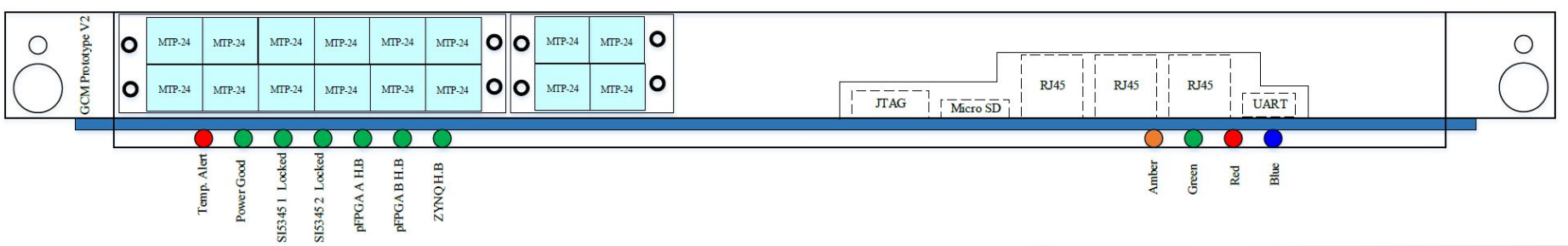


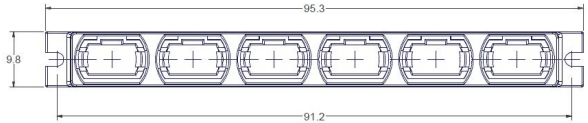


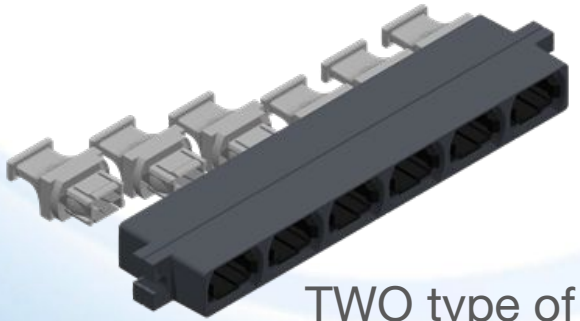
- EBTF-4-10-2.0-S-RA-1-L/R from Samtec
- Enables 56 Gbps electrical performance on 2.00 mm column pitch
- Meets industry specifications such as PCI Express®, Intel OPI abd UPI, SAS, SATA, Fibre Channel, Infini Band™ and Ethernet
- 4 pairs per column/ 10 Columns
- 2.00 mm (.0787") pitch
- Press fit termination
- Right-angle orientation

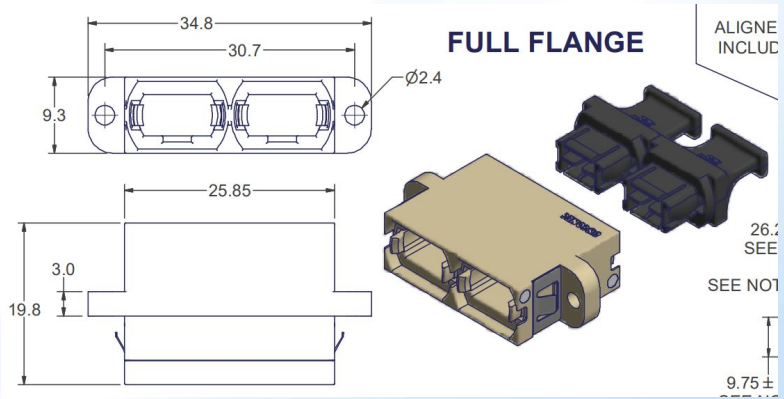
- 120943-1 from TE
- Receptacle/3 Positions-RA
- For 3.3V/GND/12.0V
- Hotswap is supported by TPS2458

FRONT Panel Design









TWO type of MTP adaptor are selected for 16 ports