Global Trigger Technological Demonstrator for ATLAS Phase-II upgrade

Virtual 2020 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC)

4 November 2020

Viacheslav Filimonov, Bruno Bauss, Volker Büscher, Ulrich Schäfer, Duc Bao Ta

On behalf of the ATLAS TDAQ Collaboration

PRISMA Cluster of Excellence

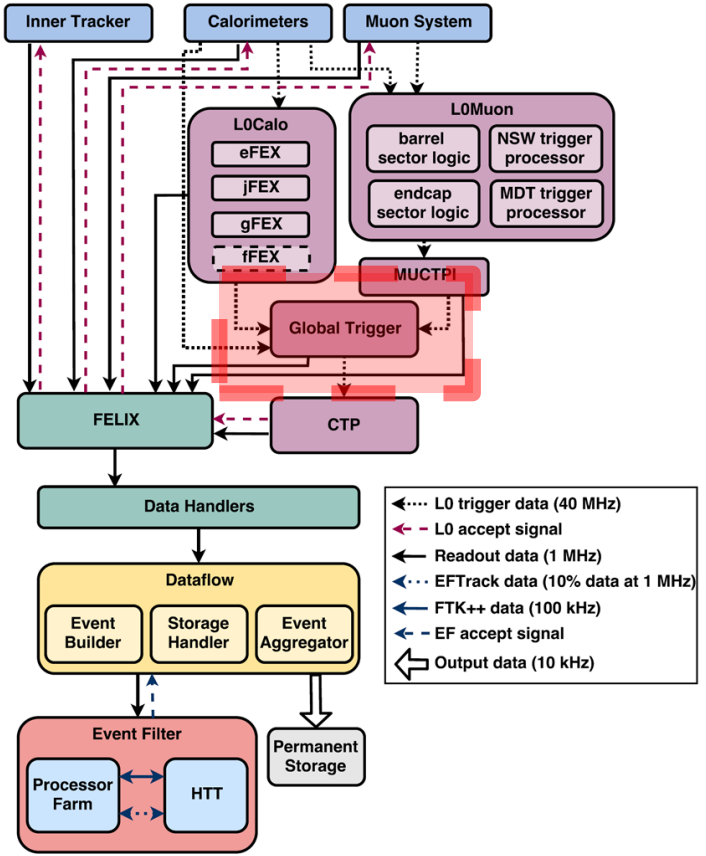
BMBF-Forschungsschwerpunkt ATLAS-EXPERIMENT FSP 103 ATLAS Physik bei höchsten Energien mit dem ATLAS-Experiment am LHC

JOHANNES GUTENBERG UNIVERSITÄT MAINZ JG|U

Introduction

Phase-II Global Trigger system: Functionality

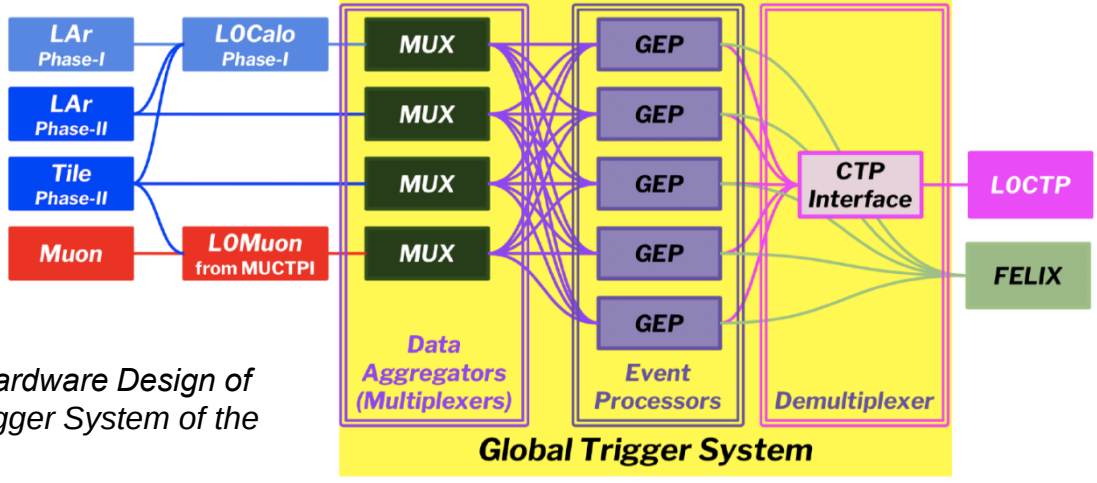
- As part of the Phase-II Level-0 Trigger System, the **Global Trigger** uses full-granularity calorimeter cells to refine L0Calo & L0Muon output
- Allows iterative algorithms such as topoclustering and use of higher level synthesis
- Reconstructs taus, jets, MET, & calorimeter-based isolation
- Applies topological requirements



TDAQ System after the Phase-II upgrade

Phase-II Global Trigger system: Implementation

- Time-multiplexed system concentrates data of full event into a single processor
- Composed of 3 main layers
  - Multiplexing (MUX) layer
  - Global Event Processor (GEP) layer
  - Demultiplexing Global-to-Central Trigger Processor (CTP) Interface
- Input: >2300 optical fibers with link speeds up to 25.8 Gb/s
- Global Common Module (GCM) is used as the building block in each layer
  - ➢ See talk by S. Tang: *"The Prototype Hardware Design of Global Common Module for Global Trigger System of the ATLAS Phase II Upgrade"*

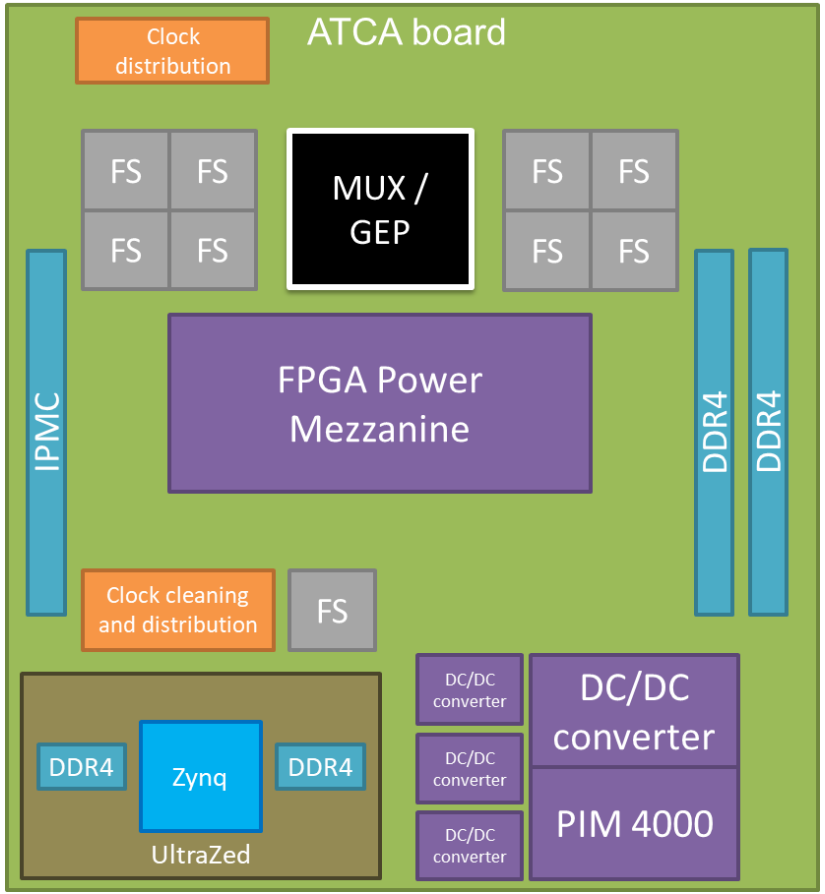


Phase-II Global Trigger system: Deployment Module

- Production Firmware Deployment Module (PFM):
  - Serves a dual purpose
    - A **hardware platform** required by each group involved in the GCM firmware development
    - Used for pre-commissioning of regular firmware upgrades **with the production system in place**
  - Represents a **slice of the GCM** (including a processing unit, a control FPGA and a number of optical modules) in any layer of the Global Trigger system
  - Will be **available well before the production GCM** to allow for early development, testing and debugging of the algorithm and infrastructure firmware

- Design based on the Technological Demonstrator R&D

Phase-II Global Trigger system: PFM Structure



- ATCA board
- Single MUX / GEP FPGA (Xilinx **Ultrascale+ VU13P**)
- Up to 8 **Finisar BOA** modules for real-time data path
- Single Finisar BOA module for interface to FELIX
- UltraZed board with **Zynq UltraScale+**
- IPMC
- Power mezzanines
- **DDR4 RAM**s

- Many PCB design blocks tested on the Technological Demonstrator
- PCB design is complete

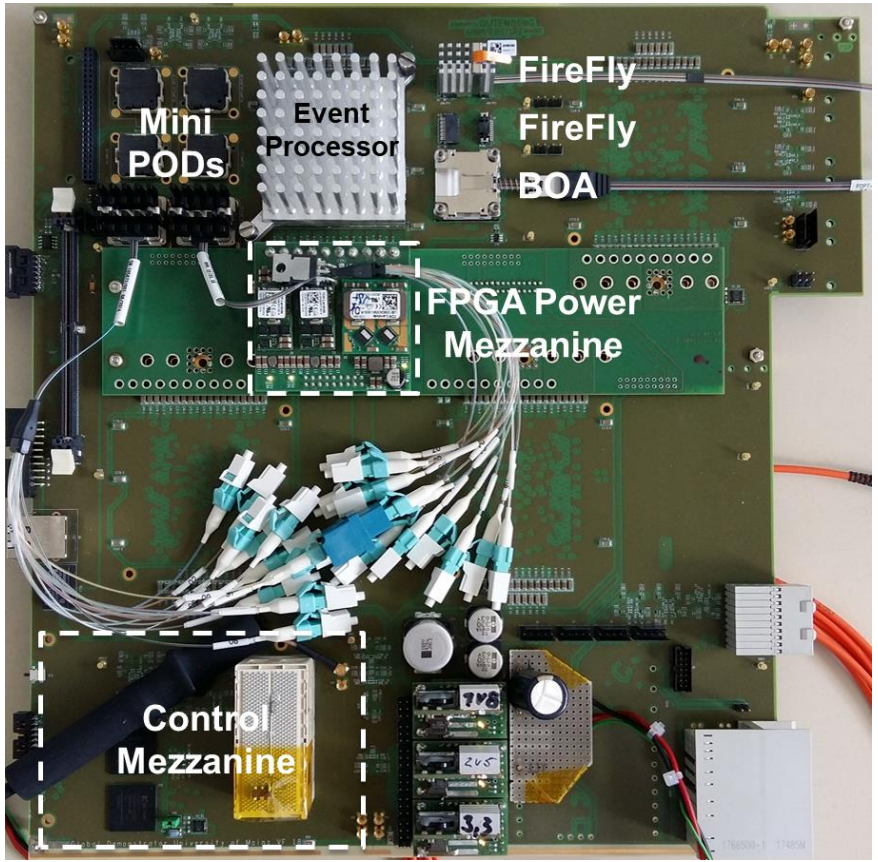
Global Trigger Technological Demonstrator

Viacheslav Filimonov

Technological Demonstrator

- GCM and PFM required an R&D for the new generation of **optical modules** and FPGAs running at **high data rates** (up to **25.8 Gb/s**) → Technological Demonstrator board designed and tested

- A **custom designed** ATCA board
- One Xilinx Virtex **UltraScale+ 9P** FPGA
- Two 28G 2x4 bidirectional **Samtec FireFly** modules
- One 28G 2x12 bidirectional **Finisar BOA** module
- Six MiniPODs: 3 RX + 3 TX
- Mezzanines: Power, Control
- Optical modules **implemented on-board**

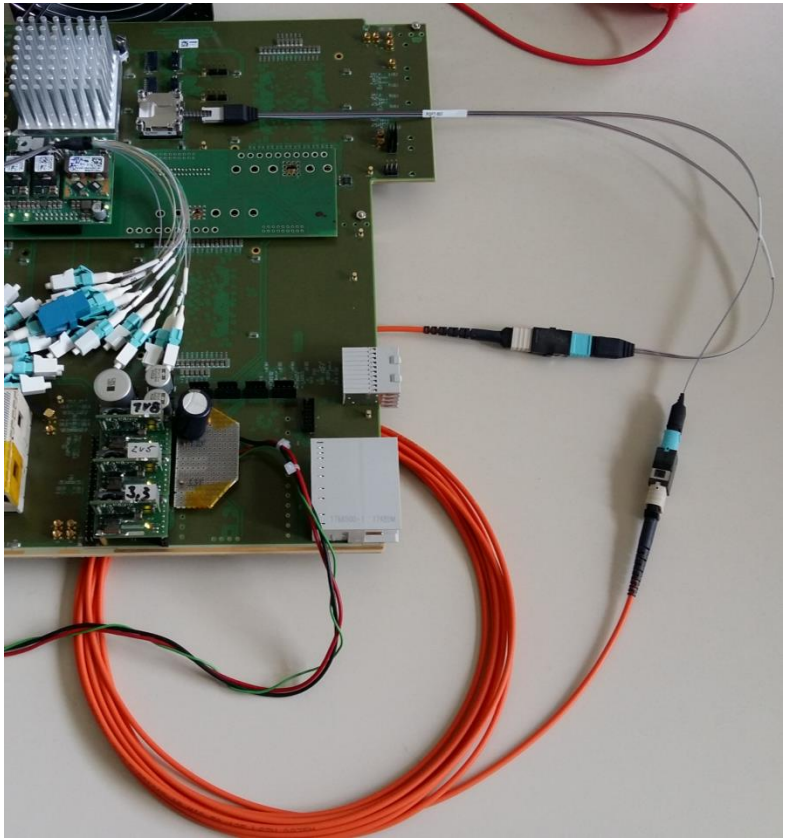


Technological Demonstrator

Finisar BOA IBERT loopback test: test setup

- Performance of the high-speed optical modules and the FPGA on the Technological Demonstrator has been evaluated with long-run loopback Integrated Bit Error Ratio Tests (IBERT)

- 12 transmitter links of the optical module were looped back to 12 receiver links of the same module with a help of a 24 to 2x12-fiber Y-cable and a 12-fiber trunk cable



Link status

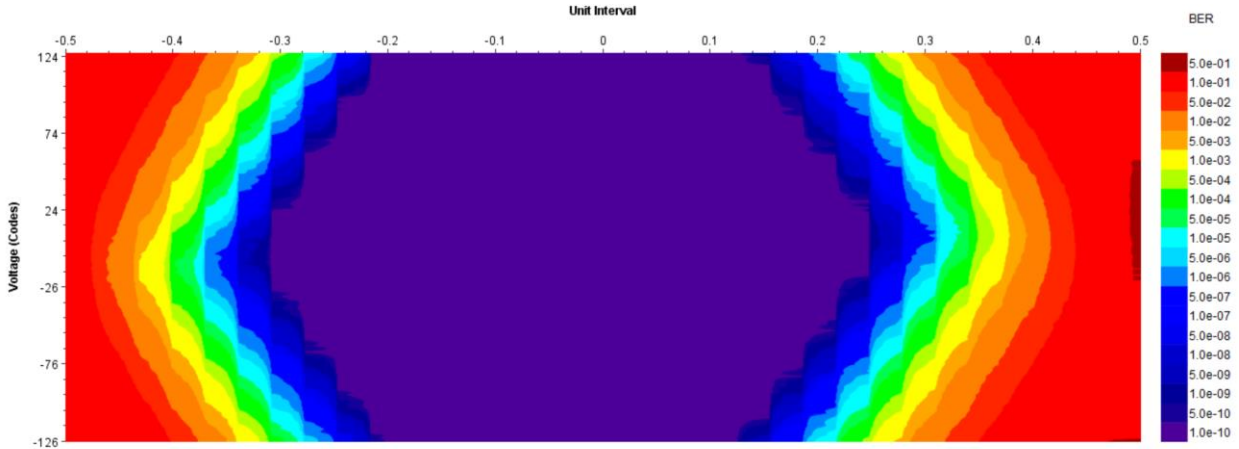
- A day-long IBERT test run at 25.65 Gb/s performed
- 31-bit PRBS pattern used

- 1.9E-15 BER reached
- All 12 links functional
- No bit errors detected

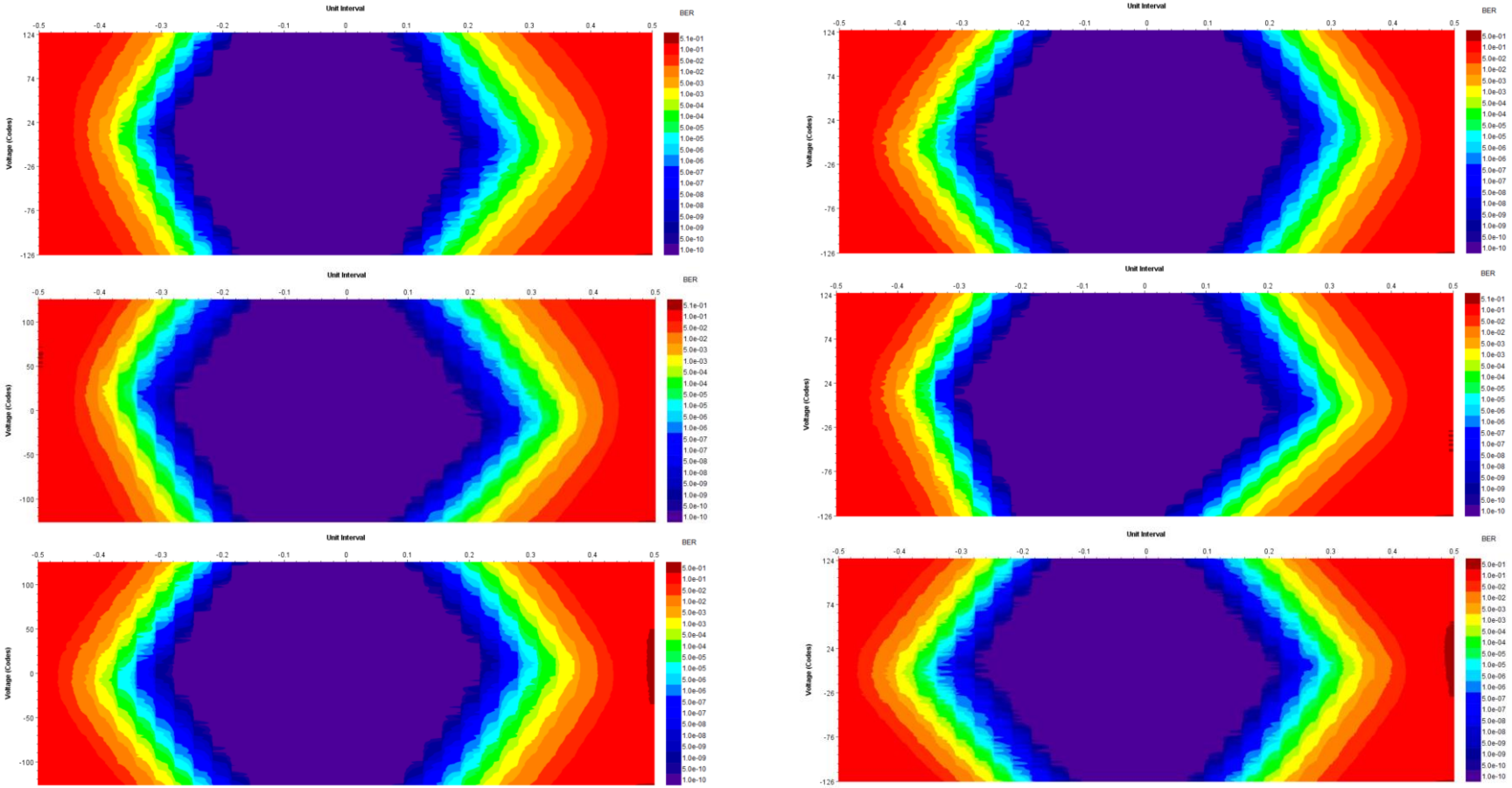
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cur
Ungrouped Links (0)											
Link Group 0 (12)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 0	MGT_X0Y43/TX	MGT_X0Y40/RX	25.652 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 1	MGT_X0Y40/TX	MGT_X0Y43/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 2	MGT_X0Y42/TX	MGT_X0Y41/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 3	MGT_X0Y41/TX	MGT_X0Y42/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 4	MGT_X0Y35/TX	MGT_X0Y22/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 5	MGT_X0Y34/TX	MGT_X0Y23/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 6	MGT_X0Y33/TX	MGT_X0Y20/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 7	MGT_X0Y32/TX	MGT_X0Y21/RX	25.650 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 8	MGT_X0Y19/TX	MGT_X0Y15/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 9	MGT_X0Y18/TX	MGT_X0Y13/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 10	MGT_X0Y17/TX	MGT_X0Y14/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(
Link 11	MGT_X0Y16/TX	MGT_X0Y12/RX	25.651 Gbps	5.27E14	0E0	1.897E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00(

Eye diagram

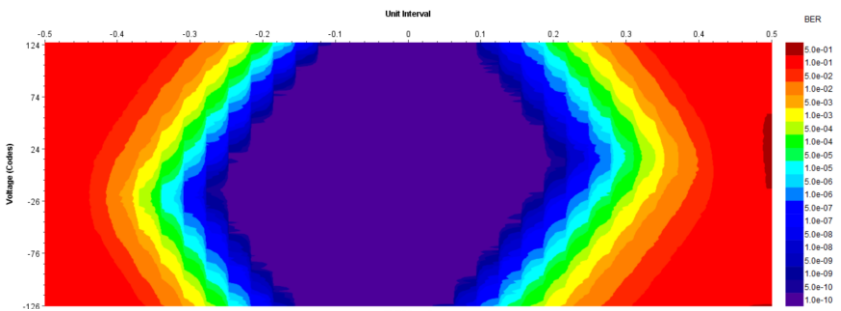
- A typical eye diagram
- Low Power Mode of the GTY receiver
- Open area: 7608, Open UI: 57.58 %, 25.65 Gb/s data rate
- Good performance

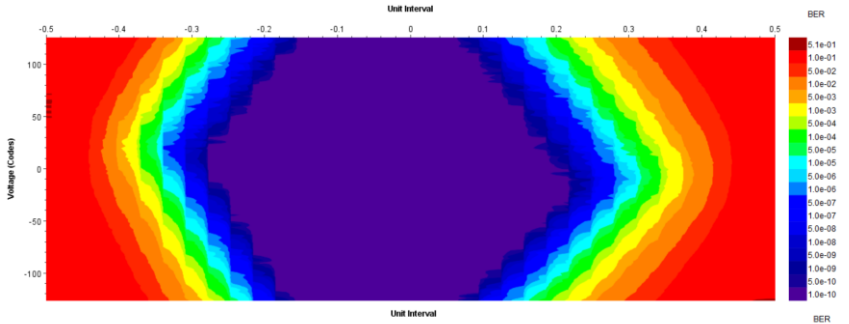


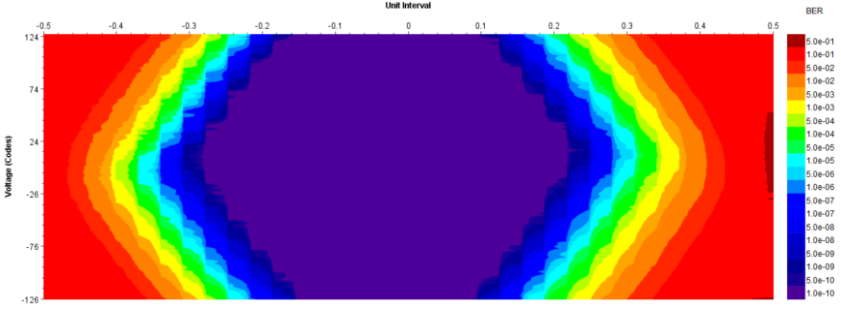
Eye diagrams: other channels

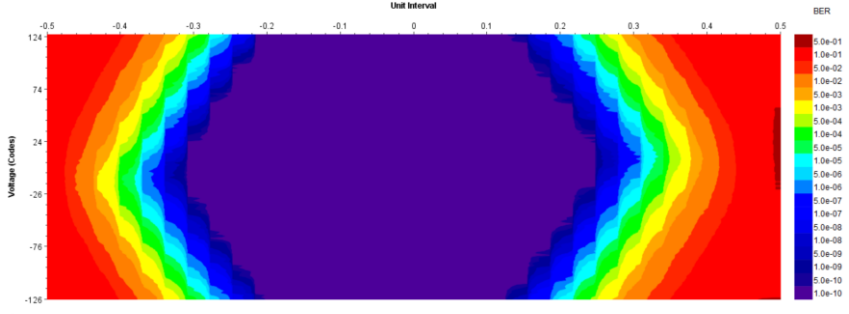


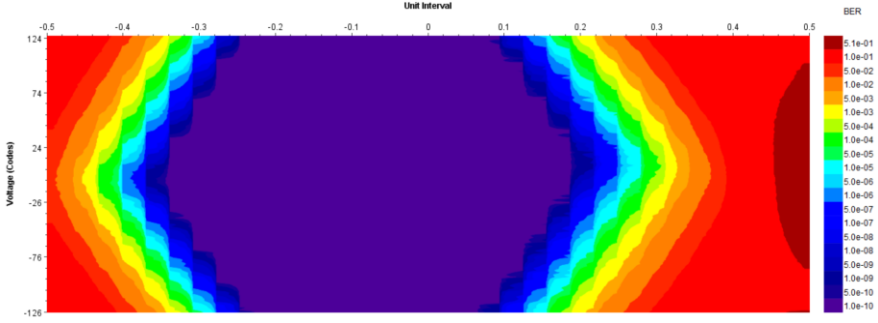
Eye diagrams: other channels





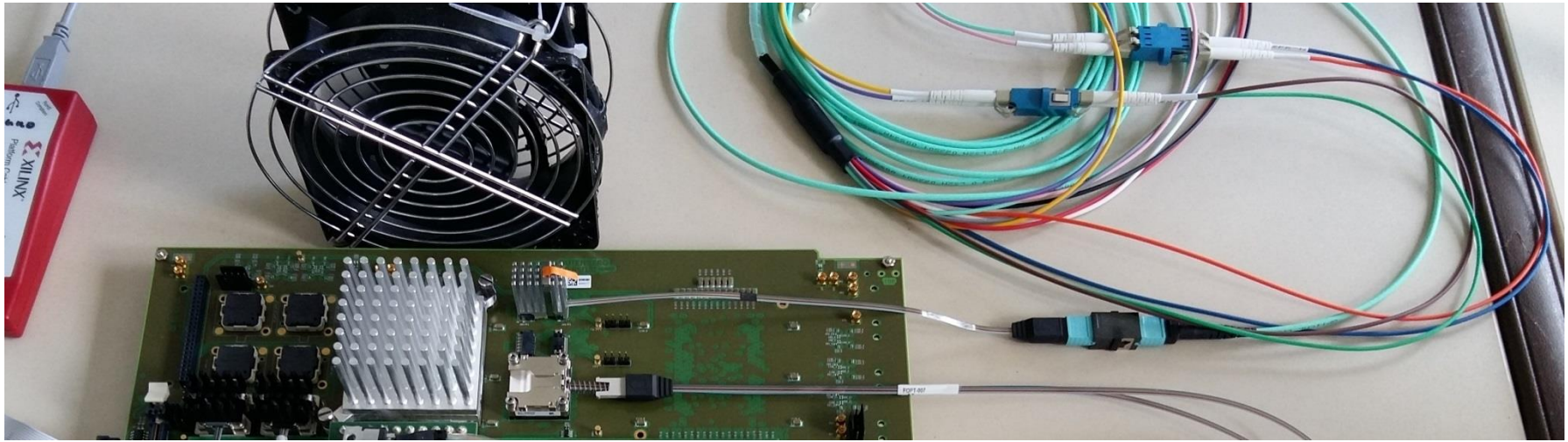






Samtec FireFly IBERT loopback test: test setup

- 4 transmitter links of the optical module were looped back to 4 receiver links of the same module with a help of a 12-fiber MTP to LC breakout cable



Link status

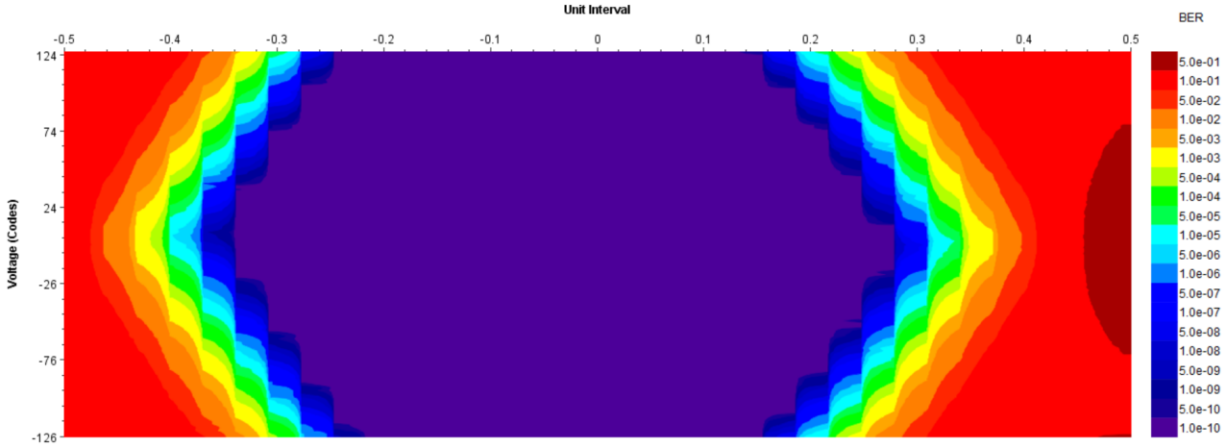
- A day-long IBERT test run at 27.58 Gb/s performed
- 31-bit PRBS pattern used

- 1.7E-15 BER reached
- All 4 links functional
- No bit errors detected

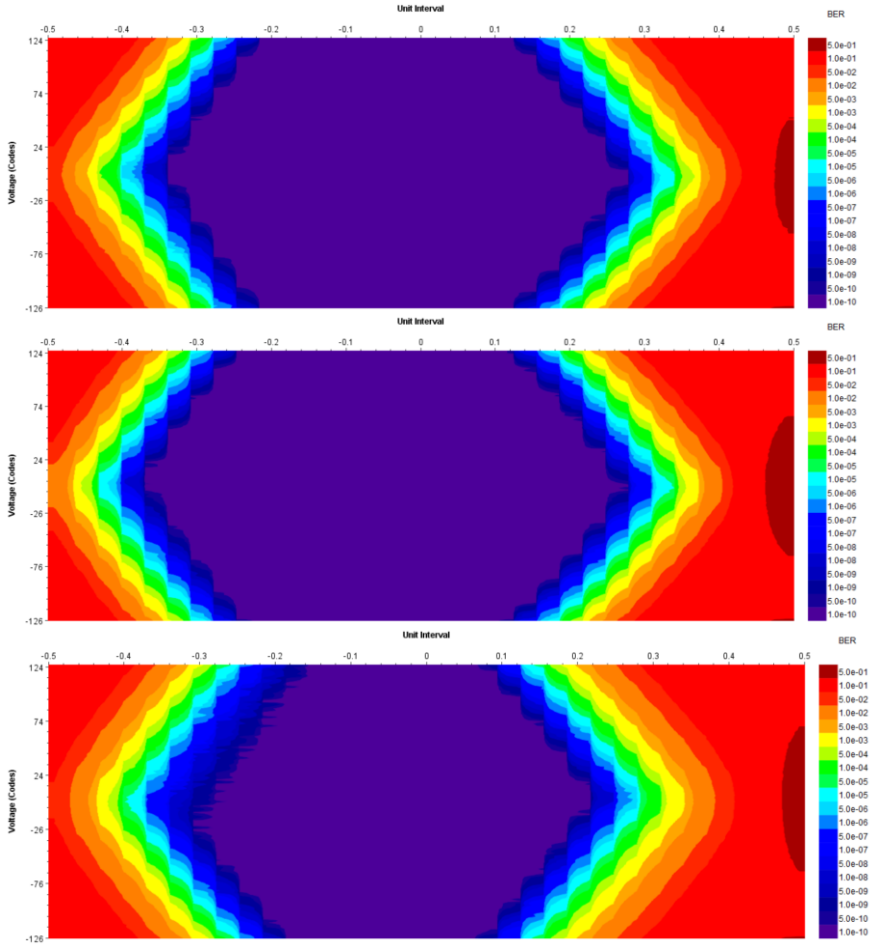
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Curs
Ungrouped Links (0)											
Link Group 0 (4)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (000
Link 0	MGT_X0Y54/TX	MGT_X0Y54/RX	27.576 Gbps	5.732E14	0E0	1.744E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (000
Link 1	MGT_X0Y55/TX	MGT_X0Y55/RX	27.575 Gbps	5.732E14	0E0	1.744E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (000
Link 2	MGT_X0Y53/TX	MGT_X0Y52/RX	27.575 Gbps	5.732E14	0E0	1.744E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (000
Link 3	MGT_X0Y52/TX	MGT_X0Y53/RX	27.575 Gbps	5.732E14	0E0	1.744E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (000

Eye diagram

- A typical eye diagram
- Low Power Mode of the GTY receiver
- Open area: 8612, Open UI: 63.64%, 27.58 Gb/s data rate
- Good performance



Eye diagrams: other channels



Summary

- The high-speed link support is essential for the Global Trigger system in order to cope with the transmission of high-granularity calorimeter data which drives the bandwidth requirements

- A technological demonstrator has been designed and used for evaluation of 25+ Gb/s Samtec FireFly and Finisar BOA optical modules implemented on-board together with the Xilinx Virtex UltraScale+ 9P FPGA

- A good performance and absence of bit errors during long runs have been demonstrated for both high-speed optical modules

BACKUP

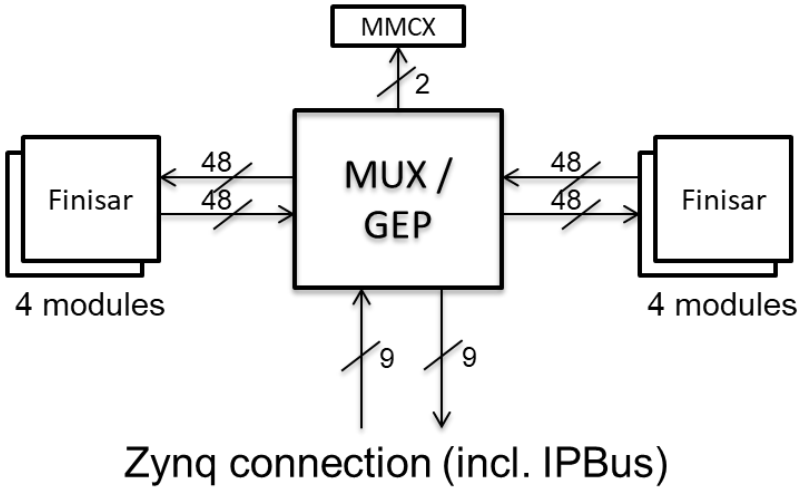
VU13P PFM Floor plan

OM = Optical Module connection
Connections to a single optical module are grouped with braces

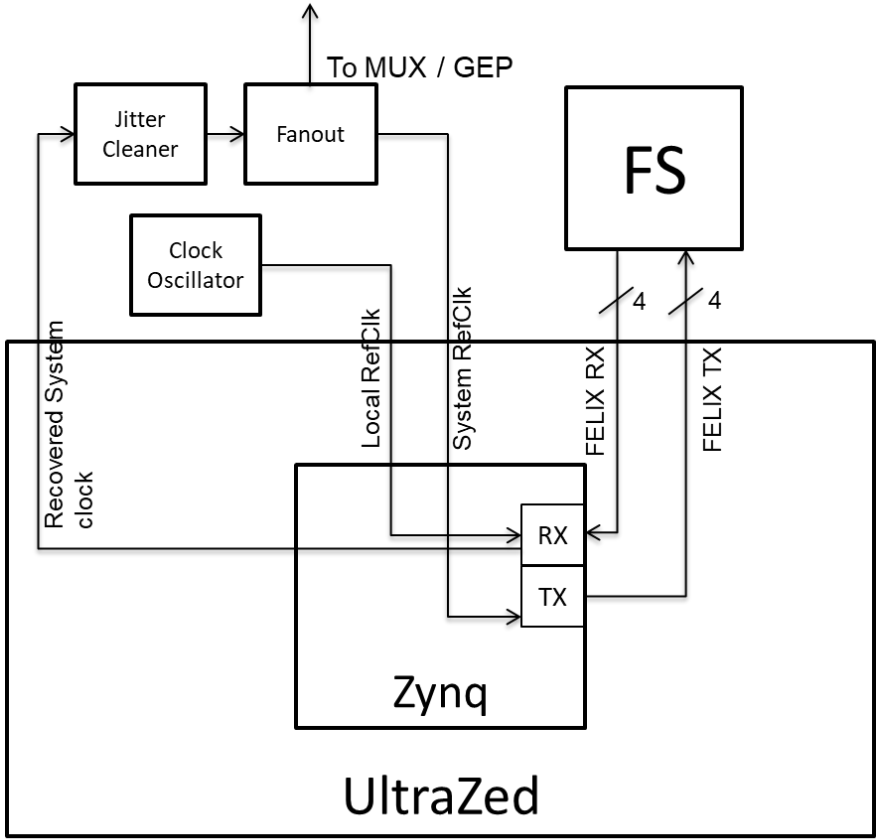
MUX / GEP MGT connections

- 32 GTY quads (128 RX, 128 TX) available, providing the following connectivity
  - Connection to optical modules (96 RX, 96 TX)
  - Zynq connection (8 RX, 8 TX)
  - IPBus connection: Zynq ↔ MUX / GEP (1 RX, 1 TX)
  - Debug (2 TX)
  - Spare (23 RX, 21 TX)

MGTs + Finisars operation tested on the Demonstrator



Clock distribution for FELIX interface



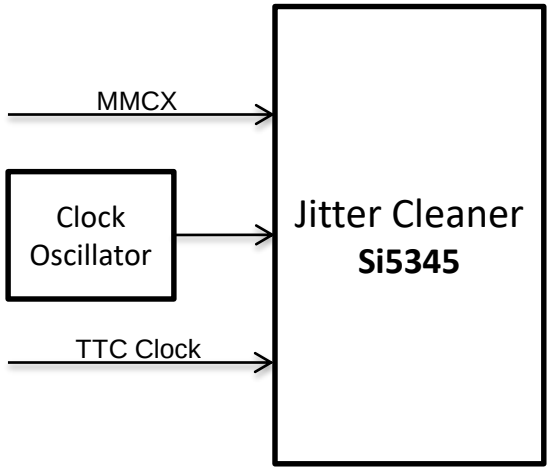
- FELIX RX
  - TTC
- FELIX TX
  - Data
  - Busy

- Samtec high-speed board-to-board connector
  - Speed rating: 14GHz / 28Gbps

http://suddendocs.samtec.com/testreports/hsc-report-sma_seam8-seaf8-07mm_web.pdf

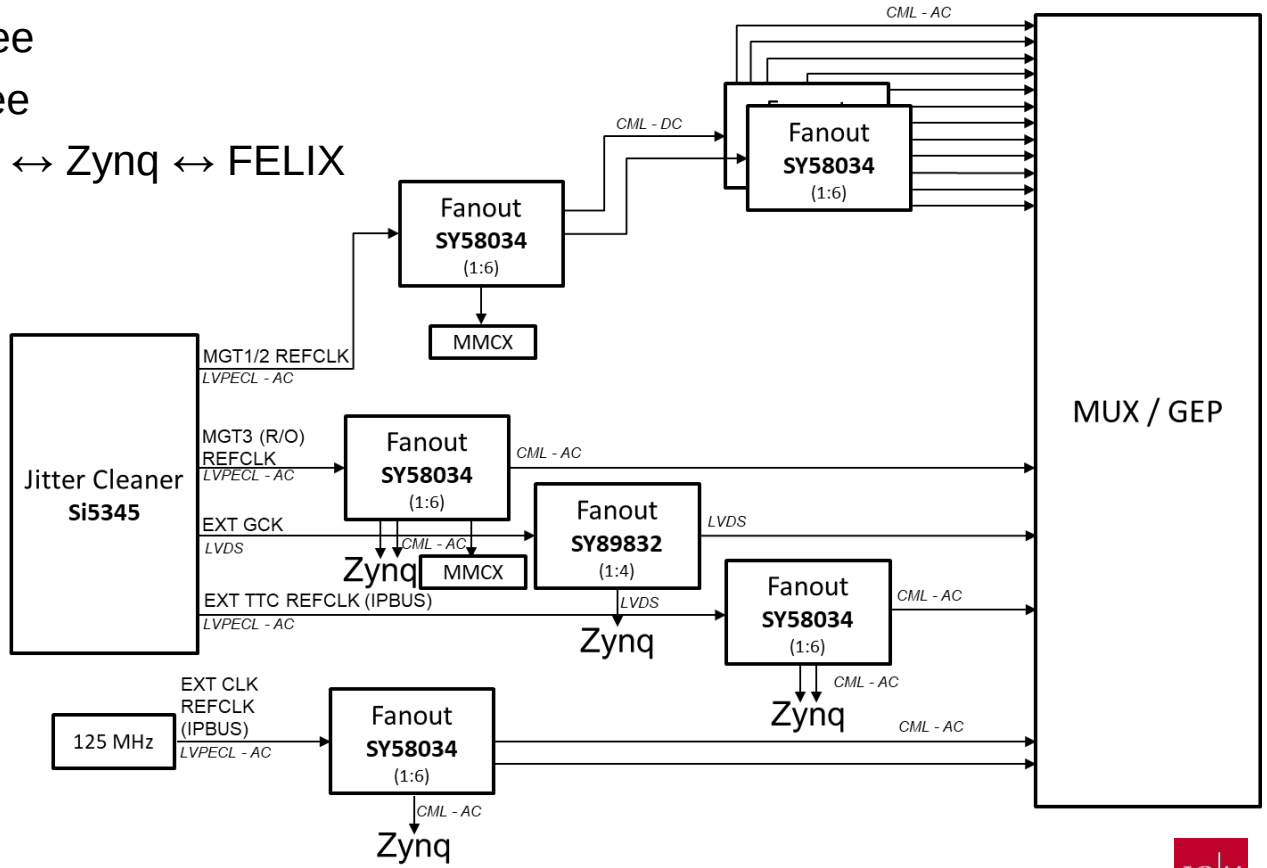
Clock scheme: Jitter Cleaner‘s input options

- Three input options
  - Recovered TTC clock
  - Clock oscillator
  - MMCX connectors



Clock trees

1. Full MGT1 (RX) REFCLK tree
2. Full MGT2 (TX) REFCLK tree
3. MGT3 (R/O) REFCLK: GEP ↔ Zynq ↔ FELIX
4. Global clock
5. IPBUS REFCLK
    1. EXT TTC
    2. EXT CLK



Reference clock restrictions

- The MGTs reference clock scheme is designed to minimize the number of signals routed on the PCB

- The reference clocks for a QUAD can also be sourced from one QUAD below or above for high data rates (16.375 – 28.21 Gb/s) and for up to two QUADs below or above for low data rates (below 16.375 Gb/s)

- Reference clock sharing between different SLRs is not allowed

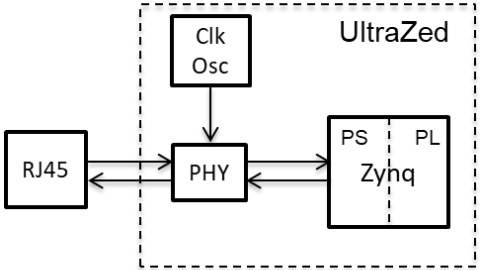
Control block

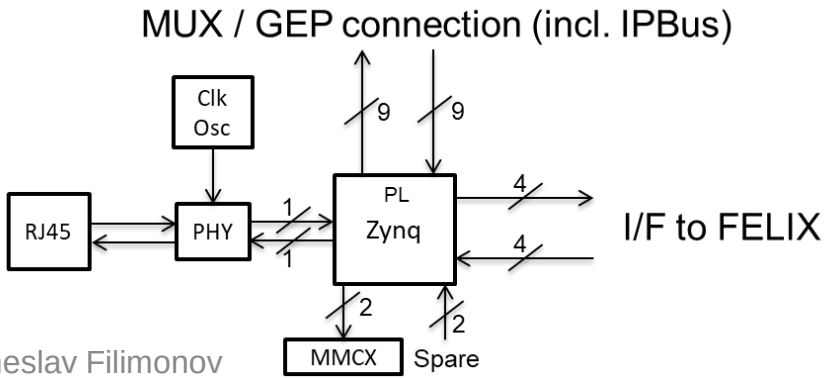
- The Control block provides many of the (non-real-time) services required on the PFM prototype
  - Hosts the control FPGA of the PFM prototype
  - Hosts the MasterSPI configuration circuitry for processor and control FPGAs
  - Clock cleaning and distribution
  - Monitoring and slow control
  - IPbus master
  - Interface to FELIX (Incl. TTC clock recovery)

- ZYNQ Ultrascale+ (XCZU7EV-FBVB900) device is used as the control FPGA
- The Control FPGA is located on a commercial system on a module (SoM) from Avnet (UltraZed-EV SOM)

Zynq MGT connections

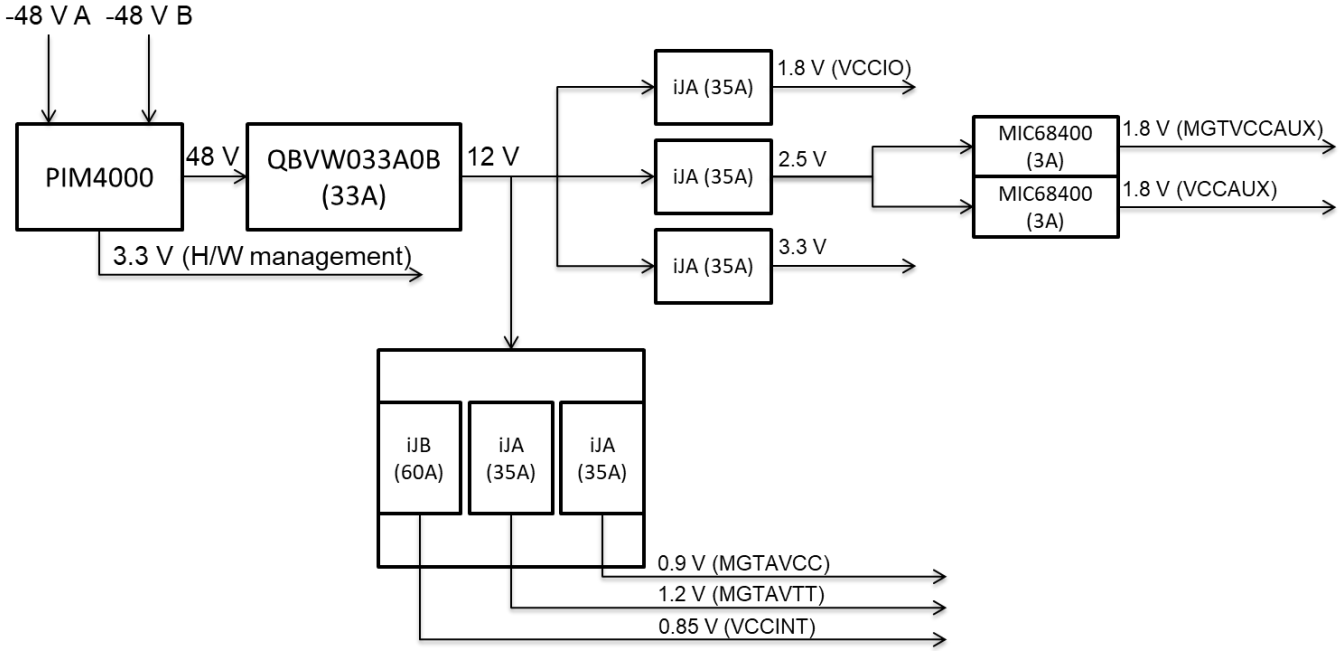
- Four quads (16 RX, 16 TX) available, providing the following connectivity
  - Interface to FELIX (4 RX, 4 TX)
  - MUX / GEP connection (8 RX, 8 TX)
  - IPBus connection: PHY chip (on the main board) ↔ Zynq, Zynq ↔ MUX / GEP (2 RX, 2 TX)
  - Debug (2 TX)
  - Spare (2 RX)
- IPBus connection can also use the PS side of the Zynq
  - PHY chip on UltraZed
  - Flexibility of implementing IPBus either in the PL or PS side of the Zynq





Power circuitry

- PIM4000 converter, QBVW033A0B DC/DC converter, power mezzanines (based on the TDK-Lambda iJX series of DC/DC converters), linear MIC68400 regulators

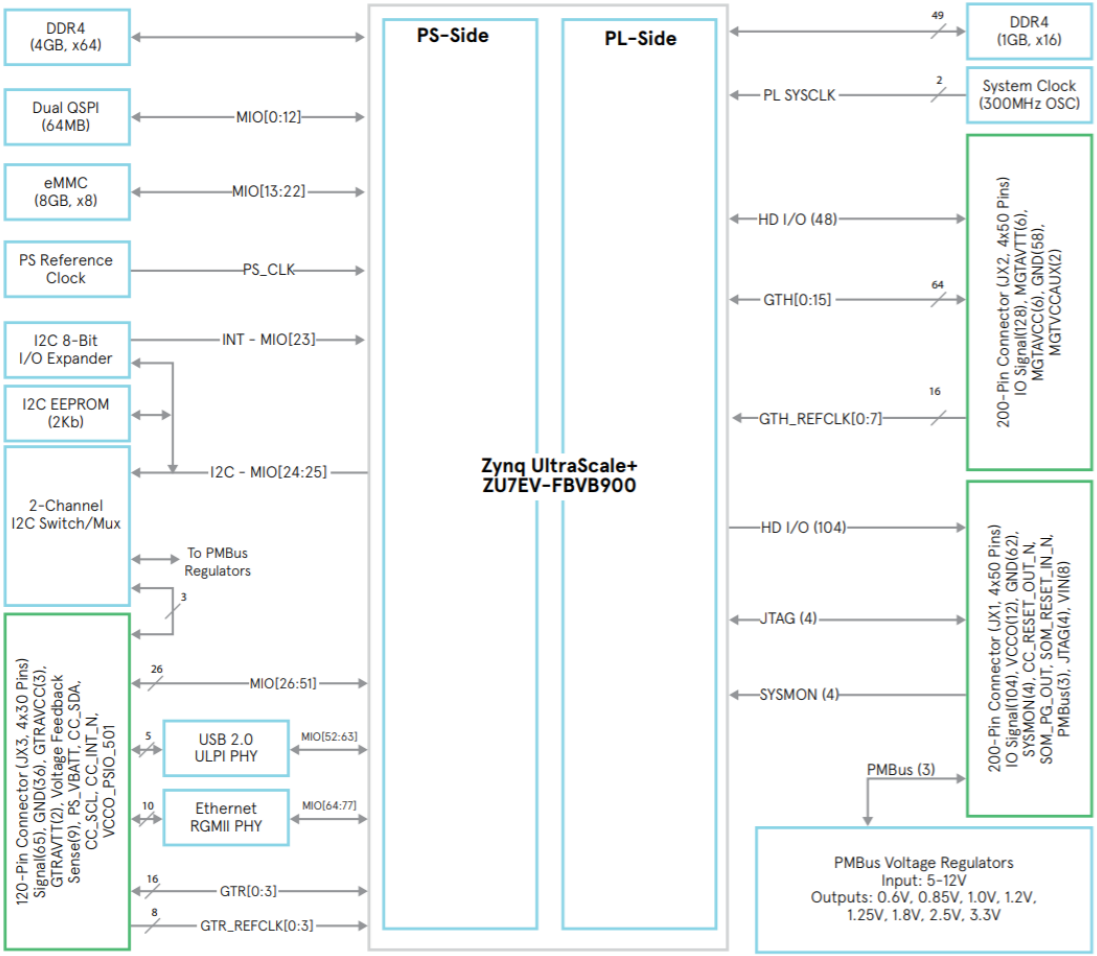


Power sequencing and operating voltages

- Power on sequence is controlled by a dedicated CPLD, which monitors the Power Good signals of every power regulator
    1. Board level 2.5 V and 3.3 V
    2. VCCINT, MGTAVCC
    3. MGTAVTT, VCCAUX, MGTVCCAUX
    4. VCCIO

- Operating voltages
    - VCCINT: 0.85 V
    - MGTAVCC: 0.9 V
    - MGTAVTT: 1.2 V
    - VCCAUX, MGTVCCAUX, VCCIO: 1.8 V

UltraZed


DDR4
(4GB, x64)
Dual QSPI
(64MB)
MIO[0:12]
eMMC
(8GB, x8)
MIO[13:22]
PS Reference
Clock
PS_CLK
I2C 8-Bit
I/O Expander
INT - MIO[23]
I2C EEPROM
(2Kb)
2-Channel
I2C Switch/Mux
I2C - MIO[24:25]
To PMBus
Regulators
3
120-Pin Connector (JX3, 4x30 Pins)
Signal(65), GND(36), GTRAVCC(3),
GTRAVTT(2), Voltage Feedback
Sense(9), PS_VBATT, CC_SDA,
CC_SCL, CC_INT_N,
VCCO_PSIO_501
26
MIO[26:51]
5
USB 2.0
ULPI PHY
MIO[52:63]
10
Ethernet
RGMII PHY
MIO[64:77]
16
GTR[0:3]
8
GTR_REFCLK[0:3]
PS-Side
PL-Side
Zynq UltraScale+
ZU7EV-FBVB900
49
DDR4
(1GB, x16)
PL SYSCLK
2
System Clock
(300MHz OSC)
HD I/O (48)
GTH[0:15]
64
GTH_REFCLK[0:7]
16
200-Pin Connector (JX2, 4x50 Pins)
IO Signal(128), MGTAVTT(6),
MGTAVCC(6), GND(58),
MGTVCCAUX(2)
HD I/O (104)
JTAG (4)
SYSMON (4)
PMBus (3)
200-Pin Connector (JX1, 4x50 Pins)
IO Signal(104), VCCO(12), GND(62),
SYSMON(4), CC_RESET_OUT_N,
SOM_PG_OUT, SOM_RESET_IN_N,
PMBus(3), JTAG(4), VIN(8)
PMBus Voltage Regulators
Input: 5-12V
Outputs: 0.6V, 0.85V, 1.0V, 1.2V,
1.25V, 1.8V, 2.5V, 3.3V