

# Charge collection properties of TowerJazz 180 nm CMOS Pixel Sensors in dependence of pixel geometries and bias parameters, studied using a dedicated test-vehicle: the Investigator chip

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## Abstract

This paper contains a compilation of parameters influencing the charge collection process extracted from a comprehensive study of partially depleted Monolithic Active Pixel Sensors with small ( $<25\ \mu\text{m}^2$ ) collection electrodes fabricated in the TowerJazz 180 nm CMOS process. These results gave guidance for the optimisation of the diode implemented in ALPIDE, the chip used in the second generation Inner Tracking System of ALICE, and serve as reference for future simulation studies of similar devices. The studied parameters include: reverse substrate bias, epitaxial layer thickness, charge collection electrode size and the spacing of the electrode to surrounding in-pixel electronics. The results from pixels of  $28\ \mu\text{m}$  pitch confirm that even in partially depleted circuits, charge collection can be fast ( $<10\ \text{ns}$ ), and quantify the influence of the parameters onto the signal sharing and amplitudes, highlighting the importance of a correct spacing between wells and of the impact of the reverse substrate bias.

*Keywords:* Monolithic Active Pixel Sensors, Solid state detectors, Charge collection

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## 1. Introduction

During the R&D for the new Inner Tracking System (ITS) [1] of the ALICE experiment at CERN LHC, a novel Monolithic Active Pixel Sensor (MAPS), named “ALPIDE”, was developed by the collaboration [2, 3, 4]. The chip is produced in 180 nm CMOS technology of TowerJazz<sup>1</sup> and features a quadruple well structure, which allows the use of PMOS together with NMOS devices within the pixel matrix. The schematic structure of a pixel cell in this technology is illustrated in Fig. 1.

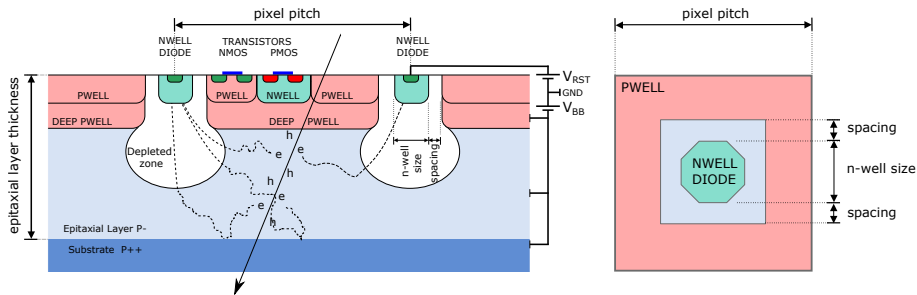


Figure 1: Schematic cross-section and top-view (not to scale) of the well structure used in the ALPIDE and Investigator chips, showing the key design parameters that influence the charge collection.

For the ALPIDE, the ALICE development has focused on partially depleted MAPS with small collection electrodes, implemented in the standard TowerJazz process. A process modification to fully deplete the sensitive layer was also introduced as a side development [5, 6], followed by additional modifications to further accelerate the charge collection in the context of detector developments for the Compact Linear Collider (CLIC) [7, 8, 9] and to enhance radiation tolerance for applications in ATLAS [10, 11, 12, 13].

For partially depleted devices, the generated electrons are transported by both diffusion and drift before being collected by the strong drift field in the depleted zone around the small collection electrode. A relatively large voltage signal of  $\Delta V \approx 100$  mV is generated on the collection electrode due to its small capacitance  $C$ , typically of the order of few fF [14] ( $\Delta V = Q/C$ , with  $Q$  being the collected charge). From this argument, it can already be seen that the performance will depend crucially on the spatial extension of the depleted region (or more generally the strength of the electric field) as it influences both the diode capacitance and the amount of diffusion and hence the charge spread. Finally, it will directly determine the duration of the collection process.

As a precise sensor technology CAD simulation model requires detailed knowledge of doping profiles for the entire sensor (wells, epitaxial layer, substrate), a series of different detection geometries were prototyped, both as bench-

<sup>1</sup><http://www.towerjazz.com/>

marks for simulations and for an heuristic approach to the optimisation of pixel geometries.

## 2. The Investigator chip

The Investigator chip was developed to study the MAPS design parameter space in the context of the ALICE ITS upgrade. It is produced using the Tower-Jazz 180 nm CMOS imaging process on wafers with a high-resistivity ( $>1 \text{ k}\Omega \text{ cm}$ ) epitaxial layer of three thicknesses: 18, 25 and 30  $\mu\text{m}$ . A reverse substrate bias voltage ( $V_{BB}$ , cf. Fig. 1) can be applied to the sensor<sup>2</sup>.

The performance of a pixel matrix is a combination of different parameters, amongst which the most prominent are conversion gain (capacitance), charge collection time, charge spread, and total charge collection efficiency. To access these parameters quantitatively, it is necessary to measure the induced signal in a direct and time-resolved way, simultaneously on a number of collection diodes. The Investigator chip contains more than hundred matrices with pixel pitches ranging from 20 to 50  $\mu\text{m}$ , different collection diode geometries, reset mechanisms, and input-transistor configurations [15]. Each of the matrices contains  $10 \times 10$  pixels, of which the central  $8 \times 8$  are read out in parallel, in an analogue fashion.

Due to its versatility, the Investigator also found applications as test vehicle in several other R&D contexts; CLIC [7, 8, 9], ATLAS [10], and the study of modifications of the CMOS process<sup>3</sup> to increase its timing performance and radiation hardness [5, 6].

### 2.1. Pixel geometries

Figure 1 shows a schematic cross section of a pixel and indicates the key geometric parameters that influence the charge collection: pixel pitch, epitaxial layer height, diode n-well size and spacing between diode n-well and surrounding p-well. The Investigator chip implements several combinations of these parameters. While they have to obey some boundary conditions in a fully integrated chip like ALPIDE, mainly imposed by the area needed to implement the in-pixel circuitry (e.g. discriminator, masking, in-pixel latches, readout network), the Investigator chip also contains pixel variants with larger diode n-wells and spacings, which is possible due to its minimal in-pixel circuitry.

Table 1 summarises the 13 different geometries that were studied for this paper. The pixel pitch is fixed<sup>4</sup> to 28  $\mu\text{m}$  and two values of epitaxial layer thickness of 18 and 25  $\mu\text{m}$  were studied. In addition, the reverse substrate bias voltage was swept from 0 to  $-6 \text{ V}$ .

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<sup>2</sup>Breakdown is observed between  $-8$  and  $-10 \text{ V}$ . To ensure sufficient operational margin, the chips were operated down to  $V_{BB} = -6 \text{ V}$ .

<sup>3</sup>The chips studied in this paper use the standard process without custom modifications.

<sup>4</sup>ALPIDE eventually features a  $29.24 \mu\text{m} \times 26.88 \mu\text{m}$  pitch due to global chip integration requirements [2, 3, 4]

Table 1: Summary of the pixel geometries analysed in this study. The pixel pitch is 28  $\mu\text{m}$  and variants were produced on 18  $\mu\text{m}$ - and 25  $\mu\text{m}$ -thick epitaxial layers.

Matrix #	69	70	73	74	75*	76	77	79	80	84	85	89	90
N-well ( $\mu\text{m}$ )	1.2				2			3		4		5	
Spacing ( $\mu\text{m}$ )	2	3	1	2	3	4	5	2	3	2	3	2	3

\*: ALPIDE-like reference pixel for which also timing and different reverse substrate biases were studied.

## 2.2. Circuitry and mode of operation

Figure 2a shows the circuitry used to control and read out the “active reset” pixels studied in this paper. The chain of multiplexers and buffers in the periphery selects the matrix to be looked at. The pixel circuitry is instantiated 64 times, to read out the central 64 pixels of a  $10 \times 10$ -pixel matrix simultaneously. The source follower M1 acts as a buffer that isolates the sensing diode from the readout circuit, which is formed by M3–M5. The overall gain of this chain is slightly below unity, but uniform (within  $\approx 1\%$ ) across pixels. The multiplexing scheme eventually limits the bandwidth of the Investigator circuit to below 100 MHz.

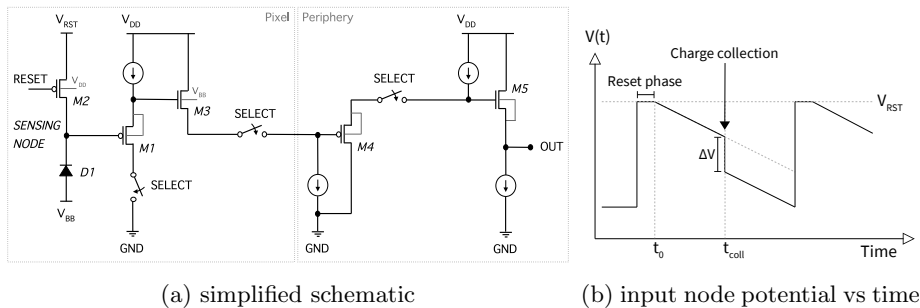


Figure 2: (a) Circuitry of the pixels discussed in this paper along with the matrix selection and output buffer circuitry. (b) Output voltage signal as a function of time. The input node potential is brought to  $V_{RST}$  by closing M2 (reset phase) and is slowly decreased by the leakage of D1 (enlarged for illustrative purposes). A charge collection is observed as a potential drop  $\Delta V$  on D1 which is brought to the output pin.

The signal formation and acquisition is illustrated in Fig. 2b, and works as follows:

1. During the reset phase the PMOS M2 is activated and the pixel diode is charged to  $V_{RST} = 0.8\text{ V}$ .
2. The pixel potential decreases slowly due to the leakage of D1.
3. If a charge  $Q$  is collected the potential drops as  $\Delta V = Q/C$ , with  $C$  being the pixel capacitance.
4. The potential continues to decrease due to leakage.
5. The next reset phase is entered in a periodic fashion.

The duration of the reset phase and the repetition frequency of the sequence are tuned such that the reset is long enough to fully restore the nominal potential

and that the leakage does not change the potential significantly in absence of particle hits<sup>5</sup>.

### 3. Measurement set-up

#### 3.1. Readout system

The Investigator readout system [14] features 64 14-bit ADCs with 65 MHz sampling rate, allowing the parallel readout of the central  $8 \times 8$  pixels in a matrix. It is operated in free-running mode, where reset pulses are given periodically to the pixels. Between the resets the signal is continuously monitored for a sudden potential drop in any of the 64 channels. When this trigger event<sup>6</sup> happens, the acquisition window of 1024 samples between the two reset pulses is stored for all channels.

Figure 3 shows an example event. The signal of a pixel is defined as the voltage step observed at the moment of charge collection. It is extracted from the recorded wave forms as the difference of the averages of samples before and after the triggering voltage step. The fact that the charge collection can last for several sampling periods is taken care of by sampling sufficiently far away from the triggering sample ( $>30$  samples). In the event in Fig. 3, the conversion presumably happened close to the boundary of two pixels and the generated charge is shared among them. The collection is rather slow, which can be attributed to a contribution from diffusion.

The following quantities are extracted from the recorded signals:

- **cluster:** the set of edge-adjacent pixels, which exceeded a given threshold.
- **cluster size:** the number of pixels with signal above  $100 e^-$  contributing to a cluster<sup>7</sup>,
- **seed pixel:** the pixel with the largest collected charge in a cluster, e.g. pixel (2, 2) in Fig. 3,
- **seed signal:** the charge collected by the seed pixel,
- **matrix signal:** the total charge collected in a  $3 \times 3$ -pixel matrix centred at the seed signal (see Fig. 3),,
- **one-pixel cluster:** a cluster with only one pixel with signal above threshold, and all neighbour pixels with signal below 1 mV (two times the electronic noise),
- **rise time constant:** time constant of the fit to an exponential of a pixel signal (see Fig. 3 and Sec. 4.2).

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<sup>5</sup>The reset phase duration was set to  $3 \mu\text{s}$ , the acquisition window was opened  $9.2 \mu\text{s}$  after the reset phase ended and it lasted for  $15.7 \mu\text{s}$ . During the acquisition window, in absence of particle hits, the average observed voltage reduction was  $<1 \text{ mV}$ .

<sup>6</sup>More technically, the acquisition trigger is given by difference between two consecutive ADC samples being larger than defined threshold; in this paper 100 ADC counts or approximately 12 mV.

<sup>7</sup>The value of  $100 e^-$  is chosen to allow for a direct comparison with other, both analogue and digital, MAPS.

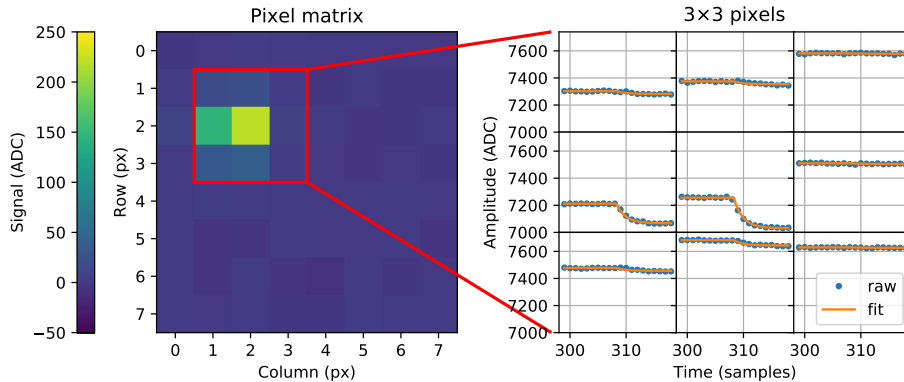


Figure 3: Example of a raw Investigator event showing the extracted signal for the full  $8 \times 8$ -pixel matrix as well as a zoom of a  $3 \times 3$ -pixel matrix (marked in red) with  $\pm 10$  samples around the trigger time (here at sample 309). The geometry and bias parameters for this example are:  $25 \mu\text{m}$ -thick epitaxial layer,  $2 \mu\text{m}$ -wide diode n-well,  $3 \mu\text{m}$  spacing,  $-1 \text{ V}$  reverse substrate bias. One ADC count corresponds to roughly  $0.12 \text{ mV}$  and one time bin to  $15 \text{ ns}$ . For a description of the fit see Sec. 4.2.

### 3.2. *Fe-55* source

An  $^{55}\text{Fe}$  source was used for the measurements carried out in this paper. It produces two characteristic soft X-rays at around  $5.9 \text{ keV}$  ( $K_\alpha$ ) and  $6.5 \text{ keV}$  ( $K_\beta$ ) to which MAPS are sensitive [16].

It is a convenient source for these studies: the deposited charge is comparable to that of minimum ionising particles traversing sensitive layers of  $20 \mu\text{m}$  to  $30 \mu\text{m}$ , and the absorption probability is adequate (absorption lengths of  $\approx 30 \mu\text{m}$  [17]), while at the same time not introducing a too strong non-uniformity. The main interaction process for these X-rays in silicon is photoelectric absorption [17]. An electron emitted by the photoelectric absorption at those energies, generates electron-hole pairs within  $1 \mu\text{m}$  of its origin [18], which can be treated here as point-like charge deposition.

The two X-ray energies are known to release on average  $1640 e^-$  and  $1800 e^-$  in silicon, respectively, and can hence be used to calibrate the sensor signal in terms of charge. In this respect, the  $K_\alpha$ -peak at  $1640 e^-$  is referred to as “calibration peak”. A charge calibration is performed to be able to better compare different pixel geometries and bias settings in terms of charge sharing; note also that a threshold of  $100 e^-$  is used to define the cluster size.

The observed signal shape of an  $^{55}\text{Fe}$  X-ray depends on the position where its absorption takes place with respect to the geometry of the detector. Three primary regions of interest can be identified:

- **High electric field region:** The electron-hole pairs are created inside the high electric field region below a collection electrode. They are directly collected by drift, resulting in a one-pixel cluster.
- **Low or no electric field region in the epitaxial layer:** The charge transport mechanism is dominantly thermal diffusion until the carriers

reach a high electric field region and are collected (or until they recombine). The deposited charge can be shared between several pixels due to the statistical nature of the diffusion process.

- **Substrate:** Electrons diffuse thermally in the substrate. Their lifetime before recombination is small, such that only a fraction reaches the epitaxial layer. The part reaching the epitaxial layer is collected as above.

In the first two cases, the entire charge deposited by the photo electron is expected to be collected, given the relatively long carrier lifetime with respect to the collection time. In the third case the amount of collected charge depends on the depth of the photoelectric conversion and the carrier lifetime in the substrate.

The carrier lifetime varies by orders of magnitude from low-doping (epitaxial layer) to high-doping regions (substrate), i.e. changes from above 10  $\mu\text{s}$  to below 20 ns, respectively<sup>8</sup>. Furthermore, the diffusion coefficient in the substrate is an order of magnitude lower than in the epitaxial layer [20]. Therefore, only a limited amount of electrons generated in the substrate is collected. In particular, only the photons converted in the first 5  $\mu\text{m}$  of the substrate are measurable [21].

Figure 4 shows a selection of recorded signal spectra. Here, both the  $3 \times 3$ -pixel matrix signal and the seed pixel signal are shown. The latter is further detailed into cases where the cluster size is one. The double-peak structure from the  $K_\alpha$  and  $K_\beta$   $^{55}\text{Fe}$  X-rays is immediately visible, in particular in the matrix and best in the one-pixel spectra. The seed pixel signal spectra show an increased frequency at around one third to one half of the  $K_\alpha$ -peak, which is attributed to the events where charge is shared between pixels. The matrix spectra contain a long tail originating from X-ray conversions in the substrate, where the generated electrons are only partially captured.

## 4. Results

The measurements are split in two categories, first the asymptotic time behaviour of the charge collection is studied, then, the time response is studied for a selected pixel geometry.

### 4.1. Asymptotic charge collection

The following quantities are extracted from the  $^{55}\text{Fe}$  measurements and are summarised in Fig. 5:

- **Charge collection ratio:** The ratio of the most-probable value of the  $3 \times 3$ -pixel matrix signal distribution to the most-probable value of the

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<sup>8</sup>Values estimated using  $\tau(N_A) = \left(1 + \frac{N_A}{N_{\text{ref}}}\right)^{-1} \tau_{\text{max}}$  [19], with  $\tau_{\text{max}} = 10^{-5}$  s,  $N_{\text{ref}} = 10^{16} \text{ cm}^{-3}$ , and  $N_A$  equal to  $9 \times 10^{11} \text{ cm}^{-3}$  and  $5 \times 10^{18} \text{ cm}^{-3}$  in the epitaxial layer and the substrate, respectively.

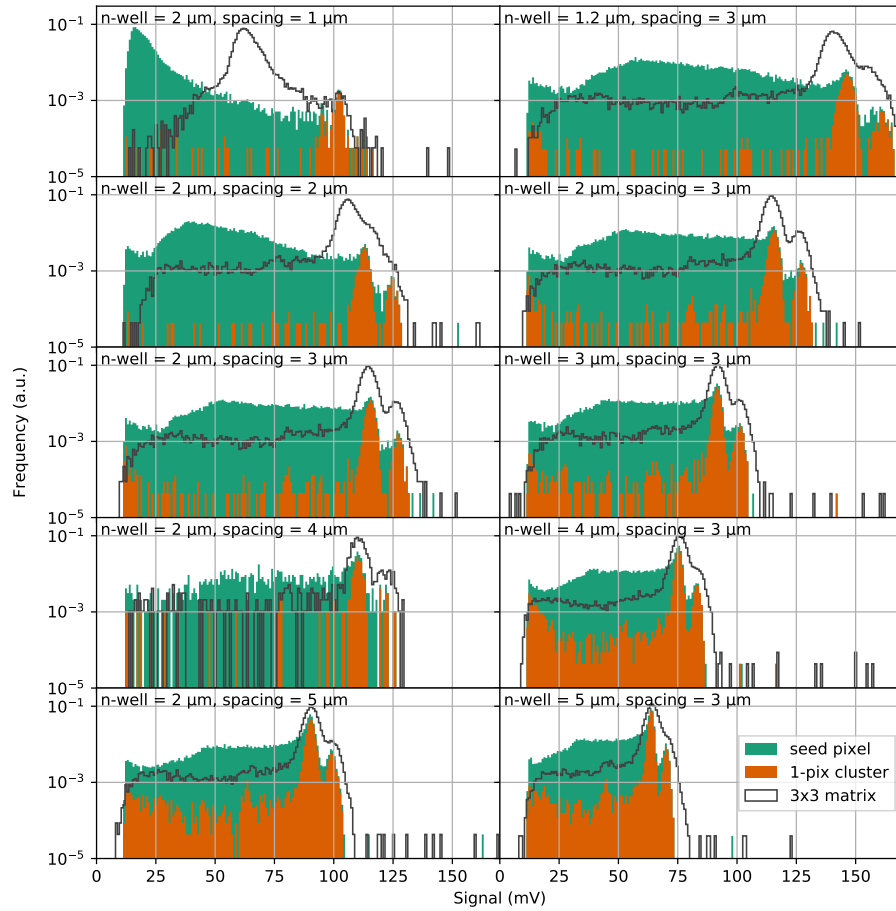


Figure 4: Example Fe-55 spectra for nine different diode geometries on a 25  $\mu\text{m}$ -thick epitaxial layer and reverse substrate bias of  $-6\text{ V}$ . The left column shows the effect of changing the spacing, the right the effect of changing the diode n-well size.



one-pixel cluster signal distribution. It is an indicator of the charge collection efficiency<sup>9</sup>.

- **Calibration peak:** The amplitude of the calibration peak (expressed as voltage) seen in the seed signal distribution (the  $1640 e^-$  from the 5.9 keV X-ray). It is an indication<sup>10</sup> of the pixel capacitance ( $C = Q/\Delta V$ ).
- **Fraction of one-pixel clusters:** The relative number of clusters of size one with respect to the total number of clusters. This quantity indicates the relative spatial extension of high electric field volume of a pixel (see Sec. 3.2).
- **Average cluster size:** A higher average cluster size is an indication of a higher charge sharing between pixels.

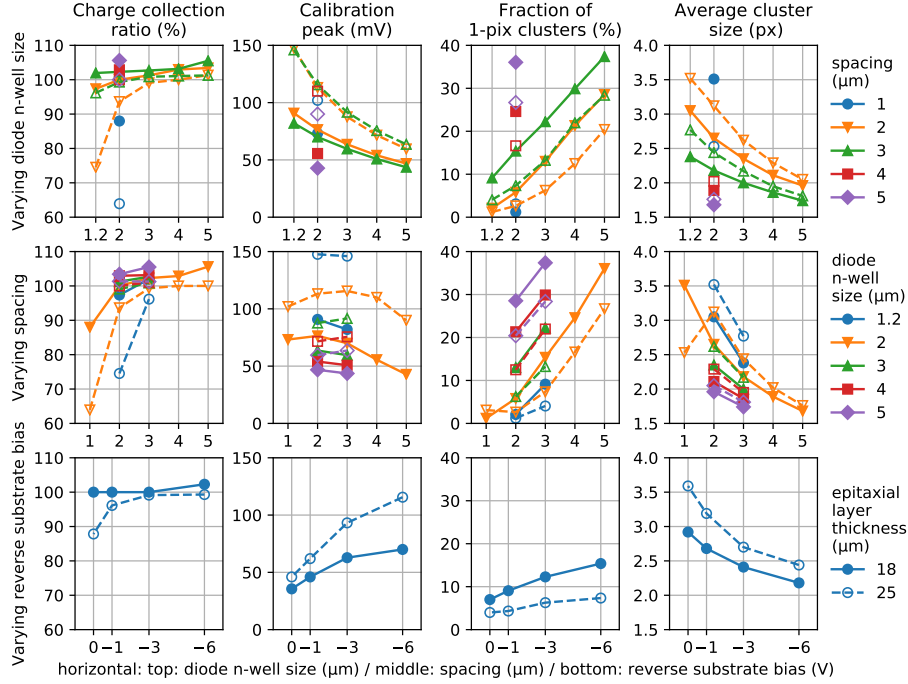


Figure 5: Extracted asymptotic charge collection parameters. The two top rows show the dependence on geometric parameters for a fixed reverse substrate bias of  $-6 V$ , the bottom row shows the influence of the reverse substrate bias for a fixed geometry with diode n-well size of  $2 \mu m$  and spacing of  $3 \mu m$ . All figures contain data from epitaxial layer heights of  $18 \mu m$  (solid lines, closed symbols) and  $25 \mu m$  (dashed lines, open symbols). See text for the definition of the parameters.

<sup>9</sup>The intrinsic assumption here is that in a one-pixel cluster the entire deposited charge is collected by one pixel. However, as a small amount of charge can be still be collected by other pixels (visible in slightly skewed one-pixel cluster distributions in Fig. 4), thus resulting in a ratio above 100 %.

<sup>10</sup>It is an indication only, as the voltage gain of the circuit is not known precisely enough.

Several trends can be observed, most of which can qualitatively be described by the change of the depletion volume i.e. the electric field and associated changes of capacitance and charge collection mechanism:

1. It can be clearly observed that the extreme choices of smallest diode n-wells or smallest spacing yield bad results in the sense that charges are being lost.
2. Increasing the diode n-well size or the spacing lead to different trade-offs between signal amplitude and charge sharing. Here it is worth mentioning that *some* charge sharing is typically (and certainly for the ALICE application) desirable as it can increase the spatial resolution of the sensor. However, charge sharing also divides the charge over several pixels thus putting higher requirements on the ability to resolve smaller signal and leading to a lower radiation hardness.
3. A thicker epitaxial layer leads to more charge sharing and needs a more careful tuning of the geometry. For tracking charged particles, however, it has the advantage that the induced signal is larger (scales with path length).
4. Reverse substrate bias has a very large influence on the performance of the sensor, generally being beneficial.

In these observations, a larger spacing leads to two competing mechanisms onto the capacitance of the input node: the well capacitance decreases due to a larger depletion, but the capacitance of the metal line connection of the diode n-well to the first input transistor (residing in the deep p-well) increases as it becomes longer.

The trade-off made for the ALPIDE chip for ALICE Inner Tracker System is a 2  $\mu\text{m}$ -wide well with a 3  $\mu\text{m}$  spacing on a 25  $\mu\text{m}$  epitaxial layer. The bias voltage is adjustable [2, 3, 4].

#### 4.2. Time-resolved charge collection

The Investigator chip and its readout system allow to resolve the time response of a pixel down to values around 15 ns, mostly determined by the bandwidths of the chip and the readout system as well as the sampling rate. In the absence of an external trigger in the measurement of X-rays, the charge collection time is defined as the time constant  $\tau$  extracted from a fit of an exponential step-response to the signal:

$$V(t) = \begin{cases} V_0 & t < t_0 \\ V_0 - \Delta V \cdot [1 - \exp(-(t - t_0)/\tau)] & t \geq t_0 \end{cases} . \quad (1)$$

Such a fit is for example shown in the right-hand panel of Fig. 3. It should be noted that this fitting procedure allows to obtain  $t_0$  and  $\tau$  with sub-sample resolution. Also note that the time  $T_{90\%}$  to collect 90% of total collected charge would be equivalent to  $\approx 2.3 \tau$  in this model.

Figure 6 shows the extracted time constants of seed pixel signals for different values of reverse substrate bias and signal amplitude. It can be observed

that there are no measured time constants below  $\approx 8$  ns, due to the bandwidth-induced limit of the system, but many signals are hitting this limit. This result, the time constant equivalent to the system bandwidth, can be regarded as the main result already – it shows that the dominant charge collection process is drift rather than diffusion. In particular the calibration peaks are collected very fast, confirming the previous assumption that the calibration peak originates mostly from the collection by drift.

Figure 7 compares the time responses for different reverse substrate bias voltages and epitaxial layer thicknesses, also indicating the time response of the 10 %-quantile of signals with the highest amplitude, corresponding to the area where the seed signal is found. The following observations can be made:

1. The time constant of the calibration peak is at the minimum measurable value given by the system resolution (i.e.  $< 10$  ns) for all cases.
2. A thicker epitaxial layer needs more reverse substrate bias to reach high collection speeds throughout the full volume. The part collected in the high electric field volume (calibration peak) shows comparable speeds (below system resolution).
3. The contributions to the signal attributed formerly to the low electric field part of the sensor become faster with more bias voltage, eventually reaching the system resolution over their full range at  $V_{BB} = -6$  V.

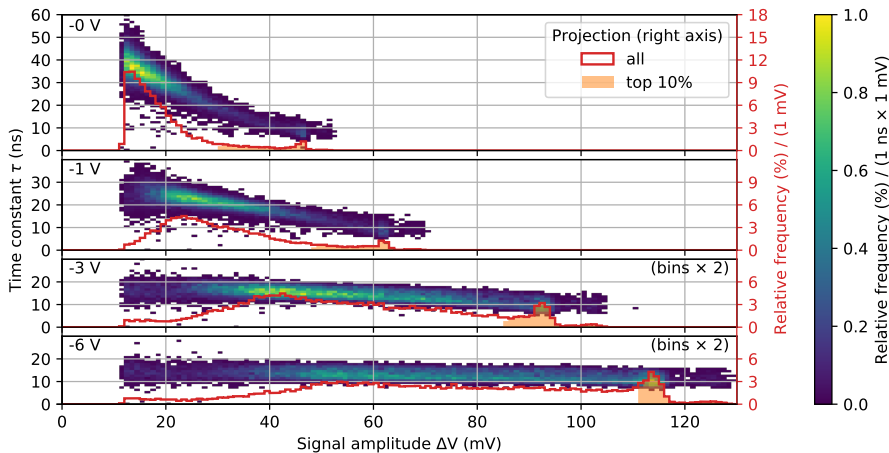


Figure 6: Time response of seed signal versus its amplitude for different values of reverse substrate bias for a pixel with diode n-well size of  $2 \mu\text{m}$  and spacing of  $3 \mu\text{m}$  on a  $25 \mu\text{m}$ -thick epitaxial layer. The right-hand vertical axis shows the projection onto signal amplitude, showing the seed signal spectrum. The highlighted part corresponds to the 10 %-quantile of signals with the highest amplitude.

## 5. Summary

The parametric study of different pixel designs shows the influence of geometric parameters, of the choice of epitaxial layer and of the bias conditions.

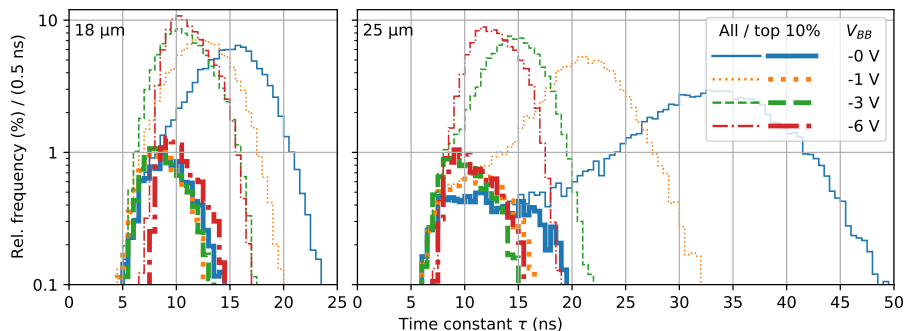


Figure 7: Distribution of signal time constants for different reverse substrate bias voltages and epitaxial layer thicknesses. The thick lines correspond to the 10%-quantile of signals with the highest amplitude, which can be largely attributed to collection within the high electric field volume (cf. Fig. 6). The studied pixel has a diode n-well size of  $2\ \mu\text{m}$  and a spacing of  $3\ \mu\text{m}$ .

While the observed trends can be understood qualitatively by simple arguments, their quantitative importance is more involved. The reported measurements can, hence, serve as reference for choosing design parameters in future developments and as benchmark of more detailed simulations.

In particular, it is worth emphasising the influence of adding an undoped gap (spacing) between the diode n-well and the surrounding p-well. It turns out to be the key parameter to largely improve the performance at a relatively small penalties in terms of capacitance increase and area requirement.

The presented results show that fast charge collections are obtainable in these kind of sensors. This naturally raises an interest of applications requiring  $O(\text{ns})$ -time resolutions or, given that the dominant charge collection mechanism is drift, radiation hardness. Eventually, in order to time-resolve the signal generation and collection of these type of sensors, a new chip and readout system with larger bandwidth would be required in the future.

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