Global Trigger Technological Demonstrator for ATLAS Phase-II upgrade

Experimentelle Teilchen- und Astroteilchen-Physik

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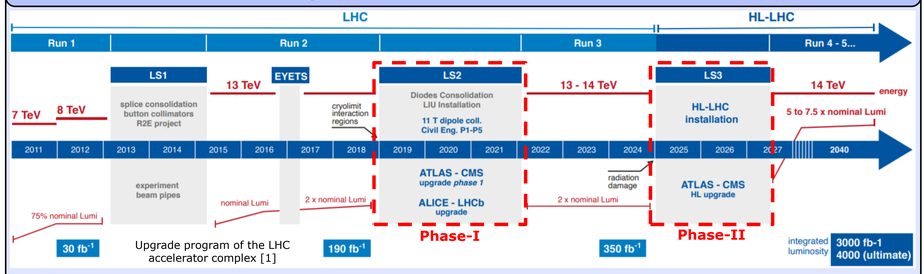
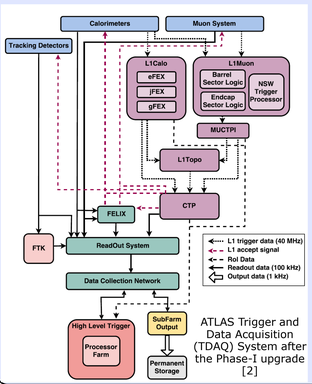
ATLAS TDAQ from Phase-I to Phase-II



Upgrade program of the LHC accelerator complex [1]

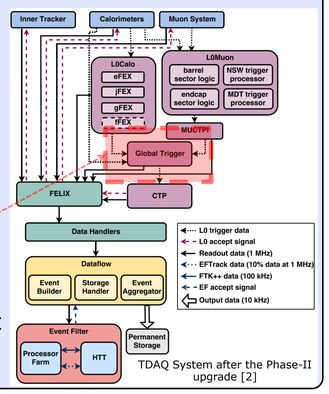


ATLAS Trigger and Data Acquisition (TDAQ) System after the Phase-I upgrade [2]

L1Calo → L0Calo
- Additional forward FEX system (fFEX)

L1Muon → L0Muon
- Additional Muon trigger processor

L1Topo → Global Trigger
- Full replacement
- Additional full granularity cells input
- Offline-style algorithms



TDAQ System after the Phase-II upgrade [2]

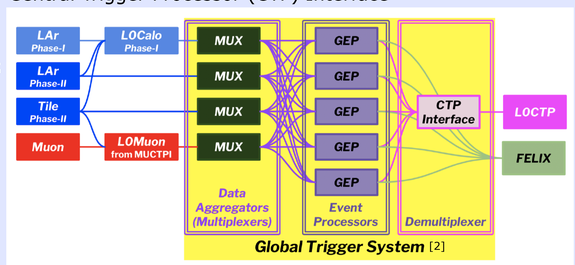
Phase-II Global Trigger System

Functionality

- Uses full-granularity calorimeter cells (|E|>2σ) to refine L0Calo & L0Muon output
- Allows iterative algorithms such as topoclustering and use of higher level synthesis
- Reconstructs taus, jets, MET, & calorimeter-based isolation
- Applies topological requirements

Implementation

- Time-multiplexed system concentrates data of full event into a single processor
- Composed of 3 main layers
  - Multiplexing (MUX) layer
  - Global Event Processor (GEP) layer
  - Demultiplexing Global-to-Central Trigger Processor (CTP) Interface
- Input: >2300 optical fibers with link speeds up to 25.8 Gb/s
- Global Common Module (GCM) is used as the building block in each layer



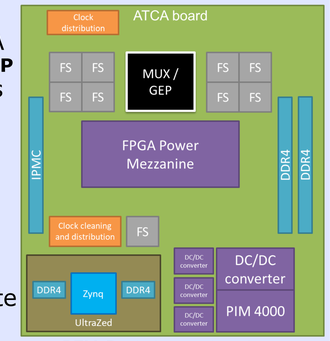
PFM

Functionality

- Production Firmware Deployment Module (PFM) represents a slice of the GCM
- Allows testing and debugging algorithm and infrastructure firmware for the Global Trigger System

Implementation

- ATCA board
- Single MUX/GEP FPGA
  - Xilinx Ultrascale+ **VU13P**
- Up to 9 **Finisar BOA**s
- UltraZed board with **Zynq** UltraScale+
- **DDR4** RAMs
- Design based on the Technological Demonstrator R&D
- PCB design is complete



PFM Prototype structure

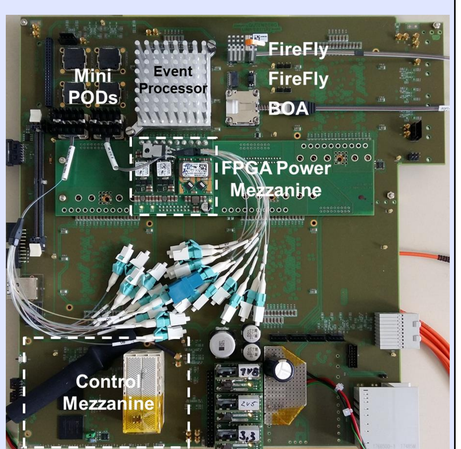
Technological Demonstrator

Motivation

- R&D for the new generation of **optical modules** at **high data rates** up to 25.8 Gb/s **implemented on-board**
- Interfaced with an FPGA

Hardware overview

- **Custom designed** ATCA board
- Xilinx Virtex **UltraScale+ 9P** FPGA
- **Samtec FireFly** 28G 2x4 bidirectional
- **Finisar BOA** 28G 2x12 bidirectional
- MiniPODs
- Mezzanines: Power, Control



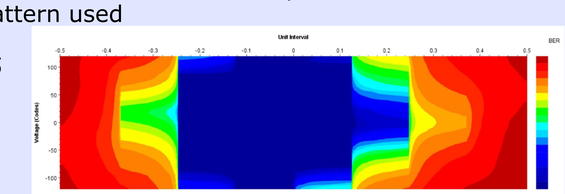
Technological Demonstrator

Performance evaluation

- Performance of the high-speed optical modules and the FPGA on the Technological Demonstrator has been evaluated with long-run loopback Integrated Bit Error Ratio Tests (IBERT)

Finisar BOA

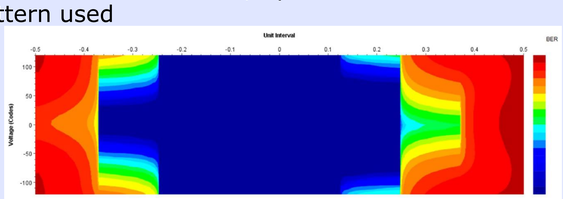
- 12 transmitter links of the optical module were looped back to 12 receiver links of the same module with a help of a 24 to 2x12-fiber Y-cable and a 12-fiber trunk cable
- Day-long IBERT test run at 25.65 Gb/s performed
- 31-bit PRBS pattern used
- BER < 1.9E-15
- All 12 links functional
- No bit errors
- Good performance



Finisar BOA IBERT loopback test: a typical eye diagram

Samtec FireFly

- 4 transmitter links of the optical module were looped back to 4 receiver links of the same module with a help of a 12-fiber MTP to LC breakout cable
- Day-long IBERT test run at 27.58 Gb/s performed
- 31-bit PRBS pattern used
- BER < 1.7E-15
- All 4 links functional
- No bit errors
- Very good performance



Samtec FireFly IBERT loopback test: a typical eye diagram

- A good performance and absence of bit errors during long runs have been demonstrated for both high-speed optical modules implemented on-board. Due to a higher link density and a good performance, Finisar BOA is used for the PFM Prototype.

http://www.etap.physik.uni-mainz.de/atlas

http://atlas.ch

References:
[1] Upgrade program of the LHC accelerator complex, https://project-hl-lhc-industry.web.cern.ch/sites/project-hl-lhc-industry.web.cern.ch/files/inline-images/HL-LHC-plan-2020-Plan-2.pdf
[2] ATLAS Collaboration, "Technical Design Report for the Phase II Upgrade of the ATLAS TDAQ System", CERN-LHCC-2017-020.

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