

Firmware developments on the TileCoM for the Phase-II Upgrade of the ATLAS Tile Calorimeter

Mpho Gift Doctor Gololo¹, Fernando Carrio Argos², Filipe Martins³ and Bruce Mellado¹

ICPPA-2020, 5-9 October 2020, Moscow, Russia

¹Institute for Collider Particle Physics, University of the Witwatersrand and iThemba LABS, mpho.gift.doctor.gololo@cern.ch, Bruce.Mellado.Garcia@cern.ch; ²Instituto de Física Corpuscular, University of Valencia, fernando.carrio@cern.ch; ³Laboratório de Instrumentação e Física Experimental de Partículas, filipe.martins@cern.ch

Abstract

The Tile Computer on Module (TileCoM) mezzanine board is one of the auxiliary boards of the Tile PreProcessor (TilePPr) for the Phase-II Upgrade of the readout electronics of the ATLAS Tile Calorimeter (TileCal). This board will be responsible for system monitoring and configuration by interfacing the Trigger Data Acquisition (TDAQ) system and the TilePPr. Features include configuration and monitoring of the Advanced Telecommunications Computing Architecture (ATCA) carrier and Compact Processing Module (CPM) onboard sensors through I2C and Gigabit Ethernet. This contribution presents firmware developments on an embedded Linux for the ZYNQ System-on-Chip (SoC) targeting an Avnet Ultra96-V2 Zynq UltraScale+ MPSoC evaluation board. This test bench will serve as a basis for the development of the main functionalities of the TileCoM mezzanine board to interface the TilePPr with the Detector Control System (DCS) and the TDAQ system of the Tile Calorimeter.

ATLAS TileCal Phase-II Upgrade

TileCal aged legacy electronics will not be able to withstand the new radiation requirements of the High Luminosity Large Hadron Collider (HL-LHC). The Phase-II Upgrade of TileCal will replace the legacy system with a fully-digital TDAQ and trigger processing, reading out the whole detector at 40 MHz at Level 0 trigger level (Figure 1).

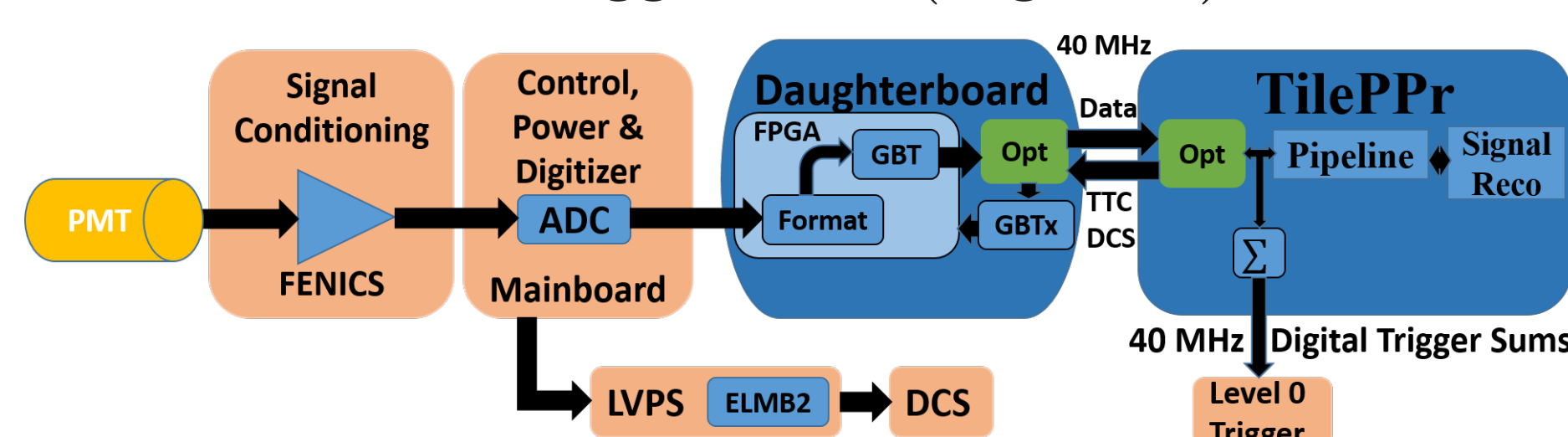


Figure 1: TileCal Phase-II Upgrade [1]

The TilePPr

The TilePPr sends LHC synchronized clocks and configuration commands to the on-detector electronics, while receiving monitoring information and PMT samples through MGBps optic fibers. The TilePPr provides remote configuration capabilities for the on- and off-detector electronics through the TileCoM. The TileCoM is accessed through the network via a Tile 16 GbE port switch (Figure 2).

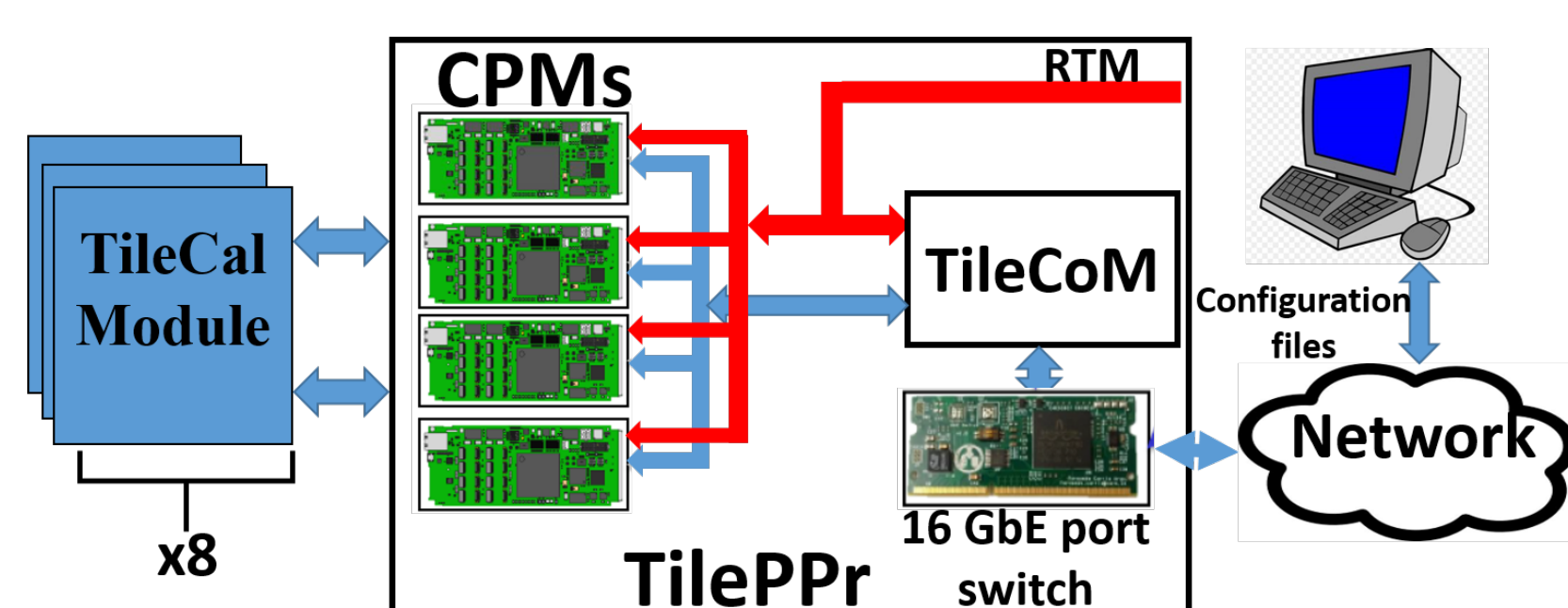


Figure 2: TilePPr interface with the network[1]

Firmware implemented on the TileCoM evaluation board

1. TileCoM functionalities:

- To remotely program the on- and off-detector FPGAs by sending bitstreams through the Xilinx Virtual Cable.
- To provide slow control and configuration capabilities; including an interface with the TDAQ to monitor and configure the TilePPr and the on-detector electronics.
- To provide monitoring data to the DCS through the Open Platform Communications (OPC) Unified Automation (UA) server implemented on the ARM processor of the Zynq SoC.

2. OPC-DCS interface:

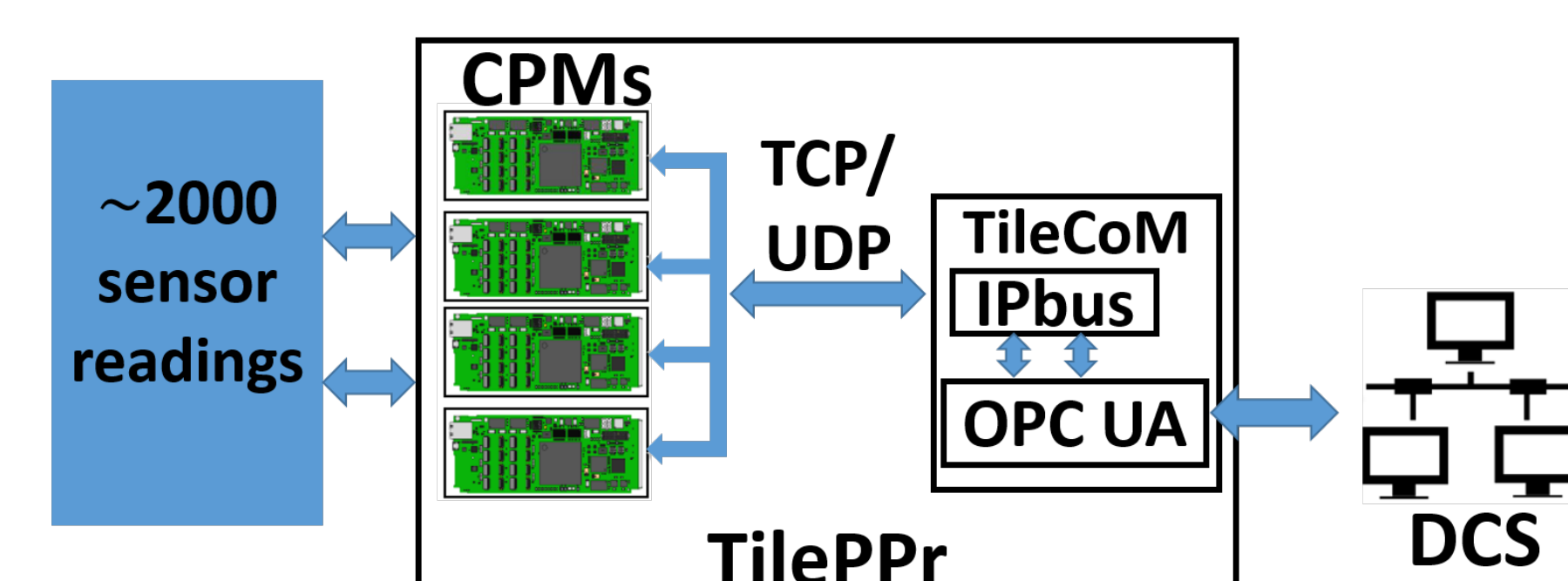


Figure 3: The TilePPr-DCS interface [2]

3. Ironman firmware overview:

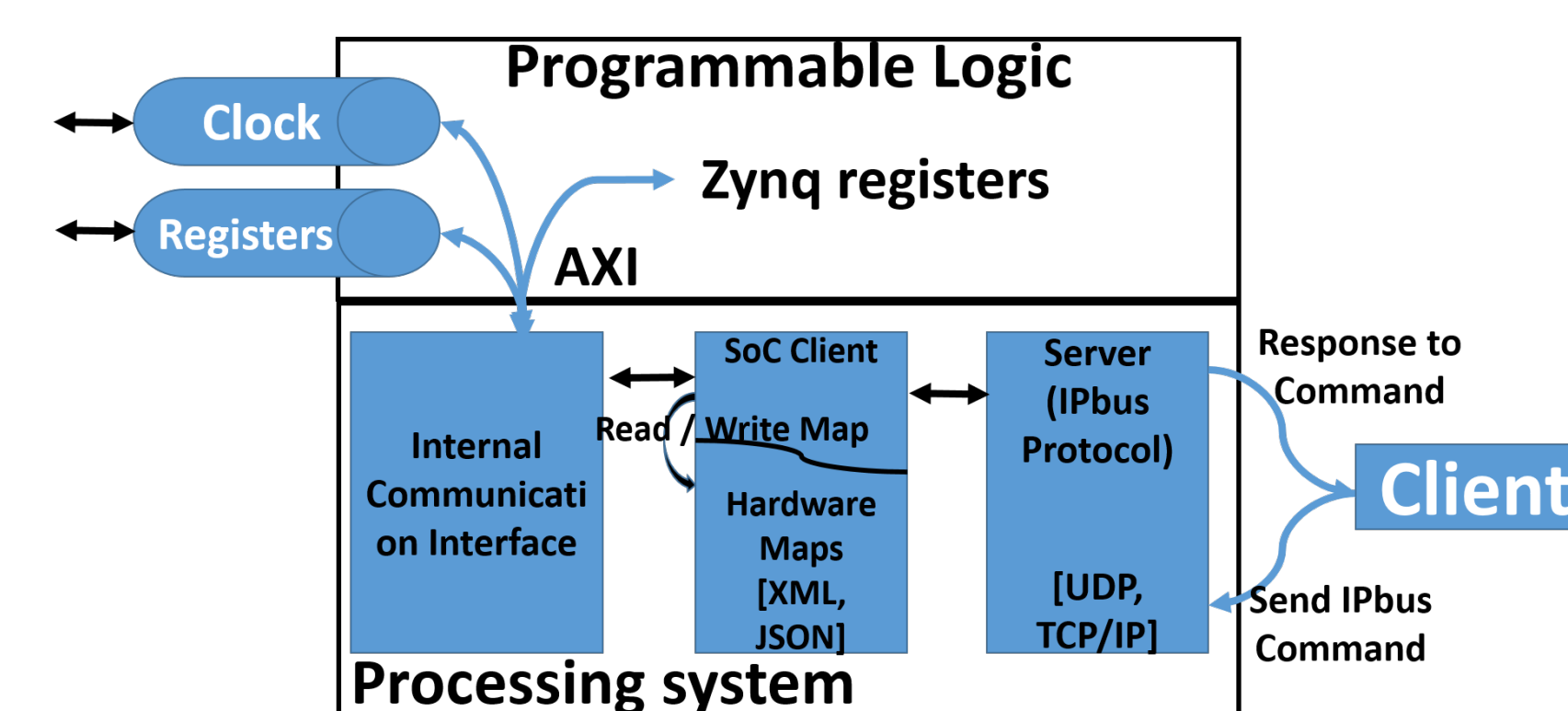


Figure 4: Ironman firmware overview [3]

OPC is implemented on a CentOS 8 embedded Linux on the ZYNQ System-on-Chip (SoC) using quasar. An open source OPC UA backend C++ Toolkit called Open62541 is used for the implementation of the server. UA Expert is used as a client to access the server running on the SoC. Figure 3 shows an interface between the TilePPr and DCS.

The Ironman software employed in the L1Calo integrated with IPbus [4] is used as a base to implement the firmware for the TileCoM. The software uses standard twisted protocol applications such as a reactor model, which is an event driven model global loop that fires listeners when certain events have been triggered (Figure 4). The SoC client analyzes the incoming packet more thoroughly and sends requests to the hardware. The response is sent back to the client through the server.

Experimental setup and results

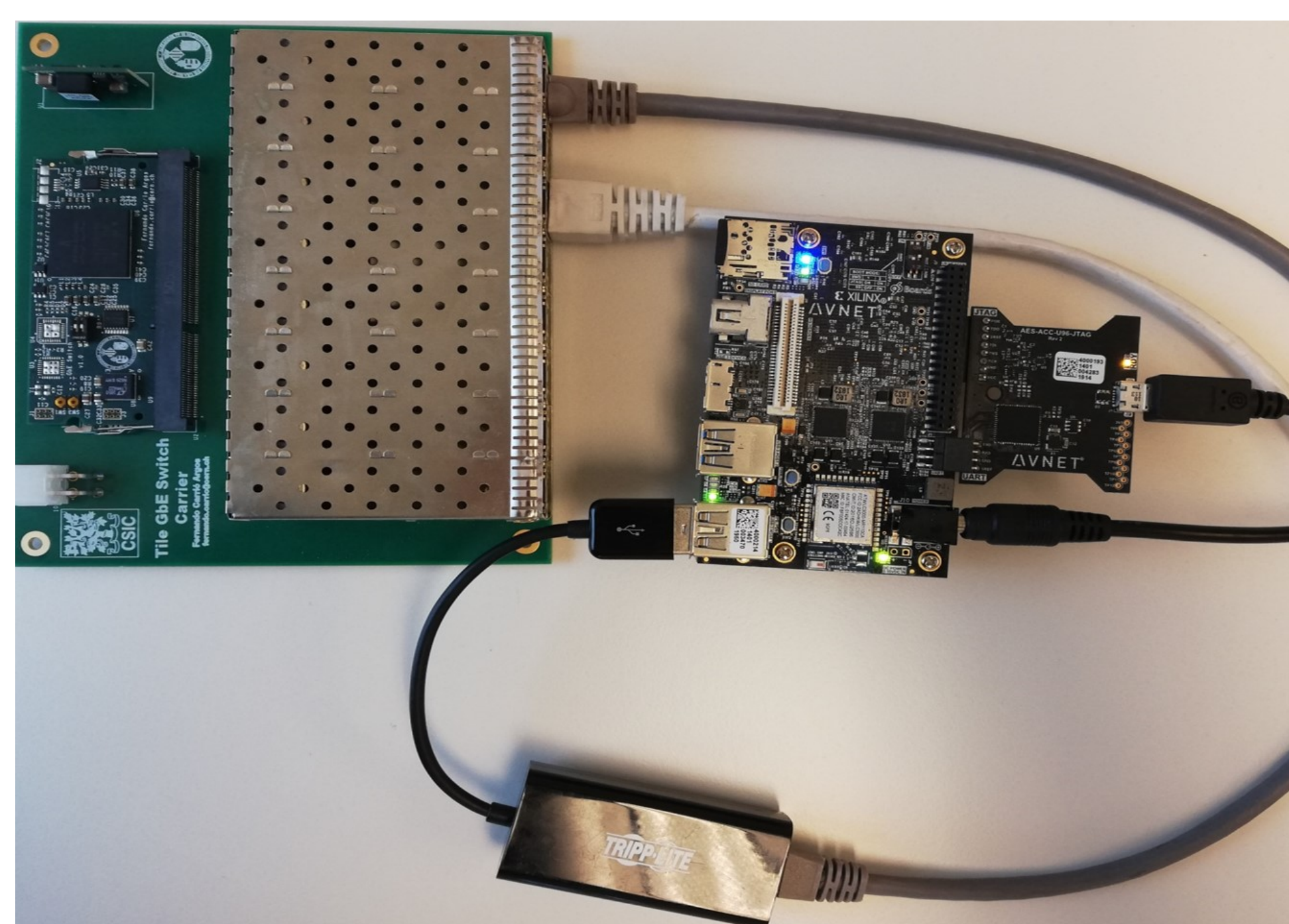


Figure 5: TileCoM testbench running server

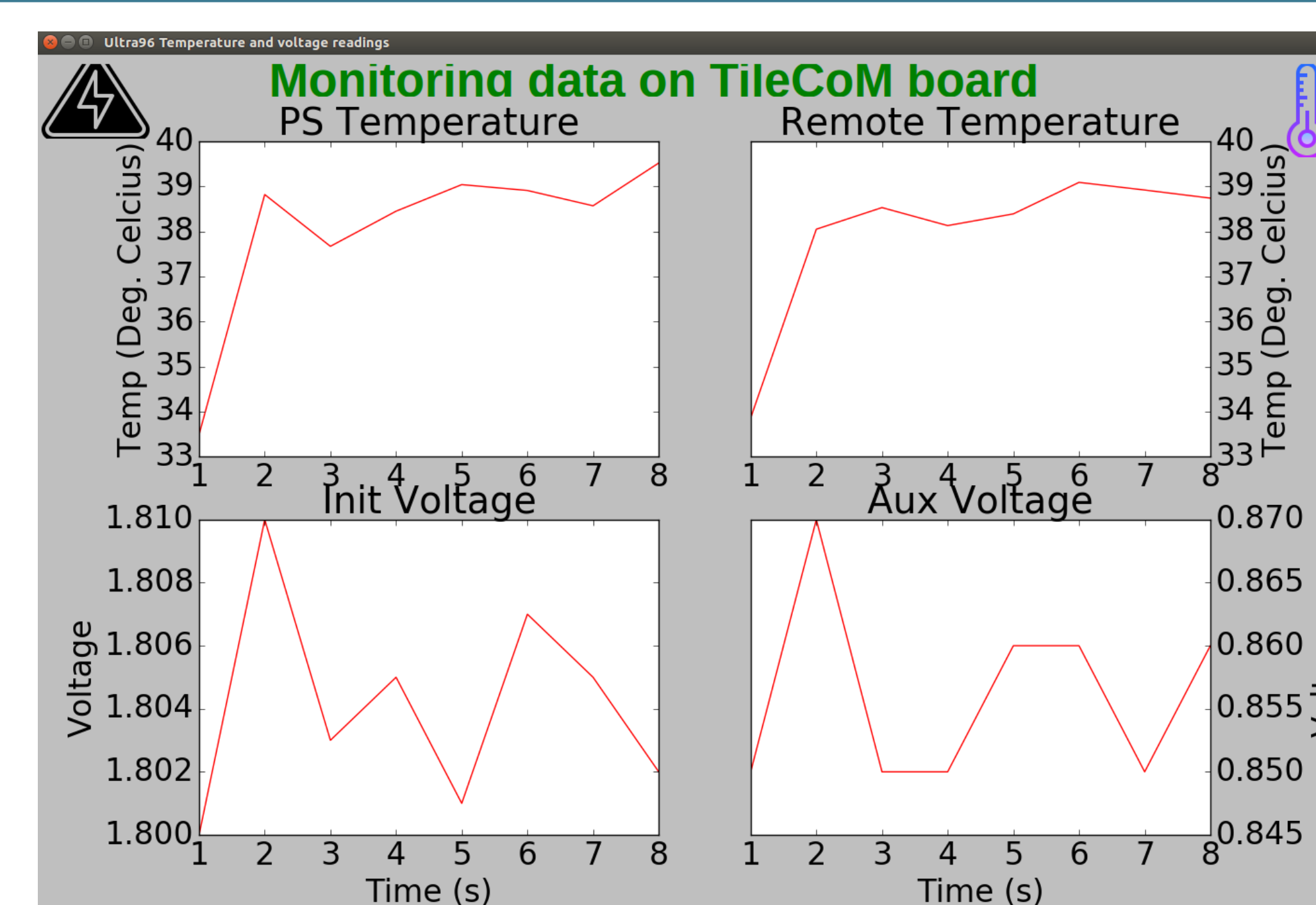


Figure 6: Client application on PyQt5

The testbench shown on Figure 5 and the readout results shown in Figure 6, exhibit the communication achieved between the implemented server and client using Twisted libraries. The evaluation board consists of the processing system and the programming logic that are capable of numerous applications.

The IPbus server is implemented directly on the on the processing system of the zynq architecture of the Ultra96-V2 Zynq UltraScale+ MPSoC TileCoM evaluation board. The client is implemented with Twisted libraries and PyQt5 on Ubuntu 18.04 to read out Xilinx Analog-to-Digital Converters temperature and voltages.

Summary and references

The firmware developments presented in this contribution are a test run for the TilePPr development boards for the ATLAS Tile Calorimeter Phase-II Upgrade. The implementation of the IPbus firmware and software on the TileCoM board have been tested with the Tile 16 GbE port switch. These development boards are connected and accessed remotely to read out temperature and voltages.

- [1] Einsweiler, Kevin, Pontecorvo, Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter. <https://cds.cern.ch/record/2285583?ln=en>.
- [2] H. Santos, The ATLAS TileCal Detector Control System. 10.1109/RTC.2010.5750473.
- [3] G. Stark, E. Smith and F. Tang, ATLAS-L1 Calo Ironman firmware. <https://github.com/kratsg/ironman>.
- [4] C. Larrea, IPbus: Ethernet-based control system for xTCA hardware. 10.1088/1748-0221/10/02/C02019.