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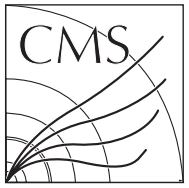

The Compact Muon Solenoid Experiment

Conference Report

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Serial powering in four-chip prototype RD53A modules for Phase 2 upgrade of the CMS pixel detector

Vasilije Perovic for the CMS Tracker Group

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Serial powering in four-chip prototype RD53A modules for Phase 2 upgrade of the CMS pixel detector

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Abstract

Serial powering is the baseline choice for the upgrade of the CMS pixel detector for the High Luminosity LHC. The first results with the four-chip prototype pixel detector modules based on the demonstrator 65 nm CMOS technology RD53A chip are presented. The serially powered chain is operated at a constant supply current and the regulation is performed on-chip using a shunt low-dropout regulator (SLDO). Chips on each module are powered in parallel to prevent single-point failures. The SLDO behaviour in the system is presented as well as relevant differences in the behaviour compared to single chips. The noise levels are measured in pixels of a module in a serially powered chain and no increase is observed compared to a single module or the reported noise levels for a single chip.

Keywords: serial powering, shunt low-dropout regulator, CMS pixel detector, RD53A

1. Motivation for the serial powering

The Large Hadron Collider (LHC) [1] will be upgraded during the Long Shutdown from 2024 to 2026 to increase the instantaneous luminosity up to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The upgraded accelerator, called High Luminosity LHC (HL-LHC) [2], aims to reach $4000\,\mathrm{fb}^{-1}$ of integrated luminosity over ten years of operation. While gaining physics potential by increasing the luminosity, the conditions at the HL-LHC require the experiments be upgraded and parts of the detectors replaced. The Compact Muon Solenoid (CMS) experiment

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will undergo a substantial upgrade for the HL-LHC programme [3], part of which is the installation of a new silicon Tracker [4]. The inner part of the Tracker, consisting of hybrid silicon pixel modules, will be exposed to the highest rates of particles per unit area. To achieve good tracking performance, the granularity of the pixel detector must be increased, as well as the size of on-chip memory. A prototype chip meeting these requirements was developed by the RD53 Collaboration. The prototype chip, RD53A [5], is designed in 65 nm CMOS technology and is about half the size of the final chip. The increased granularity results in the higher supply current required for the chip. This is further increased by the low operating voltage of 1.2 V, resulting in up to 1 A supply current for RD53A, and up to 2 A for the final chip. The pixel detector will consist of more than 13000 chips. Should the modules be powered in parallel, the high total current would lead to either high power losses or high mass of cables within the volume of the detector. The baseline choice for the powering of the pixel modules in CMS is therefore a serial scheme, in which a serial chain of modules is powered by a constant current. Small scale demonstrators for the serial powering have been produced [6, 7, 8] but never deployed in a high energy physics experiment. An immediate and profound consequence of this scheme is that the modules in a chain must have an independent on-chip voltage regulation, capable of powering the chip while taking constant current from the supply. This regulator is discussed in the next section. Results with prototype chips and modules are shown in Section 3.

2. Shunt low-dropout regulator

The required supply current for any chip varies with time because of the variations in the load on the digital circuitry of the chip. In addition, chip-to-chip variations imply that an external power supply is not able to provide general voltage regulation to such a chip. Therefore a custom radiation-hard [9, 10] on-chip shunt low-dropout regulator (SLDO) [11] is implemented in RD53A. It consists of two parts, the shunt, and the low-dropout regulator. Since the system is powered at constant supply current which must exceed the maximum current required by any module at any moment, the excess current is shunted by the regulator. Short variations in the load are filtered by the on-module decoupling capacitors. A simplified schematic diagram of the SLDO is shown in Figure 1. The regulator also provides an on-chip reference voltage because all modules of a serial chain have different local

grounds. In this arrangement the regulator behaves as an ohmic load to the power supply. The impedance is constant in time and for a particular supply current, and is set using an external resistor. Therefore such chips can be powered in either series or parallel.

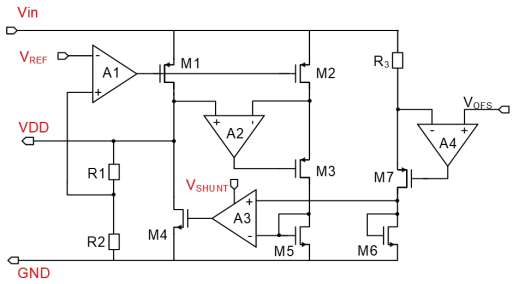


Figure 1: Shunt low-dropout regulator, SLDO. The regulator shunts the excess current in serial powering and the LDO provides the constant regulated voltage. The regulator is an ohmic load to the power supply, set by the offset voltage, resistor R3 and the current mirror ratio. Adapted from [5].

Should a simple serial powering scheme be used, where single chips are powered in series, a failure of one chip could compromise the entire chain. Therefore the serially powered hybrid modules consist of four or two [4] chips powered in parallel. The current sharing is dictated by the resistive behaviour of the regulators. Should a chip on a module fail into an open circuit, the chain is not compromised and the remaining chip(s) on the same module must shunt a higher current. Therefore the SLDO is able to shunt currents about twice the required by the chip. In case the failure mode of a chip is a short-circuit, the module is compromised in its entirety but the serial chain is not affected since this would only shift the potentials of the local grounds.

Every chip has two independent SLDO regulators, one for the digital and one for the analog domain of the chip. In addition, both are decoupled by a set of on-module capacitors. This insulates the sensitive analog circuitry from the relatively noisier digital circuitry. The serial powering scheme is illustrated in Figure 2. While the chain is powered by a constant supply current, only the ground of the last module is connected to the power supply ground. The communication is therefore done using a configurable number of AC-coupled differential electrical links. On-detector opto-electronic conversion modules, which are based on the lpGBT chip set, are used to merge data from the differential electrical links into optical links, which transfer the

data to the off-detector DAQ system [4].

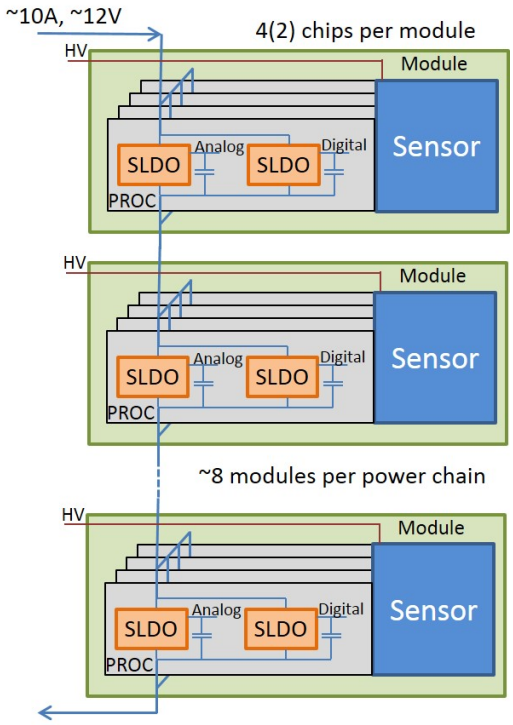


Figure 2: Schematic diagram of the serial powering scheme. Each chip has two shunt low-dropout regulators (SLDOs) to decouple the noise in the digital circuitry from the sensitive analog circuitry. Two or four chips are powered in parallel on a single module to prevent single-point failures. Up to 11 modules are connected in a chain and the sensors are biased in parallel w.r.t. local grounds. Sensors operating on lower voltages may need higher granularity in HV distribution. Adapted from [5].

In addition to the powering for the readout chips, the foreseen sensors [12, 13] in the hybrid modules require a high voltage bias which is distributed in parallel and referenced to module grounds. If the high voltage is sufficiently high and the sensor performance is not affected by the bias voltage fluctuation within the range of the variation among the module ground potentials, this scheme can be deployed. Otherwise, the high voltage distribution granularity needs to be increased. To test the serial powering scheme, single-chip RD53A cards have been powered in series [14]. Further tests with single chip cards powered in parallel to emulate the powering on a single hybrid module are

presented in the next section, as well as the results with the first RD53A four-chip modules.

3. Results

Single chip cards. A single chip SLDO I-V characteristic is shown in Figure 3. A constant current is supplied. The outputs of the analog (VDDA) and the digital (VDDD) regulators, and the input voltage are shown. If the supplied current is sufficient, above $\sim 0.75\,\mathrm{A}$, the voltage references are generated by the band gaps and the regulator output is constant, while the input behaves like an ohmic load. At the point of switching on, the impedance of the regulator increases. The slope of the input I-V curve is set by an external precision resistor R3 and the current mirror formed by resistors M1 and M2 in Figure 1.

If the supply current is now reduced, we observe a hysteresis as shown in Figure 4. The chip may therefore be operated at a current below the threshold required to start the SLDO regulator. A benefit of the hysteresis is that the state of the regulator is insensitive to small current fluctuations. Figure 5 shows an example of the regulated voltages from four different single chips tested independently. The hysteresis is observed in all cases. The chip-to-chip variation can be attributed to production variation. If the chips shown in Figure 5 are powered in parallel to emulate the powering scheme on a single hybrid module, the current sharing is affected by the increase in the impedance of the regulator when it is switched on. The current taken by a regulator is reduced at that moment, increasing the current supplied to the other chips powered in parallel, leading to all regulators switching on at the same current as shown in Figure 6.

Four-chip RD53A modules. Prototype RD53A modules have been built [15, 16]. A module is illustrated in Figure 7. The supply current and the readout data communication is provided via the high density interconnect (HDI). The HDI contains connectors and passive components only. All active circuitry is contained in the chip. A sensor is bump-bonded to the chip, but the tests presented here are performed without a sensor. The four chips are wire-bonded to the HDI. A passive fan-out distributes the current to the chips, whose grounds are connected to the downstream power connector where the next module in the serial chain is connected. At the last module in the chain, the return current is routed back via the HDI. Figure 8 shows the results of

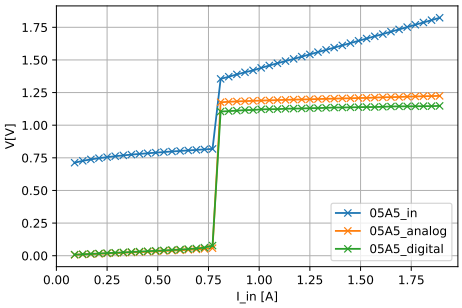


Figure 3: The V-I characteristic of the SLDO. When the current is increased above $\sim$0.75 A the impedance of the SLDO increases and the outputs are constant for further increase in the current. The slope of the input voltage is set by an external resistor in the SLDO circuit.

a single four-chip module. The input voltage spread of about 50 mV is due to the variation in resistance of the routing in the HDI. This is consistent with the simulations of the power density in the HDI [15] and has been improved in the newer versions of the HDI. The regulated voltages of both analog and digital regulators, as well as the input voltages, show the same behaviour as the single chips powered in parallel. The remaining visible chip-to-chip variation in the regulator output is at the start-up. This is due to the variation in the SLDO start-up circuitry. This circuitry does not affect the input impedance of the SLDO and therefore does not experience any positive feedback from the other chips powered in parallel.

Serially powered RD53A modules. We can now perform the same V-I characterisation with three modules powered in series. Voltages are measured at the inputs of each module, referenced to the power supply ground. The result is shown in Figure 9. Since only the potential of the last module in the chain is determined by the power supply and other modules have floating local grounds, every probed voltage in the chain depends only on the modules that are below it in the chain. Furthermore, modules in this configuration are independent and chip-to-chip variations are now seen as module-to-module variations. Different modules have different minimum required current for the regulators to switch on. Figure 9 shows the points where the modules that are below the test point switch on. The return line shows purely ohmic behaviour as expected. In this configuration the system could be sensitive to

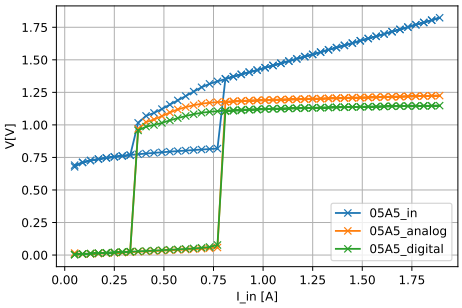


Figure 4: The V-I characteristic of the SLDO. The threshold to change the state of the SLDO depends on the state of the SLDO, exhibiting hysteresis. This makes the state of the SLDO insensitive to the small fluctuations in the supply current.

load transients, however the simulations [17] show that the scheme is insensitive to the load transients because of the local regulation and decoupling. Therefore the system should be insensitive to noise. The noise is measured as a part of chip calibration.

The chip allows the injection of charge into individual pixels for the purposes of calibration. For a set threshold, the occupancy in each pixel is measured as a function of the injected charge. In principle, this should be a step function in a noise-free system, at the point where the threshold is exceeded. In a real system this curve is smeared and provides information about noise for each pixel. In the linear front end of the RD53A prototype modules the measured noise is around 70 electrons, consistent with the reported noise levels per pixel for the linear front end of a chip with no sensor [18]. The noise is measured for each pixel in a module and the measurement is repeated for the same module in the chain after retuning of the local thresholds. The pixel-by-pixel noise increase is shown in Figure 10 and no overall increase in noise is observed. In addition, a noise map for a module in the chain is shown in Figure 11. Only the linear front end is used and the masked pixels are shown in white. Any effect of connecting a module in a serially powered chain on the noise would either be an overall change in the noise level in the system or patterns of the module-scale size in the noise map. No such patterns are observed in the noise map.

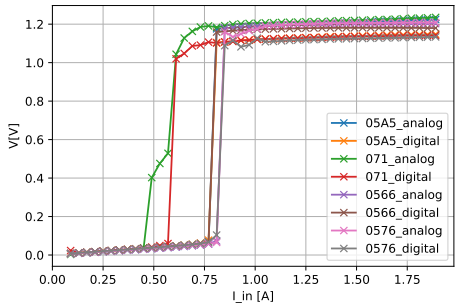


Figure 5: Regulated voltages for four single chips. All chips exhibit hysteresis. We observe chip-to-chip variation in the regulated voltage and in the threshold current for the SLDO to switch on. The regulated voltage can be finely tuned using registers in the chip.

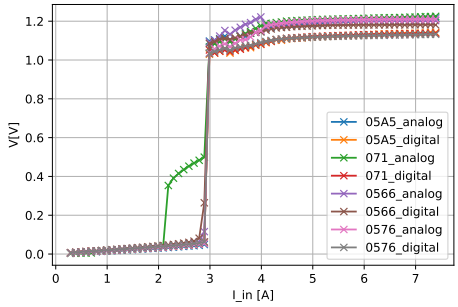


Figure 6: Regulated voltages for four chips powered in parallel. Even if there is chip-to-chip variation in the threshold, the positive feedback from the increase in the impedance when the SLDO is switched on, and the hysteresis observed earlier, lead to changes in the current sharing during the current ramp such that all SLDOs start at the same current.

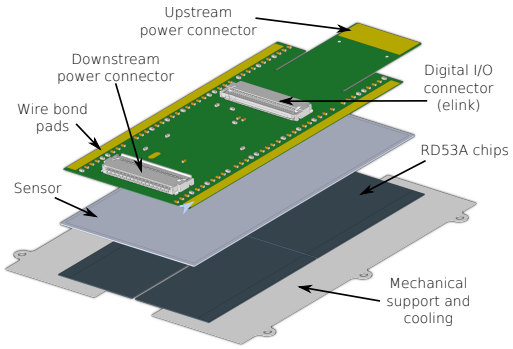
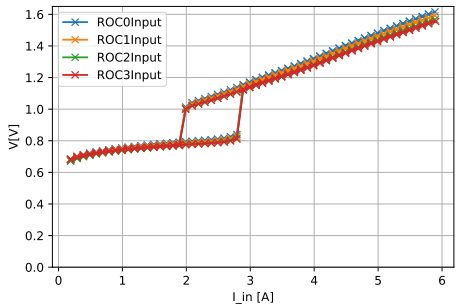
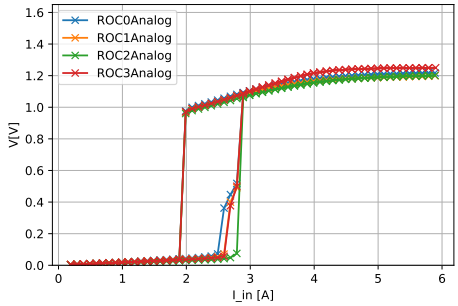


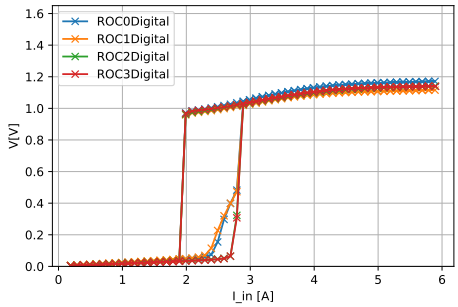
Figure 7: A model of the four-chip RD53A module. The HDI distributes the current to the four wire-bonded RD53A chips. The decoupling capacitors and external resistors are on the HDI. All active circuitry is contained within the chip. The modules are connected in series such that the local ground of one module is connected to the input of the next module. The return current is routed via the HDI from the last module in the chain. Communication to the chip is routed via a separate connector on the HDI. Adapted from [16].



(a) Input voltage



(b) VDDA output voltage



(c) VDDD output voltage

Figure 8: The V-I characteristic of a four-chip module. The chips are powered in parallel. The input voltage (a) shows a $\sim$50 mV spread due to parasitic resistances in the HDI. The analog (b) and digital (c) power domain regulated voltages show the behaviour observed with single chips powered in parallel. Chip-to-chip variation is not observed in the hysteresis.

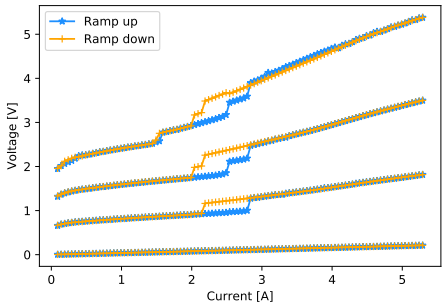


Figure 9: The V-I characteristic of a serially powered chain of three four-chip modules. Different curves represent measurements at different points in the chain, at the inputs of different modules. We now observe the effects of chip-to-chip variation as the module-to-module variation in the threshold current. Only the modules at lower potential in the serially powered chain affect the potential of a module. The return line shows purely ohmic behaviour.

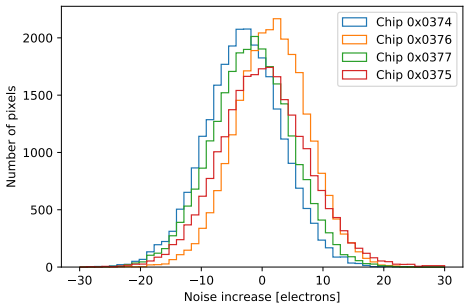


Figure 10: The noise increase for the serially powered system. The noise is measured per pixel on a single module and in the chain. After retuning, no overall increase in the noise is observed.

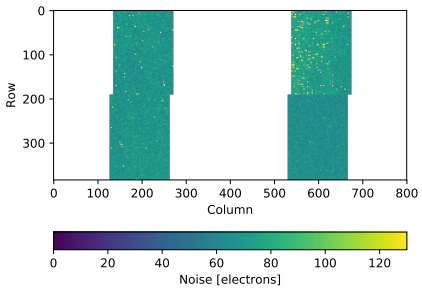


Figure 11: The noise map of a four-chip module in a serial chain. Only 136 columns are active in each chip, corresponding to the linear front end. The masked pixels are shown in white. No overall gradients or module-scale features are observed.

4. Conclusion

Serial powering is the baseline choice for the upgrade of the CMS pixel detector for the HL-LHC. The prototype test chip RD53A has got two dedicated shunt low-dropout regulators and is powered by a constant input current. While the regulator behaves as an ohmic load to the power supply, it shunts the excess current in the serial chain. Four-chip prototype modules have been built and the behaviour of the SLDOs compared to the single chips. Chips on a single module are powered in parallel and the hysteresis in the current required to switch the SLDO on or off helps all SLDOs start at the same current since the impedance of the SLDO is higher in the on-state. Parallel powering on a single module also prevents single-point failures. A chain of three serially powered modules was used and the effects of chip-to-chip variation are observed again in the minimum required current. No effect of the serial powering is seen in either the noise in the pixels or the behaviour of the SLDOs.

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