Upgrade of the ATLAS Muon Drift Tube Front-end Electronics for HL-LHC Runs

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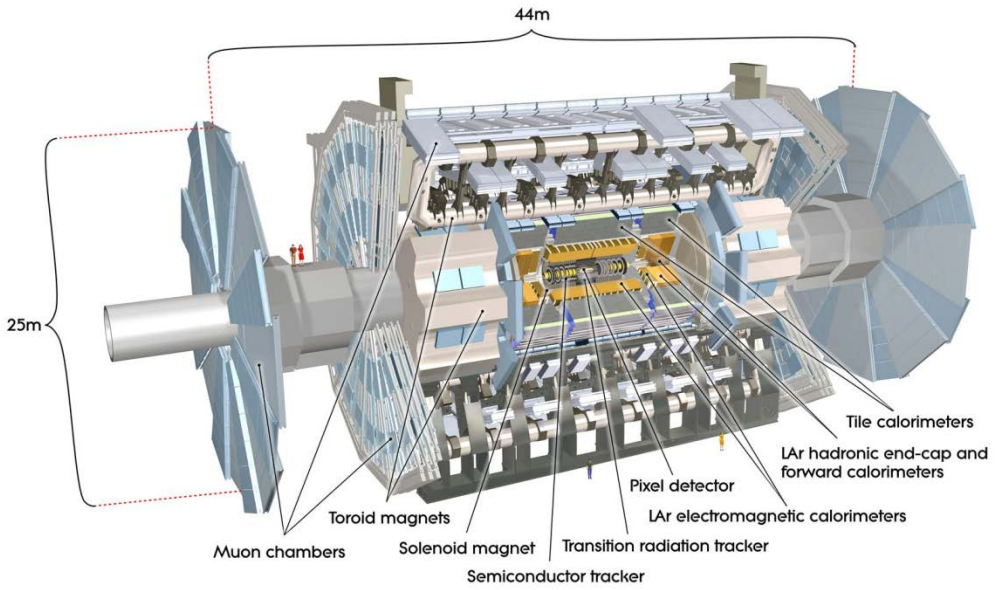
On behalf of the ATLAS Muon Collaboration

Outline

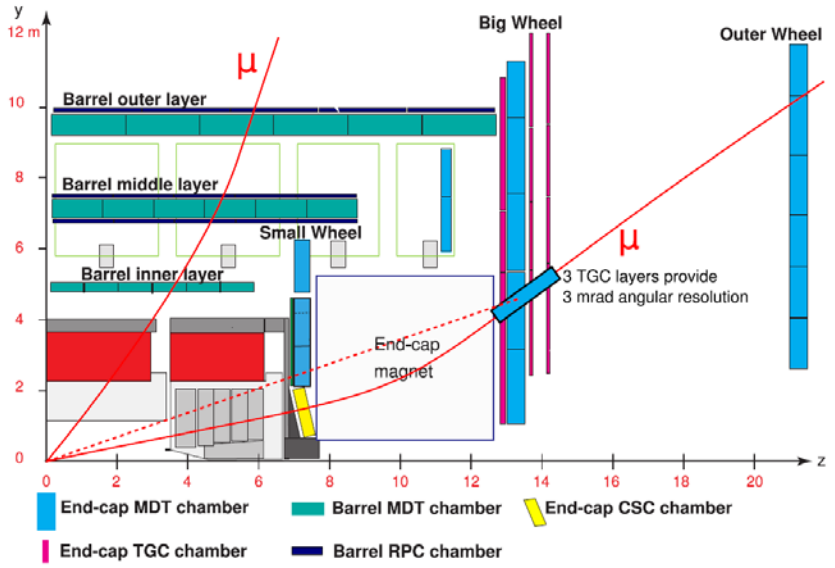
- **Introduction**
  - ATLAS MDT Detector
  - MDT Electronics System
- **Frontend Electronic System Upgrade**
  - ASD
  - TDC
  - Mezzanine Card
  - CSM
- **Integration Test Plan**
- **Summary**



Introduction

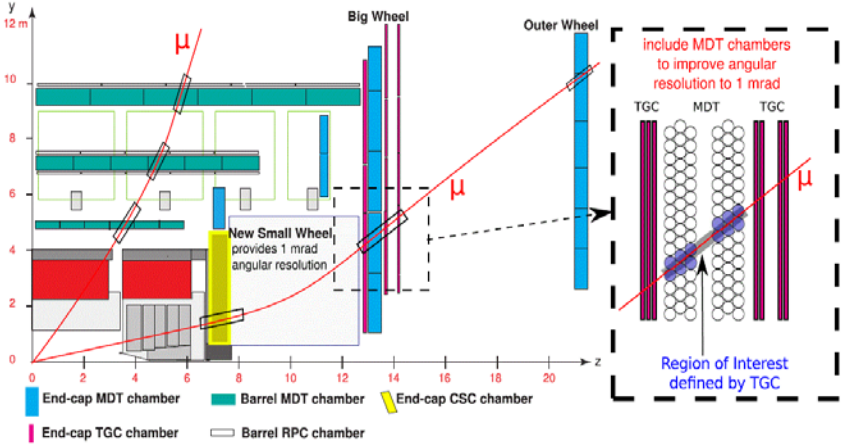
ATLAS Muon Spectrometer

- Muon triggering, identification & momentum measurement
- Resistive Plat Chambers (RPCs)/ Thin Gap Chambers (TGCs): primary trigger detectors
- Monitored Drift Tubes (MDTs)/ Cathode Strip Chambers (CSCs): precision trackers



MDT Detector Upgrade @ HL-LHC

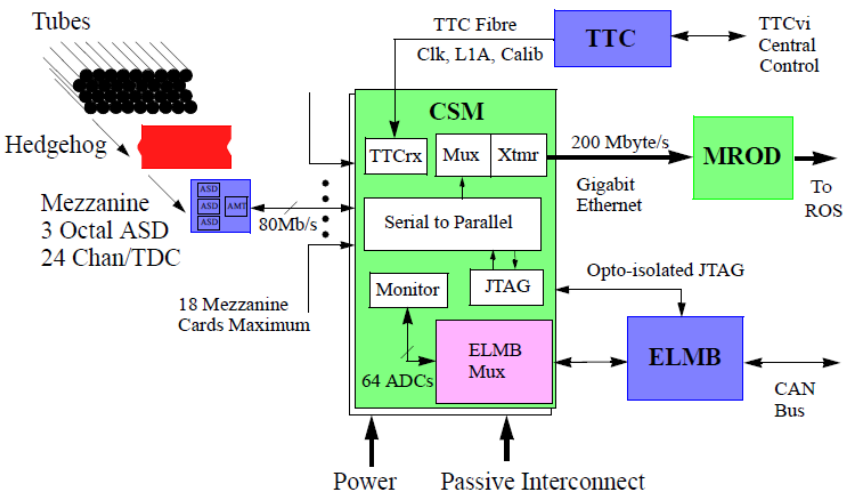
- Improve Muon transverse momentum (pT) resolution at L0 triggering
  - pT selectivity of tracks for the trigger will be improved by integrating MDT info into L0 triggering
  - RPC and sMDT chambers will replace current MDT chambers (inner barrel) to allow for a 3-station RPC trigger
- Cope with high rates
  - MDT readout electronics system must be upgraded



MDT Electronics System

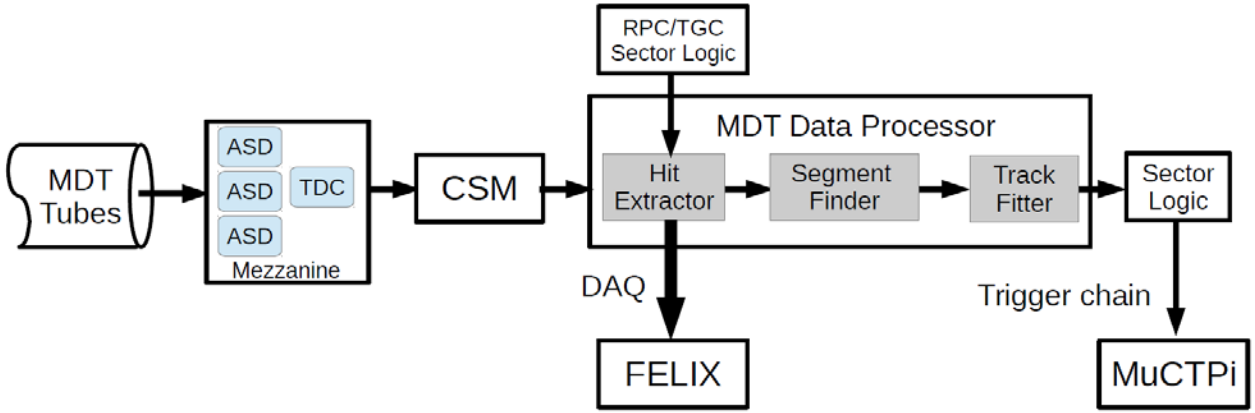
❑ MDT EIx @ Current System

- MDT & Trigger. Chambers independently R/O
  - o MDT readout only on L1 trigger → lower bandwidth
  - o Trigger mode used at the Front-end

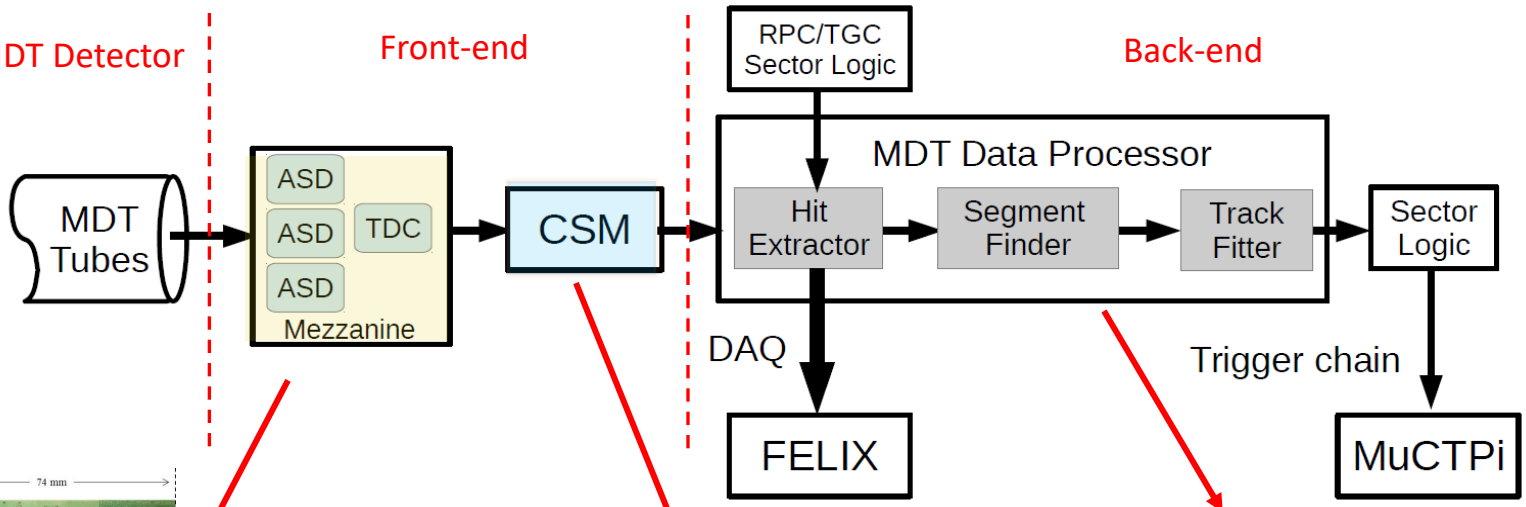


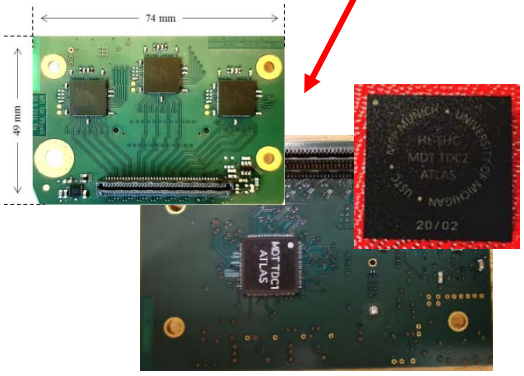
❑ MDT EIx @ HL-LHC

- MDT data "sharpen" trigger decision
  - o Find accurate pT using ROI seed from trigger chambers and confirm/reject trigger hypothesis
  - o Triggerless at FE and track fitting in the counting room → higher bandwidth

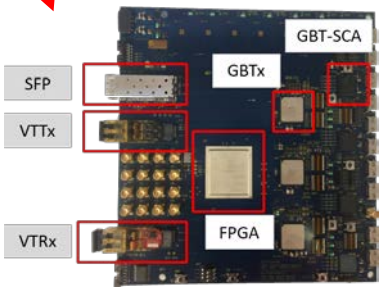


MDT Electronics System @ HL-LHC

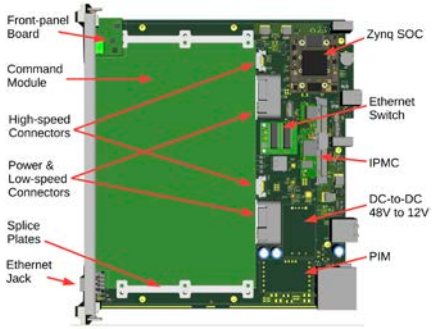




New ASD & TDC



New CSM: GBT chipset based



MDT Data Processor

- New triggerless operation
- Support higher readout bandwidth
- ~80k ASDs & ~22k TDCs will be produced

- Flexible handle both old/new Mezz.
- Fix latency & ~20Gbps bandwidth
- Will deliver 1188 boards

- Provide MDT trigger candidate to the global L0 trigger level
- Precision data readout
- Will deliver 64 ATCA cards

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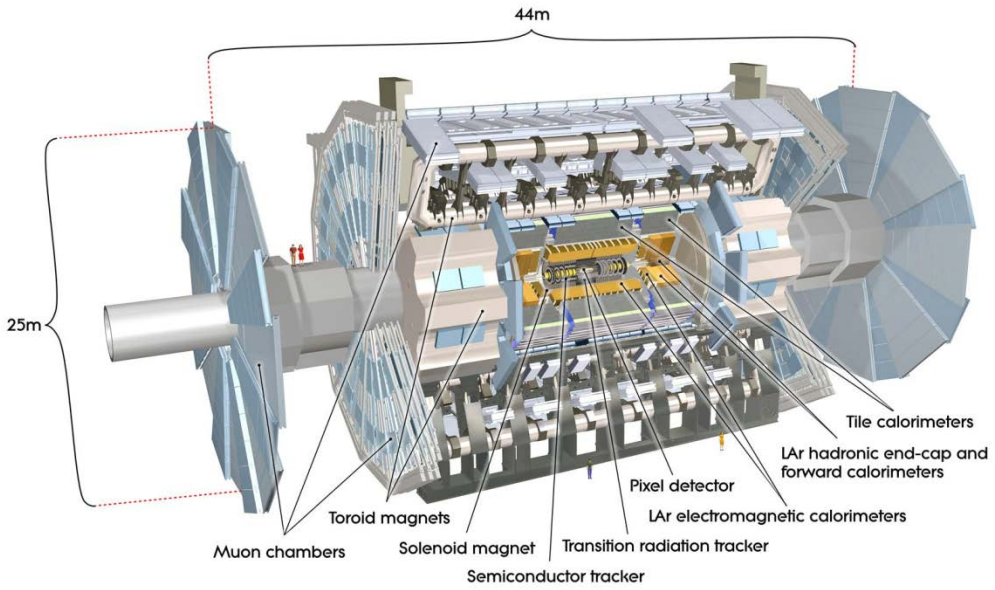
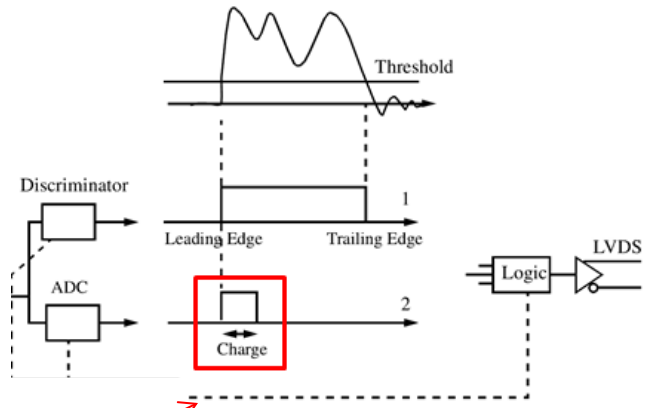


Amplifier-Shaper-Discriminator ASIC

ASD Design

- 8-Chs ASD: GF 130nm CMOS process ($7.6\ mm^2$)
- 4 key parts
  - Pre-amplifier: charge-sensitive
  - Shaper: differential amplification (DA1-DA3)
  - Wilkinson ADC & Discriminator
  - Output Driver



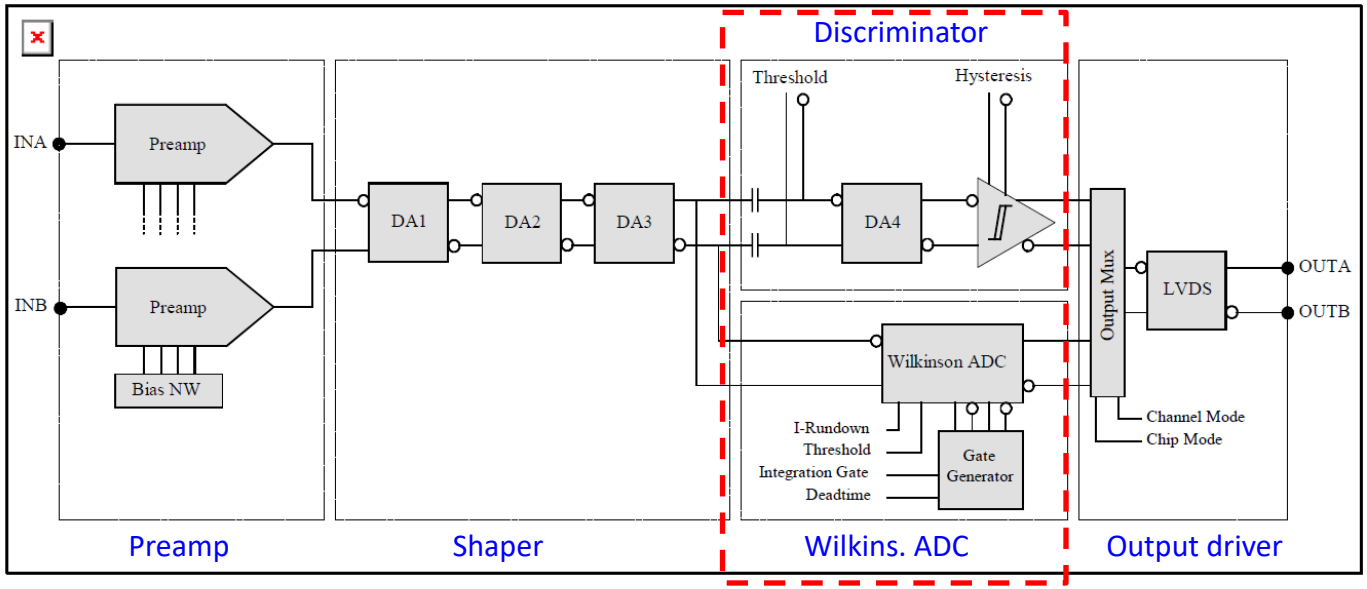
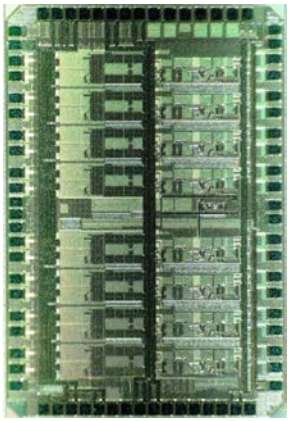


Diagram of one ASD Channel

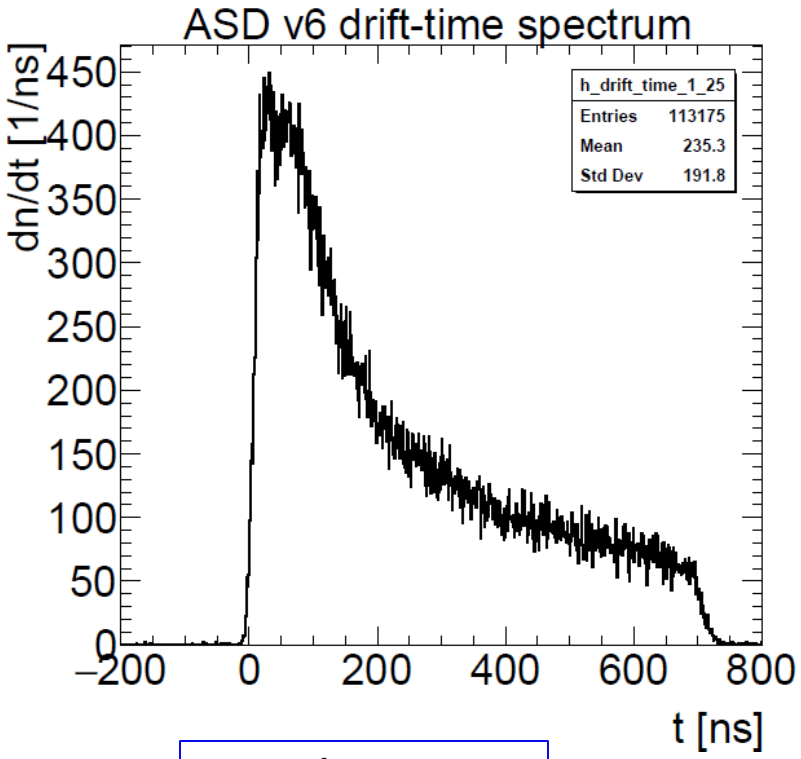


Optical photo of ASD ASIC

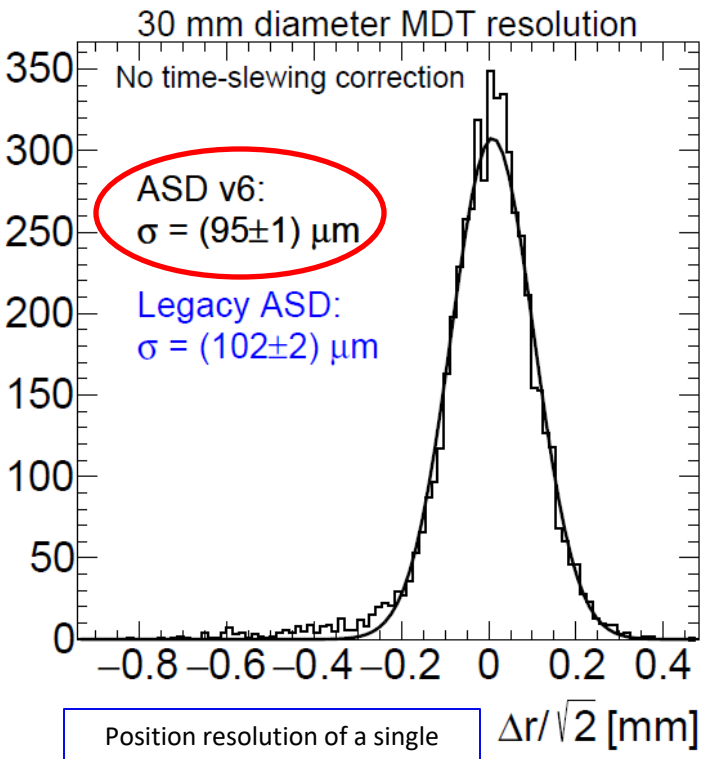
Amplifier-Shaper-Discriminator ASIC

❑ ASD Project Status

- Detailed studies performed and no design problems found
- Test of the ASD up to 1 Mrad and checked chip behaviors for current, peak time, pulse shape etc before and after the irradiation
- Also studied ASD performance at GIF++ with 150 GeV muon beam



ASD Drift time: ~ 750ns



Position resolution of a single tube measured by ASD ASIC

Time-Digital-Converter ASIC

❑ TDC Design

- 24 CHs input, 2 CHs outputs (320Mbps)
- 4 key parts
  - ePLL (extended Phase-locked loop)
  - Timing circuit: fine + coarse time (0.78ns bin)
  - TDC logic
    - Trigger-less + Trigger mode
    - New output protocol
    - High speed interface
  - Interface: serial output, configuration, clocks…

No. of channels	24
Least time count	0.78 ns
Dynamic range	17 bits (102.4 μs)
Integral non-linearity	±40 ps
Differential non-linearity	±40 ps
Double hit resolution	<10 ns
Input clock frequency	40 MHz
Max. recommended hit rate	400 kHz per channel
Edge/pair time measurements	Configurable
Output data rate	Configurable: 80 Mbps one line, 160/320 Mbps two lines
Triggerless/trigger modes	Configurable
Triggerless: Latency	<500 ns at 400 kHz per tube
Trigger: Buffer sizes	Hit buffer: 16/channel, channel FIFO: 4/channel, Readout FIFO: 16
Channel enable/disable	Yes
Input/Output signal	SLVS
Radiation tolerance	>20 kRad
Power consumption	<360 mW
Fabrication process	TSMC 130 nm CMOS process

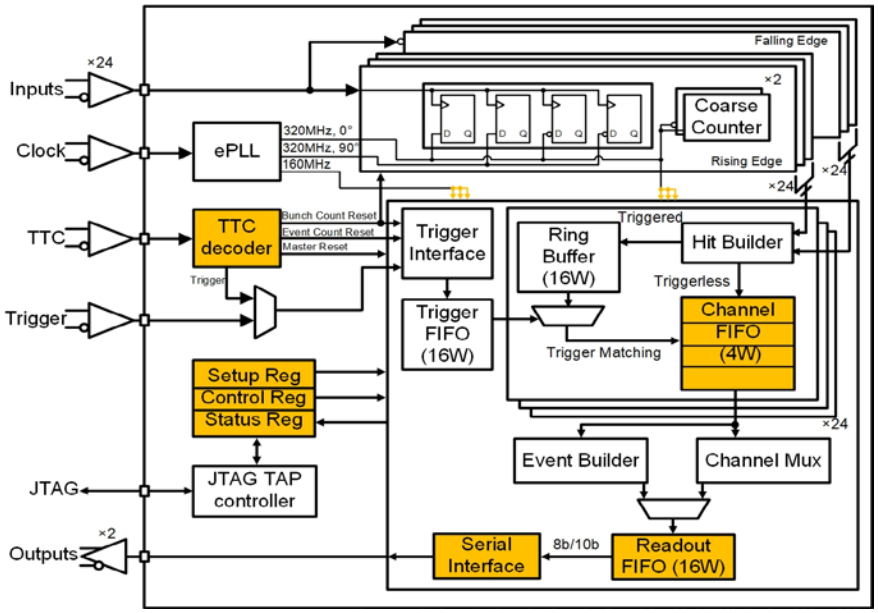
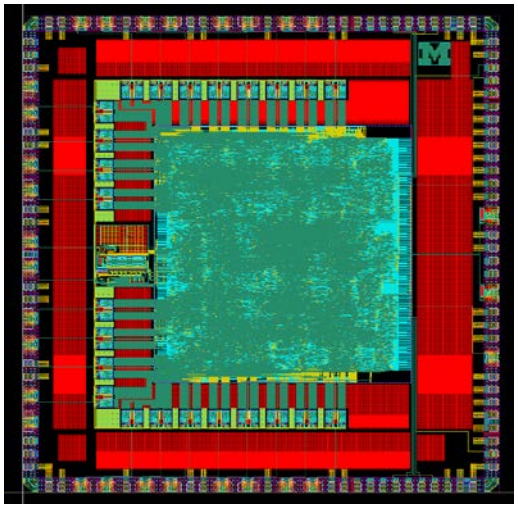


Diagram of TDC V2 with TMR implemented (yellow blocks)

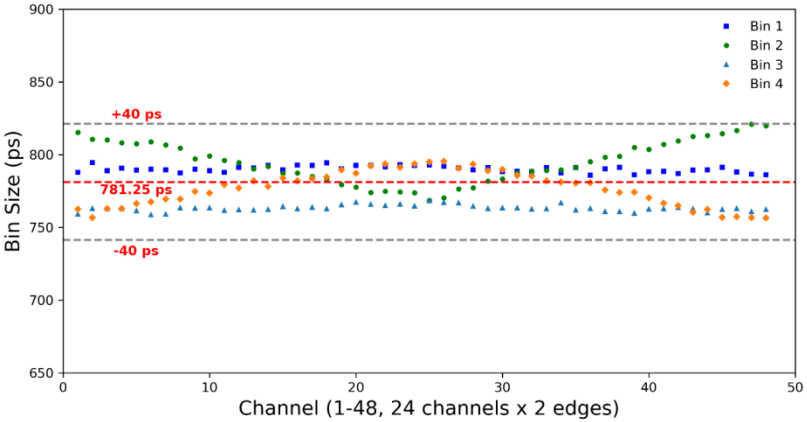


TDC ASIC Layout

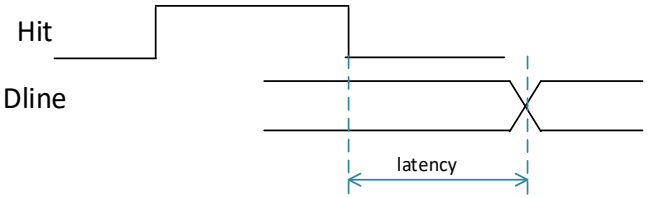
Time-Digital-Converter ASIC

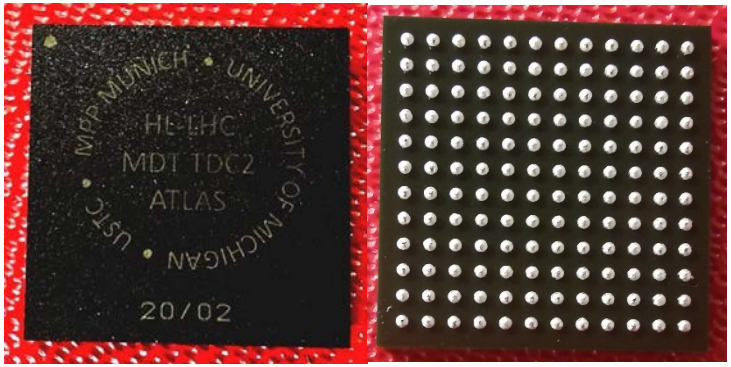
❑ TDC Project Status

- Detailed studies performed and no design problems found
  - o Bin size for all 48 channels have been measured (24 channels × rising and falling edges): variation < ±40ps
  - o Latency: For 400kHz hit rate, 99% of the data was read out after 350ns
- Brief history of TDC development
  - o 2016: V0 designed and tested (GF 130nm)
  - o 2018: V1 submitted and tested (TSMC 130nm)
  - o 2019/2020: V2 submitted and tested
    - Triple Modular Redundancy (TMR) added
    - BGA 12*12 package

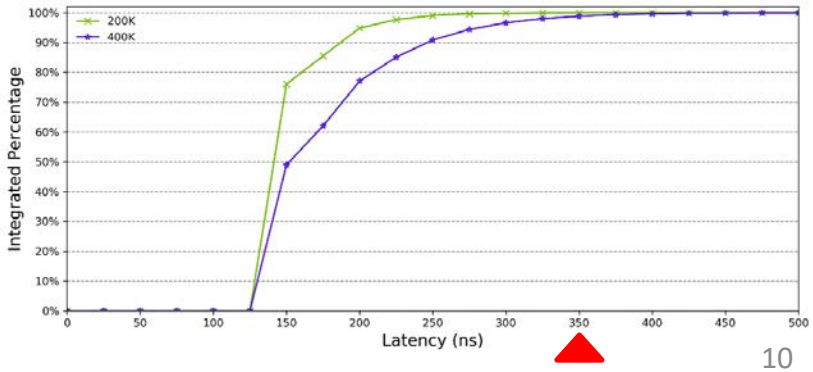


Fine-time bin size of all 48 TDC slices





TDC V2 ASIC chip



Mezzanine Card

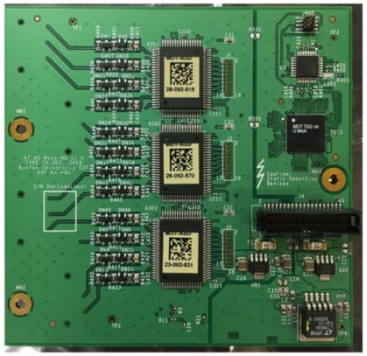
❑ Design

- Compatibility
  - o dimensions and locations of the connectors (Faraday cages, read-out hedgehog cards, and read-out cables)
  - o Pin assignment
- Radiation tolerant
  - o All critical components must be radiaion tolerant
  - o COTS LDO radiation tests have been scheduled

❑ Status

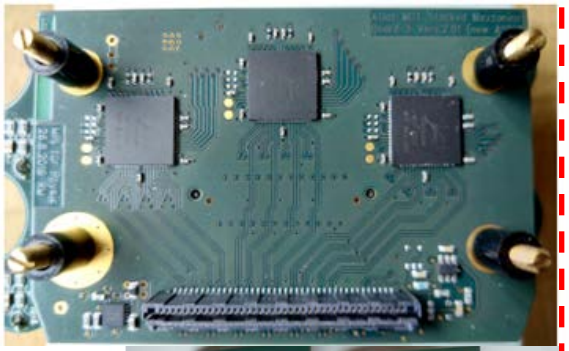
- A few mezz. Prototype cards built:
  - o Multiple ASD+TDC combinations
- Specification review in May. 2019
- Prelimiary design review in Mar. 2020

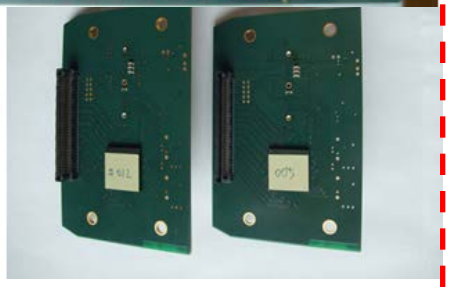
3 new ASDs + 1 FPGA TDC



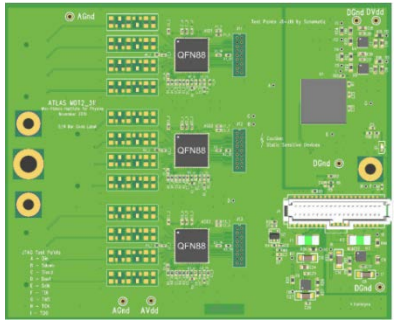
3 legacy ASDs + 1 TDC V0

3 legacy ASDs + 1 HPTDC (stacked for sMDT)





3 new ASDs + 1 new TDC v2 (stacked)

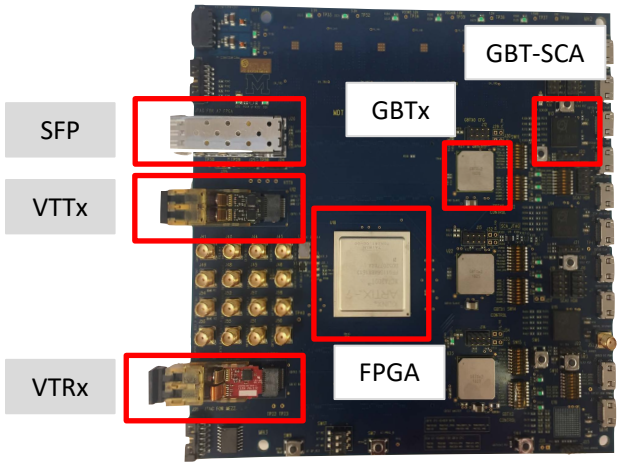


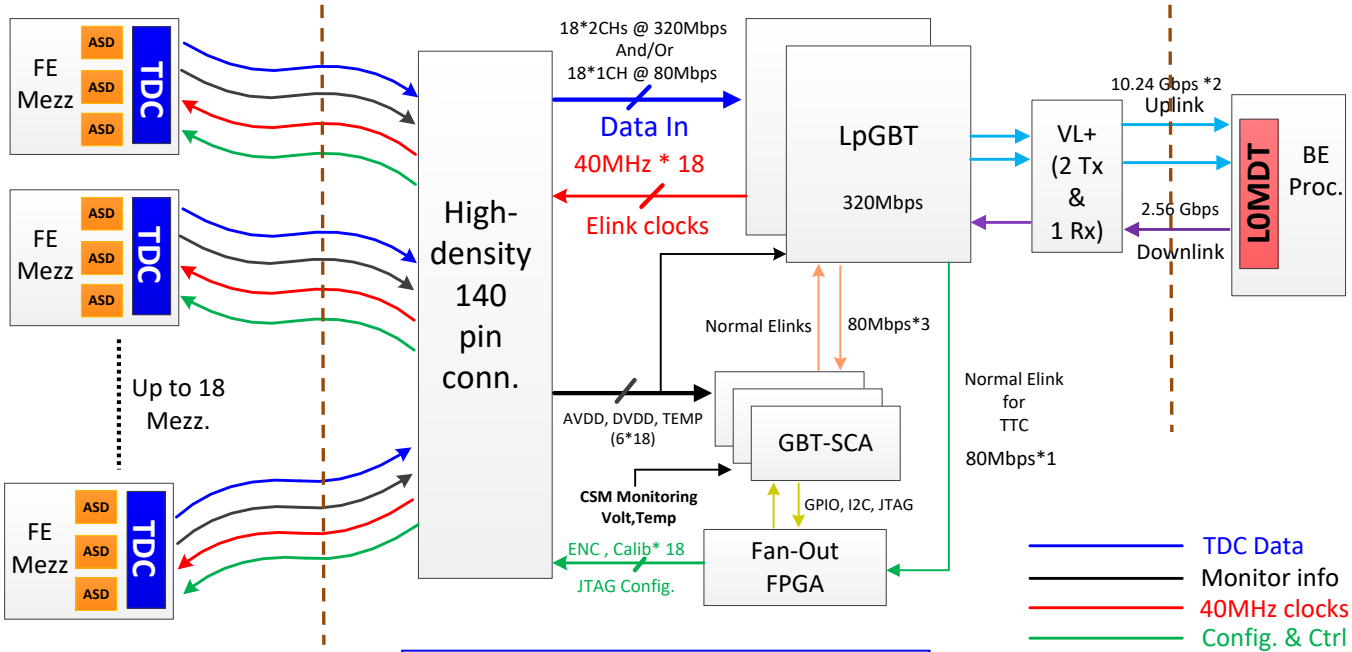
3D CAD model:
3 new ASDs + 1 new TDC V2

Chamber Service Module

❑ CSM Design

- Bandwidth: Input (36CHs * 320Mbps); Output (uplink fiber 2*10.24Gbps, downlink fiber 1* 2.56Gbps)
- 4 key parts
  - o LpGBT *2 (master-slave mode)
  - o GBT-SCA: monitoring & configuration
  - o Fan-out FPGA: receive “TTC” info and broadcast to all 18 Mezz.
  - o VTRx+: optical module





LpGBT-CSM Functionality Block Diagram

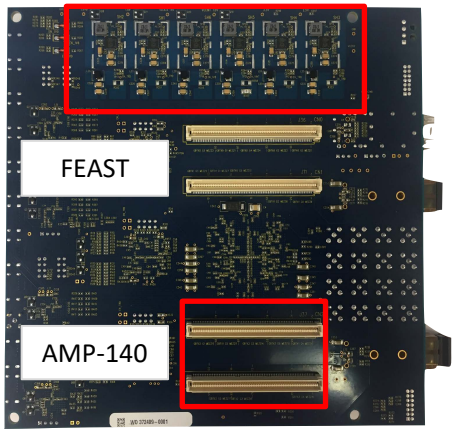
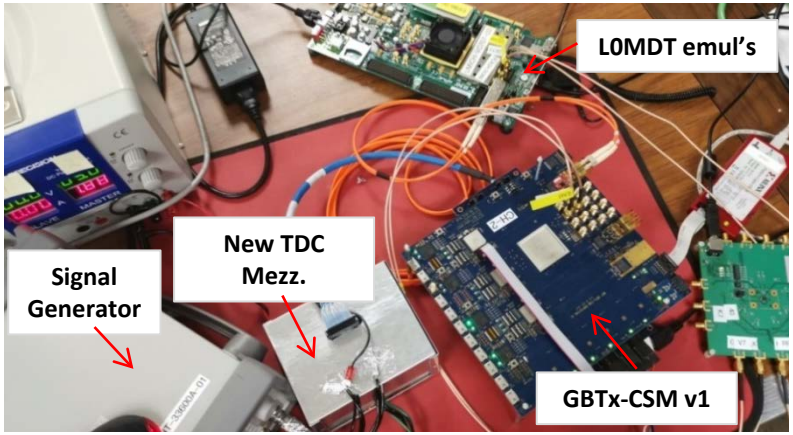


Photo of CSM prototype v1

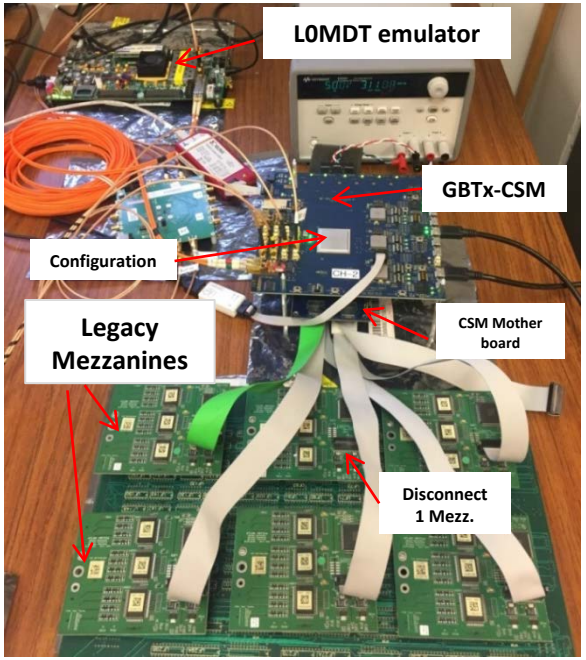
Chamber Service Module

❑ CSM Project Status

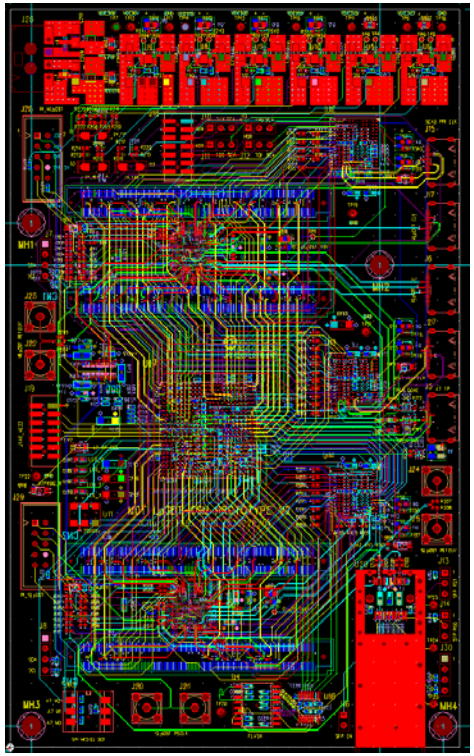
- Prototype v1 (GBTx-based): pass standalone & integration tests
- Specificaiton review in Dec. 2018
- Preliminary deisgn reivew in Mar. 2020
- Prototype v2 submitted in Jul. 2020



Test setup of new TDC Mezz. and CSM prototype v1



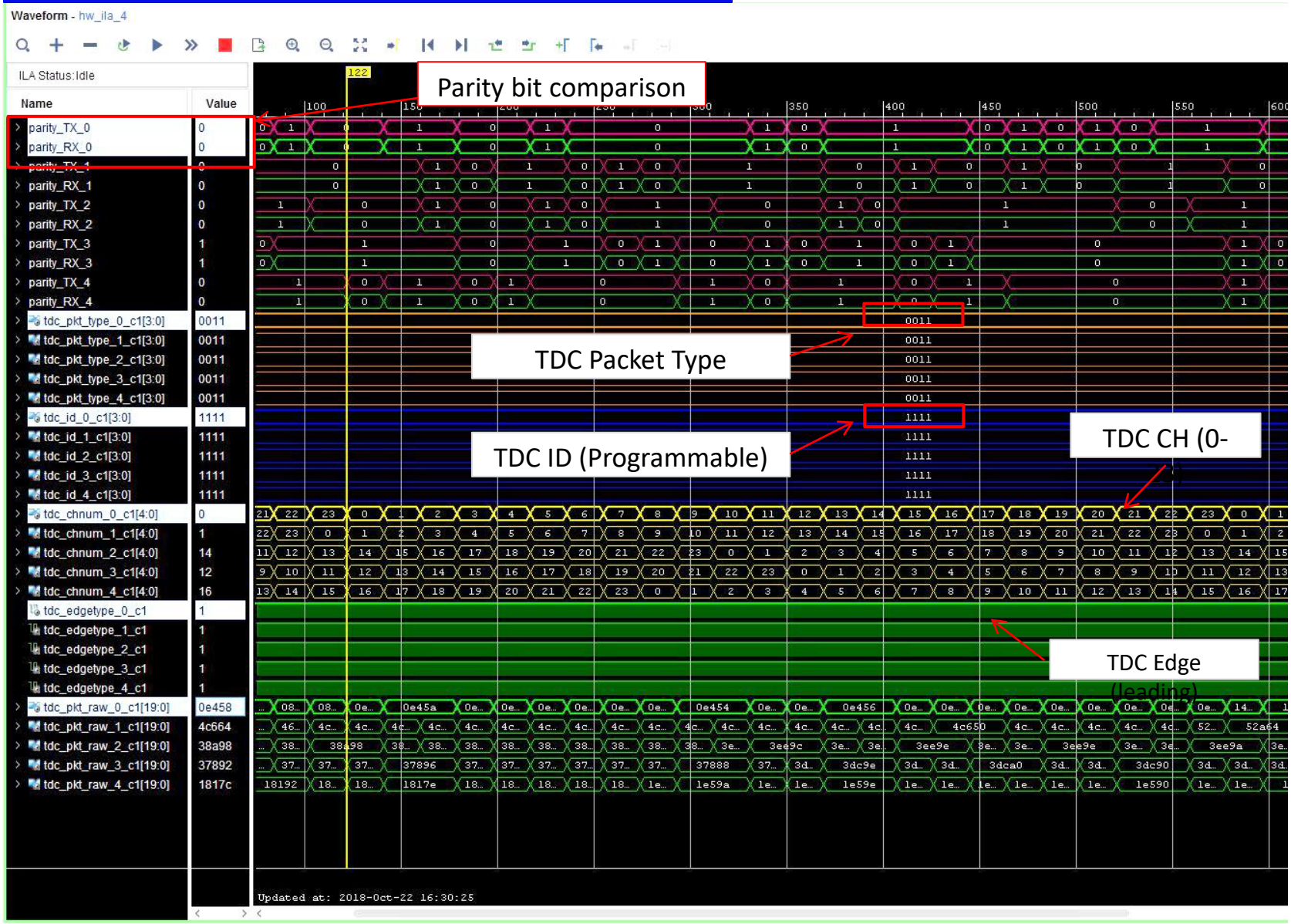
Test setup of legacy Mezz. and CSM prototype v1



LpGBT-CSM v2 layout

Six legacy Mezzanines tested with New CSM v1

- Configuration done properly
- Data decoded successfully



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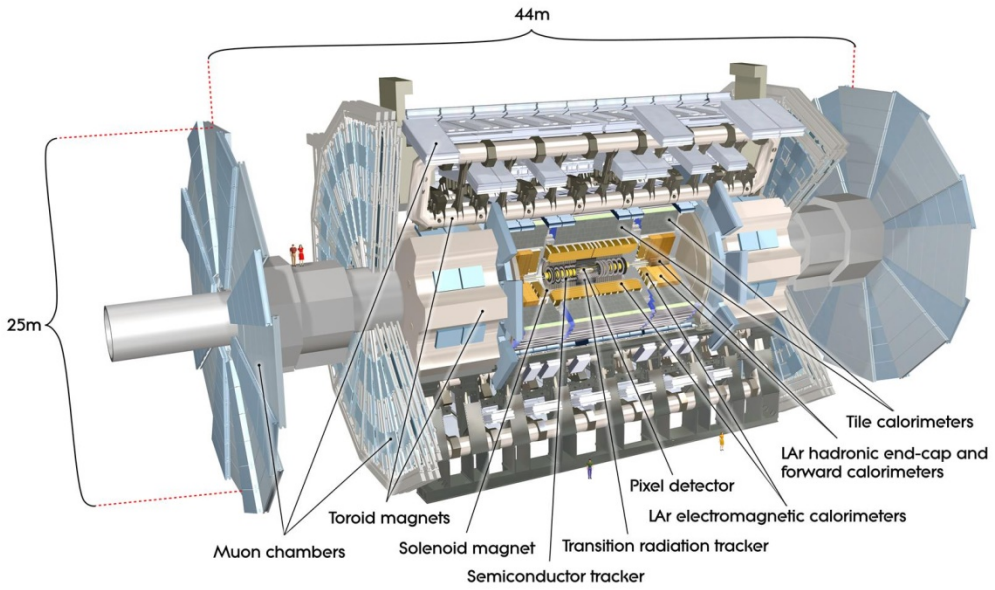
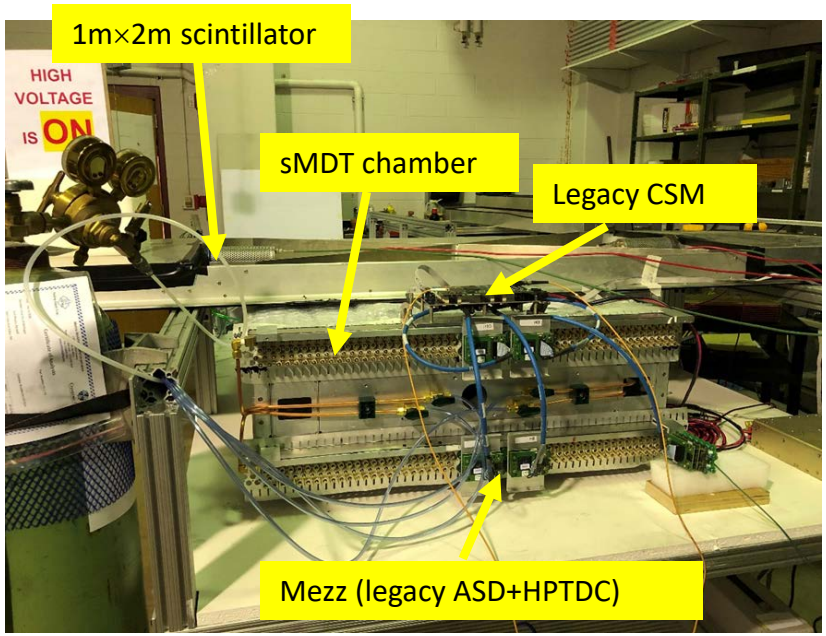
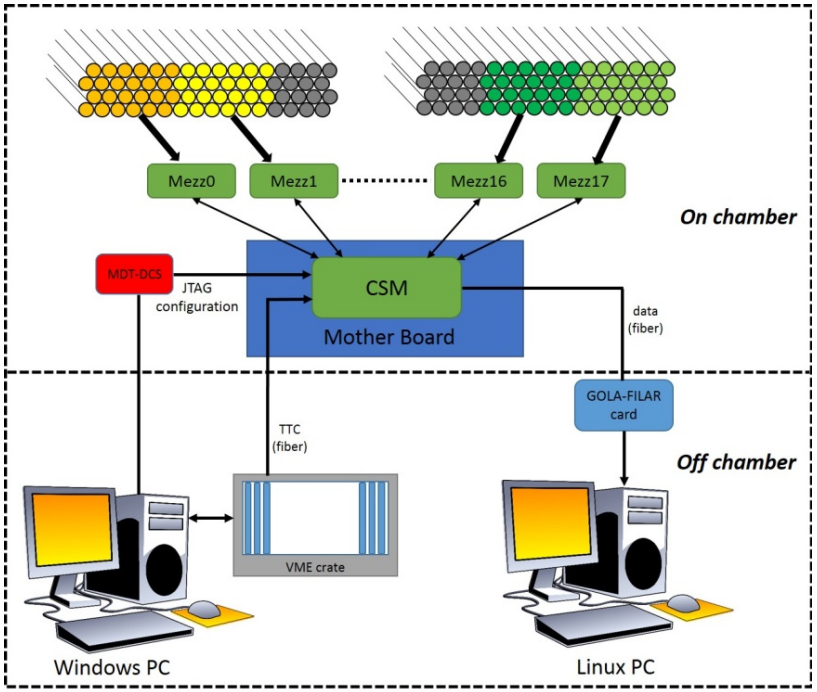
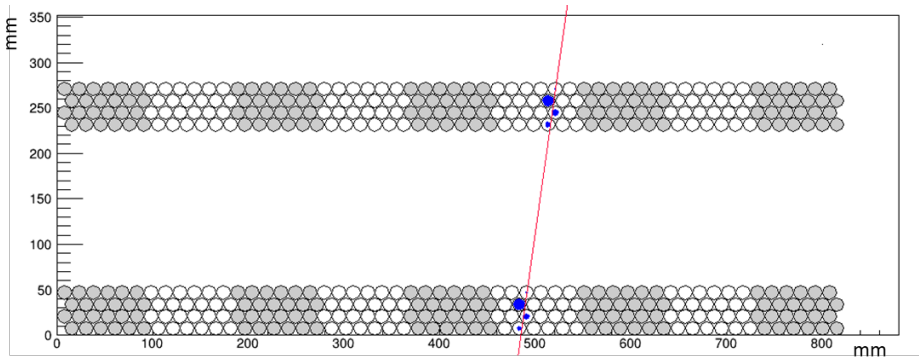


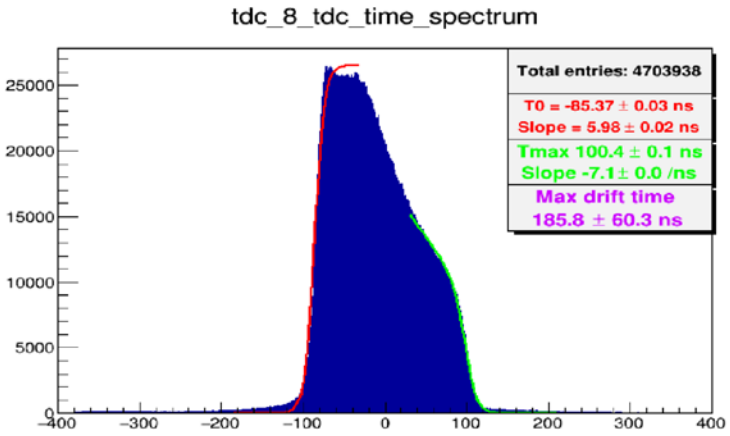
Integration Test Plan

- Current activities -- sMDT cosmic ray test system
  - Legacy electronics used, but will be replaced with new electronics later



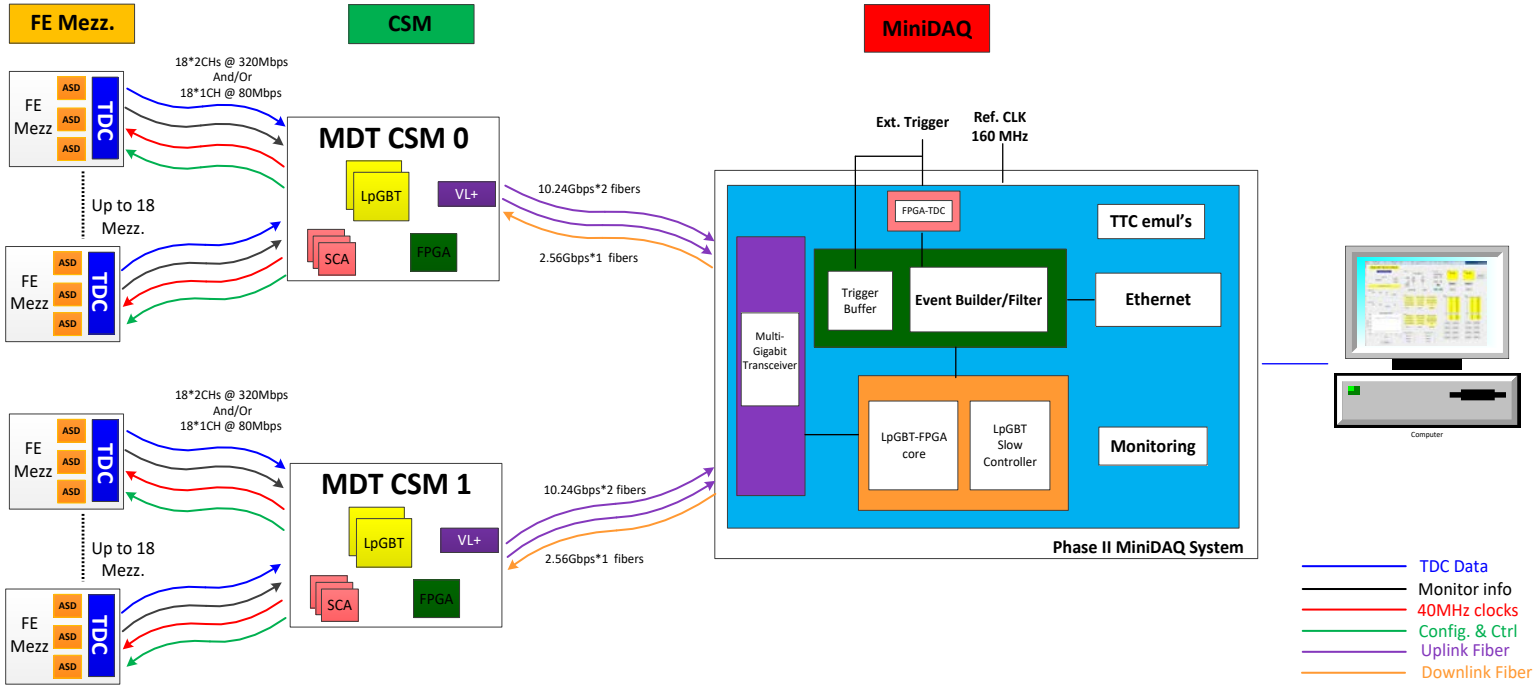






Integration Test Plan

- Goal: integrate different electronics components together and perform studies with/without sMDT/MDT chambers and L0MDT
- Plan to perform integration tests in several steps:
  - ✓ ASD+TDC v1 (QFN package) with and without CSM v1
  - o ASD (QFN88) +TDC v2 (BGA)+CSM v2 with and without chambers
  - o Develop miniDAQ system for integration tests
  - o ASD+TDC v2+CSM v2+L0MDT demonstrator
  - o Final versions of ASD, TDC and CSM with L0MDT v1



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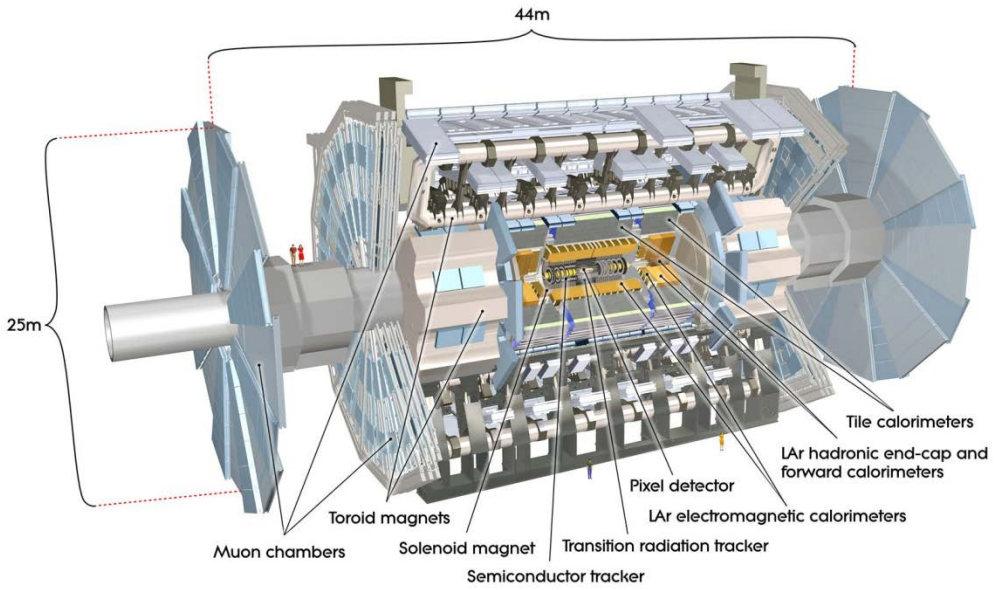


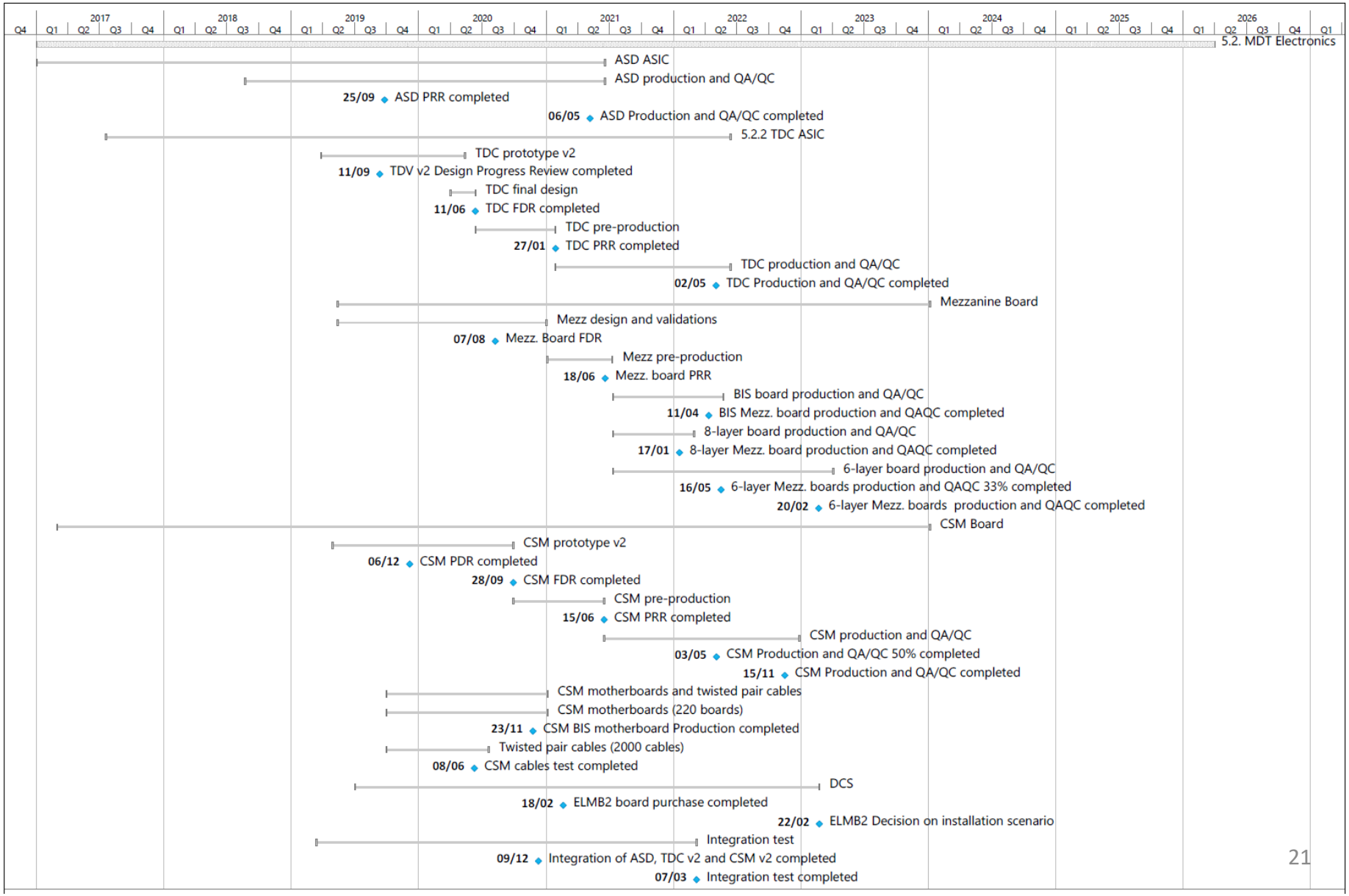
Summary

- To cope with high rates & improve pT momentum resolution, upgrade all MDT electronics system is required
- MDT FE upgrade projects have made lots of progress and passed major reviews (SPR, PDR/FDR)
  - ASD: in production run
  - TDC: close to final designs
  - Mezzanine card prototype & CSM prototype v2: all final features
- Ongoing development on the frontend electronics integration
  - MiniDAQ: sMDT/MDT chambers → Mezz. card → CSM → L0MDT emulator (light version)
- General Schedules
  - ASD production done @ Q3.2021
  - TDC production done @ Q3.2022
  - Mezz. card production done @ Q1. 2024
  - CSM production done @ Q1. 2024

We are on track!

Thanks!

Schedules


2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
Q4 Q1 Q2 Q3 Q4
5.2. MDT Electronics
ASD ASIC
ASD production and QA/QC
25/09 ASD PRR completed
06/05 ASD Production and QA/QC completed
5.2.2 TDC ASIC
TDC prototype v2
11/09 TDV v2 Design Progress Review completed
TDC final design
11/06 TDC FDR completed
TDC pre-production
27/01 TDC PRR completed
TDC production and QA/QC
02/05 TDC Production and QA/QC completed
Mezzanine Board
Mezz design and validations
07/08 Mezz. Board FDR
Mezz pre-production
18/06 Mezz. board PRR
BIS board production and QA/QC
11/04 BIS Mezz. board production and QAQC completed
8-layer board production and QA/QC
17/01 8-layer Mezz. board production and QAQC completed
6-layer board production and QA/QC
16/05 6-layer Mezz. boards production and QAQC 33% completed
20/02 6-layer Mezz. boards production and QAQC completed
CSM Board
CSM prototype v2
06/12 CSM PDR completed
28/09 CSM FDR completed
CSM pre-production
15/06 CSM PRR completed
CSM production and QA/QC
03/05 CSM Production and QA/QC 50% completed
15/11 CSM Production and QA/QC completed
CSM motherboards and twisted pair cables
CSM motherboards (220 boards)
23/11 CSM BIS motherboard Production completed
Twisted pair cables (2000 cables)
08/06 CSM cables test completed
DCS
18/02 ELMB2 board purchase completed
22/02 ELMB2 Decision on installation scenario
Integration test
09/12 Integration of ASD, TDC v2 and CSM v2 completed
07/03 Integration test completed