PROCEEDINGS OF SCIENCE

The lpGBT PLL and CDR Architecture, Performance and SEE Robustness

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We present the design, architecture and experimental results of the low jitter Clock and Data Recovery (CDR) and Phase Locked Loop (PLL) circuit in the Low-Power Gigabit Transceiver (lpGBT) ASIC. This circuit includes a low noise radiation-tolerant integrated LC-oscillator with a nominal frequency of 5.12 GHz to support a 10.24 Gbps uplink and a 2.56 Gbps downlink CDR. This CDR employs a novel loop architecture with a high-speed feed forward loop stabilization technique. A test circuit was fabricated in a 65 nm CMOS technology and has been tested experimentally for correct operation in the foreseen radiation environment.

Topical Workshop on Electronics for Particle Physics TWEPP2019
2-6 September 2019
Santiago de Compostela - Spain

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PoS(TWEPP2019)034

1. Introduction

The lpGBT is a radiation tolerant ASIC that can be used to implement multipurpose high-speed bidirectional links for high-energy physics experiments. The ASIC supports 2.56 Gb/s links in the direction from the counting room to the detectors (downlink) and 5.12 Gb/s or 10.24 Gb/s links in the opposite direction (uplink). Logically, these links provide three distinct data paths for Timing Trigger and Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information. [1]

The lpGBT can operate as a receiver, transmitter or as a transceiver. In the receiver and transceiver modes, its CDR circuit recovers clock and data from a 2.56 Gb/s downlink data stream. In the transmitter configuration, the internal clocks are synchronized to an external reference clock by means of a PLL.

This paper will outline the different operational modes of the circuit, its architecture and the radiation hardening techniques used to improve both Total Ionizing Dose (TID) tolerance and Single Event Effect (SEE) robustness. Test results and measurements obtained during multiple test campaigns will be presented.

2. Circuit Architecture, Radiation Hardening and Operation

As part of the lpGBT, the design specification of the clock generator circuit calls for radiation tolerance up to a TID of 200 Mrad as well as robustness against SEE during operation in the High-Luminosity LHC (HL-LHC) environment. The PLL/CDR circuit is based on the radiation hardened CDR circuit presented in [2]. It was extended by additional circuitry to allow PLL operation and includes a frame aligner compatible with the lpGBT high-speed link specifications [1]. Figure 1 shows a block diagram of the implemented architecture.

Phase Detectors In CDR mode, a classical full-rate Alexander phase detector is used [3]. The frequency acquisition process of the loop is aided by a frequency detector based on a four-quadrant sampling method [4] [5]. The in-phase and quadrature signals required by the frequency detector are derived from a Voltage-Controlled Oscillator (VCO), which oscillates at a frequency of twice the bit rate. In PLL mode, a radiation hardened Phase/Frequency Detector (PFD) is used [6]. The PFD is protected from single-event effects using a Triple Modular Redundancy (TMR) technique. The outputs of three redundant phase detectors are majority-voted in order to mask single event upsets and transients.

Charge Pumps and Loop Filter As seen in Figure 1, the up/down signals of the phase detectors control the respective charge pumps for the proportional and integral loop paths. The loop filter itself consists of a resistor and an integrating capacitor. The two paths of the loop filter are combined and level-shifted, and in turn connect to the tuning node of the VCO. In order to optimize the clock jitter performance in the final application, the charge pump currents as well as the value of the loop filter resistor can be user-programmed, altering the loop transfer function.

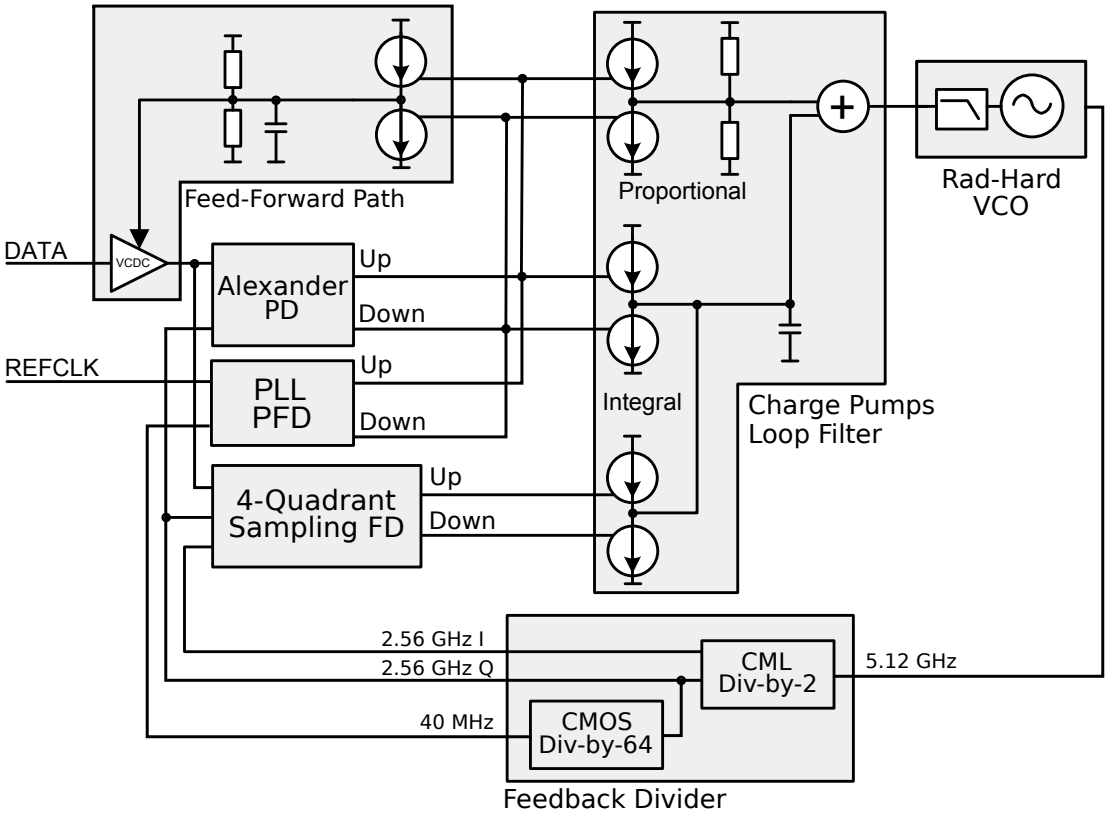

Figure 1: Block diagram of the clock generator architecture used in the lpGBT.

Radiation Hardened LC-VCO The radiation hardened VCO is implemented as an LC oscillator. Previous studies have shown that the traditional associated tuning circuits for LC-VCOs based on deep n-well varactors are susceptible to charge collection in radiation environments and exhibit relatively high SEE cross sections [7]. Our VCO therefore employs a radiation hardened tuning topology previously presented in [7]. This tuning architecture limits the tuning node bandwidth, introducing an additional low-frequency pole into the loop. This pole, if left uncompensated, would result in excessive limit cycle jitter during CDR operation. To compensate for this pole, a feed-forward path is added to the loop. To account for process variation and radiation-induced frequency shift, the LC-tank capacitance can be tuned using a Capacitor DAC (CDAC) circuit as presented in [2].

Feedback Divider The feedback divider is used to divide the 5.12 GHz VCO frequency to either 2.56 GHz (in CDR mode) or to 40 MHz (in PLL mode). It is partitioned into two separate stages. A first divide-by-two stage is implemented using a high-speed Current Mode Logic (CML) topology, while the following divider to 40 MHz is implemented using high-speed CMOS cells. To facilitate phase alignment of the internal clocks to the received data frame during CDR operation, the feedback divider allows skipping individual clock cycles. The phase alignment process ensures that the rising edge of the 40 MHz clock is in phase with the start of the frame. The feedback divider uses TMR for protection against SEE [8] and CMOS cells implemented using Enclosed Layout

Transistors (ELTs) for high frequency operation even after high levels of TID irradiation.

Frame Aligner The frame alignment circuit is required in CDR mode to align the lpGBT clocks and data path to the incoming high-speed data frame. Each frame has a length of 25 ns. After the CDR has locked to the bit clock of the downlink data, the feedback divider clock phase is aligned to the frame header by skipping single clock cycles. This circuit is implemented in standard CMOS with TMR for SEE robustness.

3. Performance Measurements

The circuit was manufactured and tested within the lpGBT. All characterization figures presented here were measured at the output of the lpGBT high-speed serializer, which was configured to output the 5.12 GHz VCO clock.

For characterization of PLL operation, the lpGBT was configured in the transmitter mode and supplied with a 40 MHz low-jitter reference clock provided by a Silicon Labs Si5344 crystal clock generator. Without applying any loop transfer function optimizations, an integrated jitter (100 Hz to 100 MHz) of 1.3 ps was achieved.

For characterization of CDR operation, the lpGBT was configured in transceiver mode and supplied with the required frame format produced by a Xilinx Virtex 7 FPGA. Again, no transfer function optimizations were performed prior to measurement the clock signal characteristics. An integrated jitter performance of 1.6 ps was achieved. In this experimental setup, jitter was dominated by the jitter of the data stream produced by the FPGA transmitter.

4. Radiation Hardness

To validate the radiation hardness of the manufactured circuit, three test campaigns were conducted: the X-ray facility at European Organization for Nuclear Research (CERN) was used to evaluate TID tolerance. The Heavy Ion Facility (HIF) at UC Louvain, Belgium was used for Heavy-Ion tests to estimate the circuit single event effects cross section. Finally, the Two Photon Absorption (TPA) laser facility of the ADVISE Laboratory at KU Leuven, Belgium was used for analysis of SEE sensitivity on a subcircuit level. The X-ray test campaign confirmed correct operation of the circuit up to 415 Mrad without significant degradation of clock signal performance, significantly exceeding the radiation specification of 200 Mrad.

The heavy ion test campaign revealed a minor implementation error inside the frame aligner circuit, which caused longer than expected frame lock times after SEE-induced loss-of-lock events. Another sensitivity was found in the high-speed CML feedback divider. A chain of untriplicated buffers distributing the VCO clock to the divider stages could be upset during a Single Event Effect, which could introduce an additional pulse in the divider. This caused a temporary misalignment of the clock and data phase, which in CDR mode resulted in a short burst of data errors. The errors were reproduced and their origins conclusively confirmed in the TPA campaign. Both these problems identified in the first lpGBT prototypes have been corrected for future revisions used for production runs of the ASIC.

More detailed measurements underlining the radiation hardness of the circuits as well as further results of these radiation test campaigns concerning the core CDR and PLL circuitry can be found in [2].

5. Summary

The architecture and performance of the clock generator circuit, a core component of the lpGBT was presented. Compliance with circuit specifications was demonstrated on manufactured samples. The power consumption of the circuit was measured to be below 34 mW while providing integrated jitter of less than 2 ps rms in PLL and CDR modes. Radiation tolerance of the circuit was tested both with regards to TID and SEE. The circuit was able to operate without significant degradation up to a dose of 415 Mrad. During Heavy-Ion testing, a single event upset cross section of less than $1 \times 10^{-6}\,\mathrm{cm}^2$ was measured, the location of which could be successfully identified. Remediation measures to reduce this cross section have already been incorporated in the design for the lpGBT production run.

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