PROCEEDINGS OF SCIENCE

The lpGBTIA, a 2.5 Gbps Radiation-Tolerant Optical Receiver using InGaAs photodetector

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The Low Power GigaBit Transimpedance Amplifier (lpGBTIA) is the optical receiver amplifier in the lpGBT chipset. It is a highly sensitive transimpedance amplifier designed to operate at 2.56 Gbps. It is implemented in a commercial 65 nm CMOS process. The device has been designed for radiation tolerance and, in particular, to accommodate the radiation effects in photodiodes that manifest themselves as an increase of both their dark current and junction capacitance. The optical receiver consisting of the lpGBTIA connected to an InGaAs photodiode has been successfully tested and irradiation tests showed that the power penalty remains below 4 dBm for exposition to a very high neutron fluences of the order of 10^{15} n/cm².

Topical Workshop on Electronics for Particle Physics (TWEPP2019)
2-6 September 2019
Santiago de Compostela

[1]Speaker

PoS(TWEPP2019)030

1. Introduction

High-energy physics experiments in the LHC require high-speed optical links for transmission of large amounts of data between the experiments and the counting room. In certain detectors or sub-detectors, the radiation levels reach 2 MGy and 10^{15} 1 MeV n_{eq}/cm^2. High-speed optical links and their constituent electronic and optoelectronic devices need thus to sustain such high radiation levels. In this paper, we report on the design of the radiation-tolerant lpGBTIA that is a high-sensitivity optical receiver amplifier operating at 2.56 Gbps. It is implemented in a commercial 65 nm CMOS process, based on a differential structure and designed to accommodate radiation-induced degradation in InGaAs photodiodes.

2. InGaAs Photodiode irradiation test results

Several photodiodes from different materials (GaAs and InGaAs) were irradiated with 20 MeV neutrons [1]. The optical responsivity as function of the particle fluence for the two types of photodiodes is shown in Figure 1-a. These measurements clearly show that from a threshold of 3.10^{14} n/cm², the responsivity deteriorates strongly with fluence and show that the InGaAs devices are more resistant to irradiation than the GaAs devices.

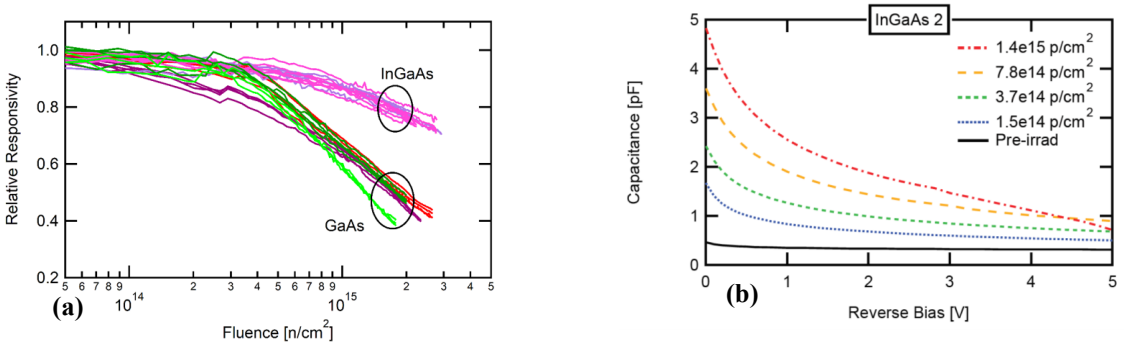

Figure 1: (a) Photodiode responsivity versus neutron fluence for different device (GaAs and InGaAs) (b) InGaAs photodiode capacitance variation with the reverse bias for different proton fluence levels

On the other hand, the measurements from the Figure 1-b show that the pre-irradiation photodiode capacitance is typically less than 500 fF and increases strongly with the particle fluence, particularly for the low reverse bias voltages. This can contribute to the degradation of performance with irradiation for high speed applications. It is therefore important to maintain a high reverse voltage across the photodiode for which the lpGBTIA receiver was designed and optimized to cope with the photodiode capacitance increase.

3. lpGBTIA Receiver architecture

Figure 2 shows the block diagram of the overall lpGBTIA chip where a differential structure is adopted for the entire design. The TIA is designed to achieve a high transimpedance gain (>20 kΩ), high bandwidth (> 2 GHz), and low input referred noise (<2 µA RMS). The limiting amplifier is composed of 4 stages to simultaneously achieve high gain and bandwidth. The output buffer is integrated in the chip to interface with an external 100 Ω differential output load. The offset cancellation circuit controls the DC current in the input stage allowing cancelling the offset DC along the amplifying chain. The photodiode signal is AC coupled to the

TIA using on-chip capacitors and a photodiode biasing circuit is designed and integrated in the chip to ensure the proper biasing of the photodiode for high irradiation levels.

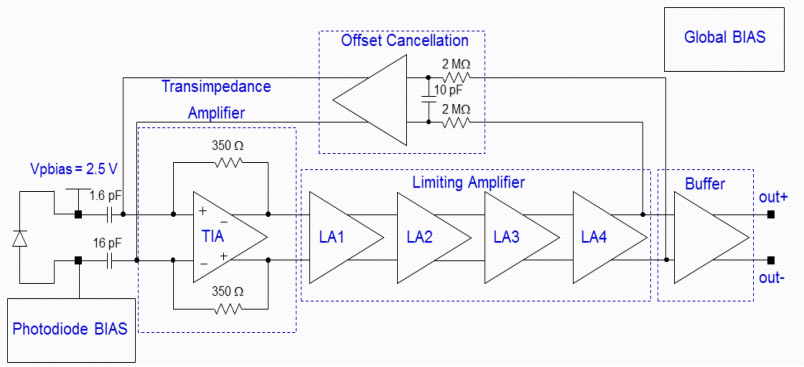

Figure 2: The Block Diagram of the Optical Receiver.

3.1 Transimpedance Amplifier Design

The bandwidth of the TIA connected to the photodiode can be enlarged by decreasing the input capacitance or decreasing the equivalent input resistance of the TIA. The input capacitance is mainly defined by the photodiode capacitance which can exceed 2 pF for high irradiation levels. The input resistance can be decreased by the use of a low feedback resistance values (R21 and R22) or by increasing the loop gain of the amplifier. The use of low feedback resistance results in additional thermal noise, which would degrade the sensitivity of the TIA. In this context, a high gain loop is needed to maintain sufficient bandwidth while keeping a noise level compatible with the requirements of the application.

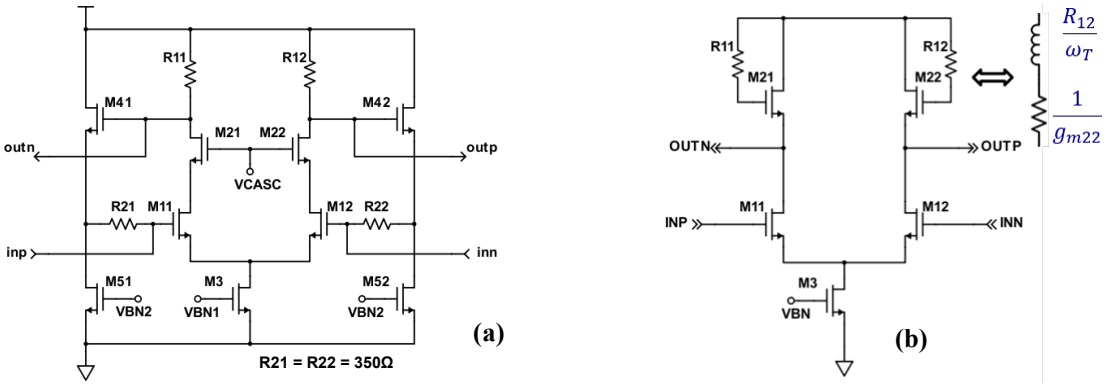

Figure 3: (a) Schematic diagram of the transimpedance amplifier (b) Limiting Amplifier Schematic

When using the 65 nm process, a large amplifier gain can be achieved only by biasing the input transistors of the TIA in the sub-threshold region. In this case, a loop gain of 10 has been achieved for a current bias of 8 mA. The cascode structure avoids Miller effect and enhances the bandwidth which was set to 2 GHz, the minimum required for the bit rate of 2.56 Gbps (≈ 2/3 times the bit rate). The TIA requires a supply voltage of 2 V mainly due to the voltage drop through load resistances (R11 and R12). For reliability, we ensure that the voltage across each transistor never exceeds 1.2V corresponding to the maximum voltage imposed by the process.

4. Limiting Amplifier Design

The limiting amplifier is composed of four gain stages where the bandwidth is further extended by the use of active inductive loads in every gain stage as shown in Figure 3-b [2].

However, the large DC voltage drop across the active inductor requires the increase of the supply voltage to 2 V. The gain of each stage is ~3.4 allowing an overall gain of 130 and the four limiting stages are sized with increasing currents and transistor dimensions. This makes the output buffer capable of delivering 8 mA to the 100 Ω differential load while maintaining a high bandwidth. It is worth mention, that the dissipation of the buffer is representing more than 30 % of the total power consumption.

4.1 InGaAs photodiode bias circuit

Degradation due to irradiation in photodiode can result in large DC leakage current which can be as high as 1 mA [1]. Due to the large impedance of the photodiode bias circuit, this large dark currents reduces the voltage across the photodiode and thus prevent the optical receiver from operating properly. The photodiode bias circuit is shown in Figure 4-a where the NMOS transistor with source degeneration maintains a high impedance despite the high bias current. This large impedance keeps the low-frequency cut-off below 1 MHz which is necessary to avoid closing the eye-diagram at the input of the receiver and to avoid degrading the sensitivity.

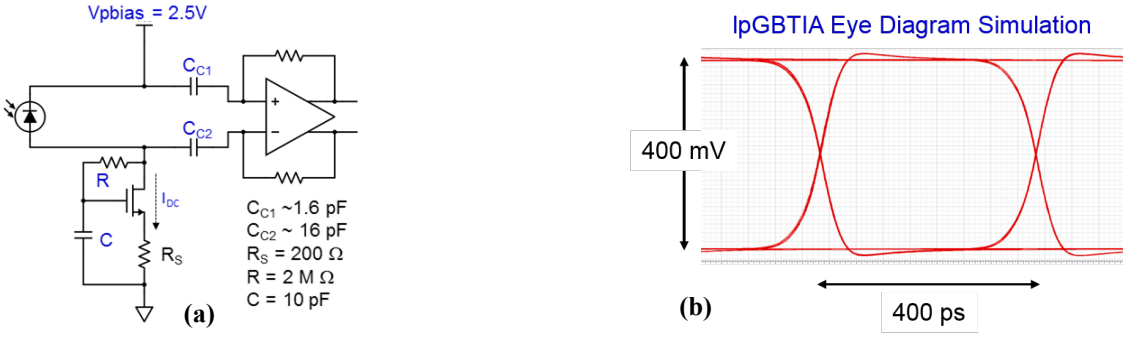

Figure 4: (a) Photodiode bias circuit (b) Simulated eye diagram at 2.5 Gbps

Figure 4-b shows the eye diagram simulation for the whole lpGBTIA for the worst case of biasing (dark current of 1 mA and photodiode reverse voltage of 1.8 V). It is showing a well opened eye diagram with minimal inter-symbol interference jitter. This confirms that the bandwidth remains sufficient despite the increase in the photodetector capacitance.

5. Test results

The lpGBTIA die size is 1750 µm × 461 µm and the pads are arranged to fit in a Versatile TransReceiver (VTRx+) module [3]. The chip was wire bonded to a high speed InGaAs photodiode with a typical responsivity of 0.9 A/W and a parasitic capacitance of 300 fF.

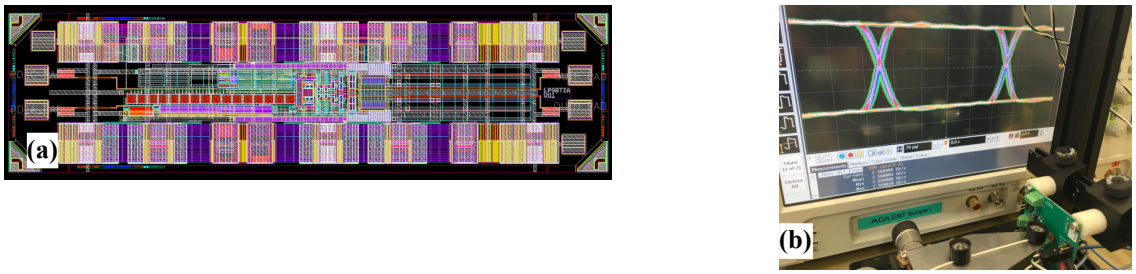

Figure 5: (a) lpGBTIA chip layout (b) Measured differential eye diagrams at 2.5 Gbps for -6 dBm input power

Figure 5-b is showing the eye diagram measured at 2.5 Gbps for a pre-irradiated receiver using a PRBS7 sequence. A clear and well opened eye diagram was obtained for an input power of 6 dBm. The rise time is 30 ps and the total jitter is below 0.15 Unit Interval for a Bit Error Rate of 10^{-12}. This optical receiver powered by 2.5 V is having a total power consumption of 70 mW.

Several receiver samples using photodiodes from different materials (GaAs and InGaAs) were exposed to 20 MeV neutrons beam. Figure 6 shows the radiation penalty as function of neutron fluence for optical receivers based on GaAs and InGaAs photodiodes. This shows clearly that an InGaAs-PIN optical receiver is more resistant to irradiation in terms of sensitivity or responsivity. This validates the lpGBTIA architecture choice that allows to take advantage of the good performance of InGaAs photodiodes while providing a larger power budget for the optical link.

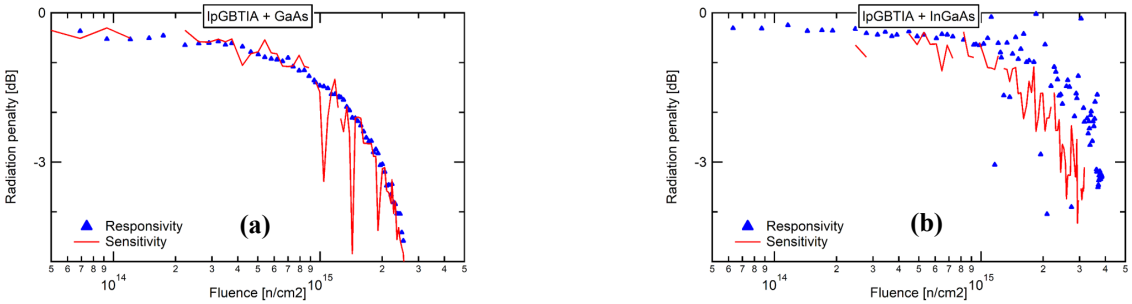

Figure 6: Radiation penalty versus the neutron fluence (a) GaAs (b) InGaAs

6. Conclusion

We showed the methodology followed for the design of the lpGBTIA to meet the different characteristics of the InGaAs photodiodes and particularly the huge increase of their capacitance with the irradiations. Different measurements have shown that the lpGBTIA associated with the InGaAs photodiode maintains very good performances at 2.56 Gbps even after irradiation. In addition to a low degradation of the responsivity inherent to the InGaAs photodiode, the lpGBTIA design allows maintaining a good sensitivity for a very high level of fluence (up to 10^5 n/cm²). The lpGBTIA associated with the InGaAs photodiode is then considered as a good candidate for the optical receiver in high energy physic experiments at the HL-LHC.

The obtained performances are partly due to the photodiode bias circuit that maintains a sufficient reverse voltage across the photodiode despite the effect of radiation. However, this structure of the bias circuit removes the differential feature at the input and this could produce a certain sensitivity to the noise of the power supplies that must be measured and estimated.

References

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[3] J. Troska et al. "The VTRx+ an optical link module for data transmission at HL-LHC" Proc. Sci. vol. 313 pp. 48 Mar. 2018