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Low-power SEE Hardening Techniques and Error Rate Evaluation in 65 nm readout ASICs

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Single event radiation effects represent one of the main challenges for digital designs exposed to ionizing particles in high energy physics detectors. Radiation hardening techniques are based on redundancy, leading to a significant increase in power consumption and area overhead. This contribution will present the single event effects hardening techniques adopted in the pixel and strip readout ASICs of the PS modules for the CMS outer tracker upgrade in relation to power requirements and error rates. Cross section measurements on the silicon prototypes and expected error rates evaluated for the CMS tracker particle flux and spectrum will be presented.

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1. Introduction

Single Event Effects (SEE) represent one of the main concerns for ASICs exposed to ionizing particles in high energy physics applications. Single event hardening techniques are based on redundancy and may introduce significant overhead in power consumption. In applications as the pixel and strip readout ASICs for the CMS outer tracker high luminosity LHC upgrade [1], the readout front-end and the complex digital logic capable of performing on-chip real-time discrimination of particles based on transverse momentum, are required operating with a very tight power budget of less than 100 mW/cm^2. The Macro Pixel ASIC, MPA [2], is a 65 nm CMOS technology pixel readout ASIC featuring on-chip real-time particle discrimination with trigger-less and zero suppressed readout. The Short Strip ASIC, SSA [3], is a strip readout ASIC, designed in the same technology, which provides real-time particle hit coordinates from a strip sensor to the MPA for the particle discrimination. A concentrator ASIC, called CIC [4], aggregates the information from multiple MPA ASICs.

The SEE hardening techniques implemented in the design of the three ASICs need to be evaluated in relation to power requirements and tolerable error rates. It is essential to study how different parts of the design may benefit from different SEE protecting techniques, and eventually, which percentage of power consumption could be traded to reach higher radiation tolerance.

2. Single event effects hardening approach and simulation

To study which technique to implement and eventually which percentage of power consumption and area can be traded to reach higher radiation tolerance, it is essential to evaluate the maximum error rates that can be accepted and, eventually, their consequences. Any upset in the control state machines may lead to the ASIC to operate in an unknown state and ultimately lead to a deadlock situation or system failure. If such a situation occurs, it may require to issue a reset signal to restore the correct operation, with subsequent loss of synchronization of the whole detector for an extended time window. SEEs on the data paths instead can lead to erroneous information about a single strip or pixel, leading eventually to inefficiencies in the reconstruction of a specific event. They do not affect the readout system operation.

A common hardening technique is the Triple Module Redundancy (TMR). Figure 1 shows how this technique has been implemented in the critical part of the design and in the control state machines. All state variables have to be periodically refreshed with their voted state. Thus a feedback loop is required. The triplication was implemented at RTL level and, where possible, automated by the TMRG

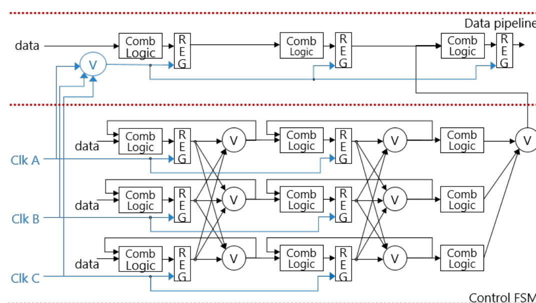

Figure 1: Triple module redundancy strategy implemented in the SSA, MPA and CIC ASICs.

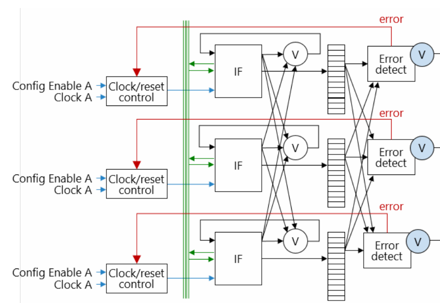

Figure 2: Implementation of the TMR technique with clock gating and self-refresh feedback.

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tool [5]. Clearly, the TMR technique can protect from SEUs only if the physical distance among triplicated registers is sufficient to guarantee that the charge generated by an ionizing particle traversing the substrate can not upset more than one node at the same time. Specific constraints were developed for synthesis and standard cell placement to guarantee a minimum distance. The common approach consists in separating spatially the three instances of the state machine by constraining the placement. This solution may drastically complicate the routing and timing closure. The solution implemented in the SSA and MPA ASICs instead consists of assigning each triplicated registers to an instance-group and constrain the relative placement exclusively within it, allowing to guarantee a minimum distance of 15 μm among equivalent registers without constraining the standard cell placement optimization.

The TMR techniques require an active clock to refresh the state variables. The SSA and the MPA ASICs implements a large number of registers to store calibration, trimming, and configuration according to the module location in the tracker, representing approximately 16% of the power budget. The adopted solution (Fig. 2) consists in introducing an error detection logic for clusters of 32 registers, each capable of triggering an asynchronous pulse to locally refresh the stored value only when an SEU occurs, allowing the usage of the clock gating technique. The cluster's size is evaluated as a compromise between the power overhead during the access operations and the power overhead due to the SEU probability. In case of an SEU, larger clusters would activate the clock for a larger amount of logic. On the other hand, smaller clusters would introduce a significant overhead in terms of control and SEU detection logic. The usage of SEU hardening techniques in the data pipeline is not affordable due to the strict power limitation of 250 mW for the MPA-SSA chip-set. The expected event-error-rate needs to be accurately evaluated. While for the particle p_T discrimination and for the triggerless zero-suppressed readout, the latency is 600 ns, for the triggered transmission of the full raw image, the event is stored in the embedded memories for up to 12.6 μs (CMS Level-1 trigger latency). For this reason it becomes necessary to use custom SRAMs featuring the capability to tolerate a TID up to 200 Mrad and a SEE Linear Energy Transfer (LET) threshold of 15 $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$ [3]. A higher SEE tolerance is achieved with high input capacitance memory cells and by increasing the drive strength of the addressing circuit. The total area occupied by the SRAMs is 0.29 mm^3, approximately seven times the SRAM implemented with minimum size devices.

A system-level simulation framework described in [6] was developed in SystemVerilog/UVM to study and optimize the system architecture and to assist and verify the design of the multiple ASICs composing it. It provides randomized transactions emulating particle detector hits according to the tracker geometry. The environment includes the possibility of randomizing SEE injection in terms of injection path and error probability accordingly, either a uniform distribution for high coverage tests or a time of arrival exponential distribution for error rate studies. It represents an essential tool to validate the efficiency of the SEE hardening strategy on the control state machines and estimate the error rates at the chip-set level. From the power analysis of the ASICs based on realistic signals generated from Monte Carlo physics events, it was possible to estimate the overall increase in power consumption due to the SEE hardening to be between 12% to 15%, achieving an error rate of $< 6.3 \cdot 10^{-11}$ per module per event (Sec. 3). Ensuring no errors due to SEE would have required to almost double the power consumption for introducing TMR and encoding techniques on the data path.

3. Measurements and error rate evaluation on the silicon prototypes

The SEU sensitivity of the circuits was tested by irradiation with heavy ions of various types at the UCL-CRC-HIF cyclotron facility. The test procedure consisted of exposing the ASIC to the maximum achievable event rate and in verifying the output data against the expected data in the

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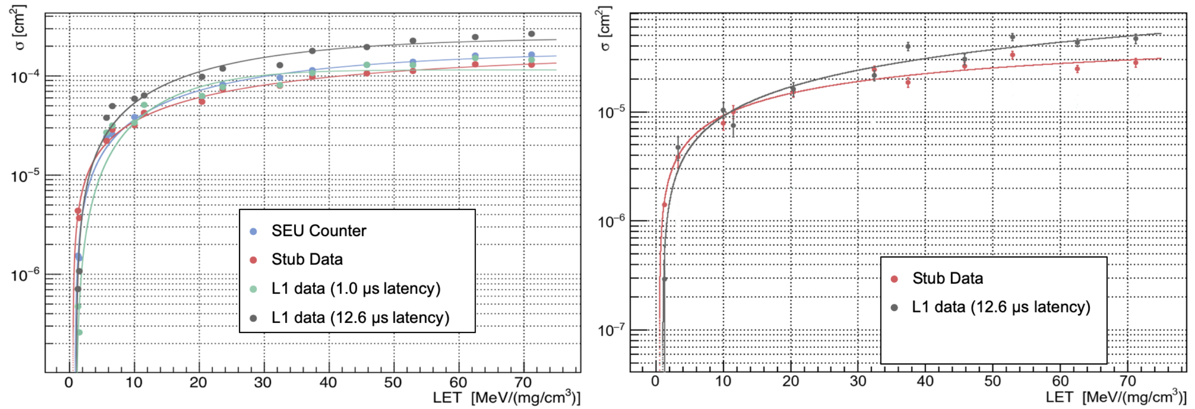

Figure 3: Measured cross section as function of the LET for the MPA (a) and SSA (b) stub-data and L1 raw data transmission path.

FPGA. Furthermore, the static configuration registers were regularly monitored reading out every 30 seconds the values via the serial interface.

As a worst-case scenario, irradiating the ASICs with $^{124}Xe^{35+}$ ions at an energy of 995 MeV, featuring therefore an LET on silicon of 62.5 MeV mg^{-1}cm^{-2}, it was possible to verify that the implemented solution ensuring no losses of control and synchronization among the ASICs. To evaluate the SEU rate, an SEU counter implemented in both ASICs counts the number of corrected upsets. Errors on the transmitted data are expected, and the bit error rate needs to be evaluated according to the operating conditions and the particle flux and spectrum foreseen in the CMS outer tracker region. Based on the computational method described in [7], experimental SEU cross section data as function of the deposited energy can be fit with an integral Weibull distribution $\sigma = \sigma_0 \left(1 - exp\left(-\frac{E_{dep}-E_0}{W}\right)^s\right)$ where E_{dep} is the deposited ionization energy, σ_0 is the saturation value of the SEU cross section, E_0 is the SEU threshold energy for $E_{dep} \mid \sigma(E_{dep}) \to 0$ and W and s are parameters directly dependent on the sensitive volume depth and shape. The measured SEU cross section as a function of the heavy ion LET are presented in Fig. 3.a for the MPA and in Fig. 3.b for the SSA. The measurement error on the cross section values reported in the plot is related to the uncertainty on the fluence value (assumed to be 100 s^{-1}cm^{-2}), the Poisson error on the counts, and the variability of the measurement time (1 s).

The cross section for a specific particle and energy Σ can be approximated as the convolution of the Weibull distribution as a function of the E_{dep} and the energy deposition probability. The same expression can be extended to the case of a radiation environment composed of multiple particle types, based on the assumption that their effects are independent. From the probability distribution of having, within a volume of 1 μm^3, an ionizing deposition per unit of flux greater than E_{dep}, it was possible to evaluate the cross section values for the SSA and the MPA ASICs summarized in Tab. 1. This analysis takes into consideration hadrons with energy higher than 20 MeV in the CMS tracker, for 13 TeV proton-proton collisions.

	SEU Counter	Stub data	L1 data (1 μs)	L1 data (12.6 μs)
MPA	$6.77 \cdot 10^{-11}$ cm^2	$7.92 \cdot 10^{-11}$ cm^2	$5.59 \cdot 10^{-11}$ cm^2	$9.55 \cdot 10^{-11}$ cm^2
SSA	-	$2.74 \cdot 10^{-11}$ cm^2	$0.82 \cdot 10^{-11}$ cm^2	$1.39 \cdot 10^{-11}$ cm^2

Table 1: MPA and SSA SEU cross section values for the CMS outer-tracker particle spectrum for 13 TeV proton-proton collisions.

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	R [cm]	Z [cm]	Er. rate Stub [BX^{-1}]	Er. rate L1 [BX^{-1}]	Er. rate L1 [BX^{-1}]
MPA*	21	265	$3.32 \cdot 10^{-11}$	$2.35 \cdot 10^{-11}$	$4.01 \cdot 10^{-11}$
	60	265	$4.61 \cdot 10^{-12}$	$3.25 \cdot 10^{-12}$	$5.57 \cdot 10^{-12}$
SSA*	21	265	$1.15 \cdot 10^{-11}$	$3.43 \cdot 10^{-12}$	$5.84 \cdot 10^{-12}$
	60	265	$1.60 \cdot 10^{-12}$	$4.73 \cdot 10^{-13}$	$8.09 \cdot 10^{-13}$
Module†	21	265	$< 6.3 \cdot 10^{-11}$	$< 2.49 \cdot 10^{-11}$	$< 6.8 \cdot 10^{-11}$

* Error rates per chip. † Error rates per PS module.

Table 2: PS module expected error rates for the CMS outer-tracker particle spectrum and fluxes.

The SEU upset rates for MPA and SSA can be directly calculated from the cross section measurements and the particle flux evaluated from FLUKA simulations for 13 TeV pp collisions in the volume of interest. The error rate at the PS-module output is given by the combined effect of errors in the SSA, the MPA and the CIC. Under the hypothesis that errors due to SEUs in MPA and in SSA are not correlated, and that the CIC is agnostic about SEUs in the other chips, it is possible to evaluate an upper limit for the expected module error rate. The results are presented in Tab. 2 for PS modules located at $r = 210$ mm and $z = 2650$ mm (flux peak for the innermost outer tracker barrel layers).

4. Conclusions

The proposed solution implemented in the SSA, MPA, and CIC ASICs for the CMS outer tracker upgrade, ensuring no SEE related losses of control and synchronization among ASICs. The data error rate for a module located in the innermost barrel layer and for a 13 TeV pp event is limited to less than $6.3 \cdot 10^{-11}$ errors per module per event. This result was obtained by irradiating the ASICs prototypes with heavy ions. The overall increase in power consumption is estimated to be $< 15\%$.

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