A CANopen based prototype chip for the Detector Control System of the ATLAS ITk Pixel Detector

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The ATLAS collaboration will install a new inner tracker (ITk) during the phase II upgrade. The innermost part will be a pixel detector. A new Detector Control System (DCS) is being developed to provide control and monitoring of the ITk pixel detector. The MoPS is a CANopen based Application Specific Integrated Circuit foreseen to independently monitor a serial power chain. The final chip is required to be radiation hard up to an ionizing dose of 500 Mrad.

This paper focuses on the feasibility of combining low supply voltage custom ASICs found in radiation detection applications and commercial CAN bus equipment. It proposes a CAN physical layer which is operated at 3.6 V and intended to drive a CAN bus of 60 m length at a data rate of 125 kbit/s. In addition voltage regulators with an input voltage of 5 V, output voltages of 3.6 V, 2.4 V and 1.2 V and a load current capability of 200mA have been developed to power the chip via the CAN bus.

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1. Introduction

Serial powering is the baseline option for the ATLAS inner tracker (ITk) pixel detector targeting the phase II HL-LHC upgrade. Serial powering is based around a current supply and multiple serially connected pixel detectors modules[1]. The Detector Control System (DCS) is required to monitor and control the serial power chain. It provides information about the system state with module level granularity. The control and monitor path of the DCS is intended to be independent of the Data Acquisition System (DAQ) and available all the time including times in which the FEs are switched off. This allows for continuous monitoring of the detector status during long shutdowns.

2. Monitoring of Pixel System - MoPS

The MoPS is an ASIC planned to be used in the control and feedback path of the DCS. The integration of over-voltage and overload protection circuitry into the FE chips removes the requirement to bypass a FE-Module. As a consequence, the functionality of the MoPS ASIC is limited to monitoring functions. One MoPS chip is responsible for measuring the supply voltage and the temperature of multiple FE-Modules within a serial chain, as shown in Figure 1. The tempera-
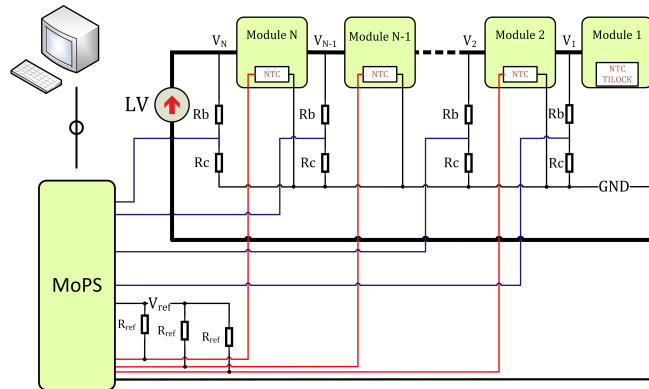

Figure 1: Schematic of the Detector Control System monitoring ASIC (MoPS)

ture of the modules is measured by means of negative temperature coefficient (NTC) thermistors available on each FE-Module. The NTCs are supplied from a reference voltage provided by the MoPS chip through external pull-up resistors. However, the NTC of the last module in every serial power chain is used for the interlock path (separate, safety path) of the DCS and is therefore not connected to the MoPS ASIC. The MoPS features an integrated analog-to-digital converter (ADC) which has a resolution of 12 bit and can convert voltages from up to 40 channels using an analog multiplexer. The MoPS communicates with the DCS main server over a CAN bus defined by standard ISO 11898 using an integrated CAN protocol unit and a physical layer. The core logic of the MoPS chip is the bridge between the CAN bus protocol unit and the ADC. It implements a hardwired version of the CANopen application layer protocol which is used to transfer data to the main server. The MoPS ASIC has identical radiation tolerance requirements as the FE chip and must withstand a total ionizing dose of up to 500 Mrad. It is designed using a commercial 65 nm CMOS technology and utilizes only thin oxide core transistors to limit the effects of radiation.

3. Controller Area Network Physical Layer

A first submitted testchip contained the CAN physical layer specified in the original draft of the MoPS chip. According to this specification it must be able to drive a CAN bus of 60 m length at 125 kbit/s to allow a direct connection between the MoPS ASIC and the DCS server. A challenging design target of this CAN physical layer is the compatibility to standard industrial interfaces, resulting in the requirement for an operation with the voltage levels defined by the CAN standard ISO 11898-2 of up to 4.5 V. However, the maximum applicable voltage for the thin oxide core transistors of the used technology is 1.32 V. Therefore special circuits with several cascoded transistors have to be used to prevent violations of the technology voltage limits at all transistor electrodes while the required input and output voltage ranges specified in the standard are met.

3.1 Transmitter

The transmitter section uses the scheme shown on the right of Figure 2 with three serially connected driving transistors for each of the CAN-L (low) and CAN-H (high) bus lines. To avoid an over-voltage situation in one of the driving transistors, due to an imbalance of the voltage spread across the devices, special biasing circuits are connected to the gates of the cascoded transistors which adjust the bias voltage depending on the CAN bus state the transmitter is connected to. The
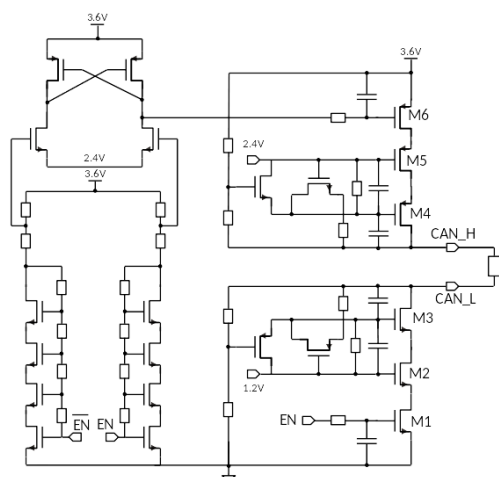

Figure 2: Schematic of the CAN physical layer transmitter
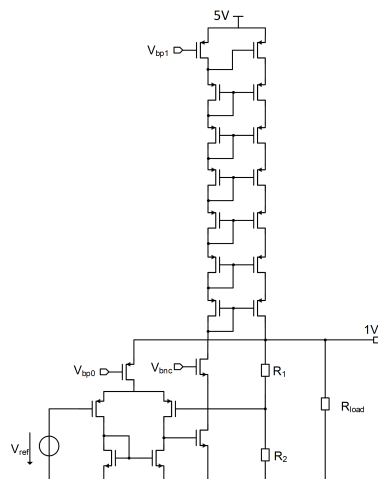

Figure 3: Partial schematic of the 1.2V voltage regulator

physical layer reaches a CAN-H voltage of 3.3 V and a differential voltage of at least 2.5 V using a typical 120/60 Ω termination. The level shifter shown on the left side of Figure 2 is integrated to drive the output stage with the 1.2 V level signals from the digital logic. The transmitter section of the physical layer requires three different supply voltages of 1.2 V, 2.4 V and 3.6 V to operate.

3.2 Receiver

The receiver section of the CAN physical layer translates the differential CAN bus signal into a single-ended digital signal. The input stage of the receiver circuit is a resistive divider which reduces the CAN bus-voltages to voltages below the limit of the core transistors. This allows for a

simpler comparator circuit design since no supply voltages higher than 1.2 V are required for the signal processing. Special care must be taken that at the minimum specified CAN bus differential voltage the comparator hysteresis is smaller than the difference of the divided CAN bus signals.

3.3 Voltage Regulators

The original draft for the MoPS chip specification specified a single 5 V supply. To create the three different supply voltages required by the physical layer a set of voltage regulators were designed. These regulators, similar to the physical layer, are built from core transistors only and need cascoded structures to achieve a sufficient input voltage range. The number of cascoded pass-devices depends on the voltage drop across the output stage, which in turn depends on the specified output voltage. Therefore the 1.2 V regulator, shown in Figure 3, contains seven pass-devices in series while the 2.4 V and 3.6 V regulator which use the same architecture only need five and three, respectively. The differential amplifiers of all three regulators are powered by the output of the 1.2 V regulator. The 1.2 V regulator is the only regulator requiring an additional startup circuit due to the feedback loop from the regulator output to the amplifier supply voltage. The bias voltages V_{bnc}, V_{bp1} and V_{bp0} are generated by multiple cascoded beta multipliers which are supplied by 5 V and 1.2 V respectively.

4. Results from the first Testchip

Initial measurements of the first testchip showed an excessive current flow occurring at input supply voltages above 2.8 V. As can be seen from the measurement for a set of three voltage regulators in Figure 4. The input voltage collapses as soon as it reaches values around 3.1 V. This is caused by the excess current present at high input voltages which triggers the 25 mA current limitation of the voltage source. Further investigations showed that this behavior is caused by the activation of the ESD protection structures at the regulator input which in their current version are not suitable for the required high voltages. Using a Focused Ion Beam (FIB) procedure the
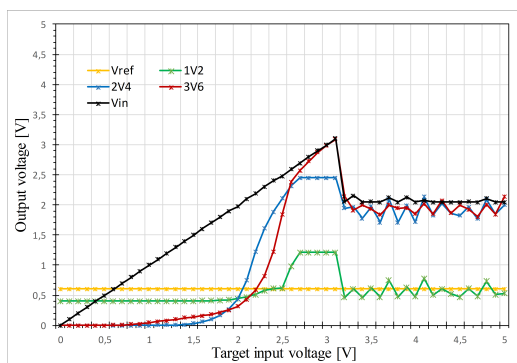

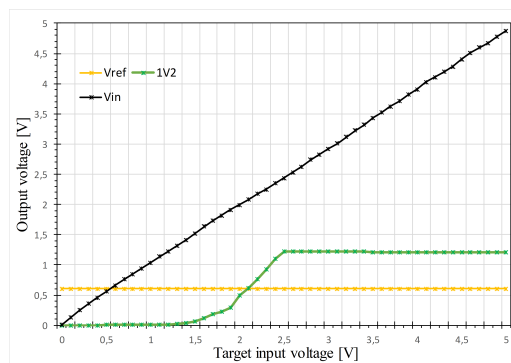**Figure 4:** Unmodified voltage regulator

Figure 5: Modified voltage regulator

ESD protection has been removed for the conduction of additional tests. Figure 5 shows a single modified 1.2 V regulator after the removal of the ESD structures which is working without any excess current flow at input supply voltages of up to 5 V. Unfortunately the complex FIB procedure created unintended shorts on the treated chips prohibiting the simultaneous operation of all three integrated regulators. However since the 1.2 V and 2.4 V regulator can be operated stand-alone

after the modification there is a high probability that the 3.6 V regulator will also work properly as soon as the ESD protection interference is removed. First tests with the CAN physical layer show that it can be operated in combination with commercial interfaces as well as with other instances of the same physical layer. During these tests all required supply voltages were provided from external sources. Figure 6 shows the output signals of the transmitter section, while the behavior of the receiver can be found in Figure 7. The preliminary results indicate that the physical layer
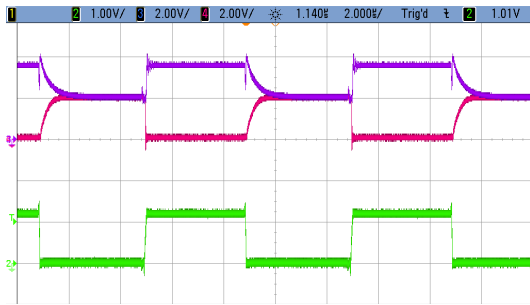

Figure 6: CAN physical layer - Transmitter (violet: CAN-H, red: CAN-L, green: digital input)
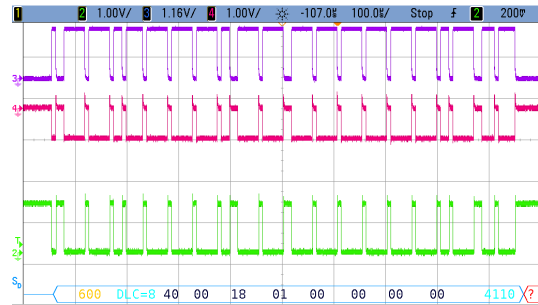
Figure 7: CAN physical layer - Receiver (violet: CAN-H, red: CAN-L, green: digital output)

works with bit rates up to at least 250 kbit/s, exceeding the design target of 125 kbit/s. Similar to the voltage regulators, modifications to the ESD protection of the pads connected to the physical layer had to be made in order to allow bus voltages higher than 2.8 V. The physical layer is not fully verified at this stage and needs to be subjected to radiation campaigns and long term operation test to evaluate the impact of radiation and ageing effects. A chip version without ESD protection has been submitted in August 2019 to conduct further tests.

5. Conclusion and Outlook

A baseline limited to monitoring duties for the control and feedback path of the Detector Control System has been defined. One of the central elements is the MoPS ASIC which is responsible for acquiring voltages and temperatures of the FE-Modules. The first complete version of the MoPS chip is to be submitted in November of 2019.

The preliminary results from the first test chip show that the use of standard CAN voltage levels with thin oxide core transistors is possible if 5 V tolerant ESD structures are available. However due to the limited time available in this project to react to potential problems detected after irradiation, it was decided to continue the development with a more conservative approach using a non-standard compliant 1.2 V low voltage CAN physical layer integrated in the MoPS ASIC as well as in the devices located in the control room. The presented results and planned irradiation studies could still be of benefit to future projects to solve the incompatibility between devices with low supply voltages used in radiation detection applications and commercial buses.

References

[1] ATLAS Collaboration: *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, CERN-LHCC-2017-021. ATLAS-TDR-030, (2017), https://cds.cern.ch/record/2285585