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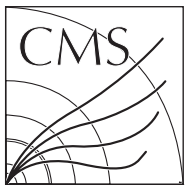

The Compact Muon Solenoid Experiment

Conference Report

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MPA-SSA, design and test of a 65 nm ASIC-based system for particle tracking at HL-LHC featuring on-chip particle discrimination

Davide Ceresa, Gianmario Bergamin, Alessandro Caratelli, Jan Kaplon,
Kostas Kloukinas, Simone Scarfì and Yusuf Leblebici on behalf of the CMS Tracker Group

Abstract

Particle tracking detectors for High Energy Physics need a new readout technique to cope with the increase of the collision rate foreseen for the High Luminosity LHC upgrade. In particular, the selection of interesting physics events at the first trigger stage becomes extremely challenging at high luminosity, not only because of the rate increase, but also because the selection algorithms become inefficient in high pileup conditions. A substantial increase of latency and trigger rate provides an improvement that is not sufficient to preserve the tracking performance of the current system. A possible solution consists of using tracking information for the event selection.

Given a limited bandwidth, the use of tracking information for the event selection implies that the tracker has to send out self-selected information for every event. This is the reason why front-end electronics need to perform a local data reduction. This functionality relies on the capability of continuous particle discrimination on-chip based on the transverse momentum.

The high complexity of the digital logic for particle selection and the very low power requirement of $< 100\,\mathrm{mW/cm^2}$ drive the choice of a 65 nm CMOS technology. The harsh environment, characterized by a high ionizing radiation dose of 100 Mrad and a low temperature of around - 30 °C, requires additional studies and technology characterization. Several architectures for particle tracking have been studied and evaluated with physics events from Monte Carlo simulations. The chosen architecture reaches an efficiency of $> 95\,\%$ in particle selection and a data reduction from $\sim 30\,\mathrm{Gbps/cm^2}$ to $\sim 0.7\,\mathrm{Gbps/cm^2}$

Two full-size and full-functionality prototypes, called MPA and SSA, have been designed, produced and tested. These two readout front-end ASICs perform binary readout of silicon modules which combine pixel and strip sensors, full-event storage with triggered readout, and continuous data selection with trigger-less readout.

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***Abstract*—Particle tracking detectors for High Energy Physics need a new readout technique to cope with the increase of the collision rate foreseen for the High Luminosity LHC upgrade. In particular, the selection of interesting physics events at the first trigger stage becomes extremely challenging at high luminosity, not only because of the rate increase, but also because the selection algorithms become inefficient in high pileup conditions. A substantial increase of latency and trigger rate provides an improvement that is not sufficient to preserve the tracking performance of the current system. A possible solution consists of using tracking information for the event selection.**

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I. Introduction

THE Macro-Pixel ASIC (MPA) is a 65 nm CMOS technology pixel readout chip featuring on-chip real-time particle discrimination with trigger-less and zero suppressed readout. The Short Strip ASIC (SSA) is a strip readout chip, designed in the same technology, which provides real-time particle hit coordinates from a strip sensor to the MPA for the particle discrimination. The trigger-less readout is based on transverse momentum (p_T) particle discrimination and it works in parallel with a triggered and zero suppressed readout with a programmable latency (up to 12.8 µs at 40 MHz event rate), which provides the entire event with a maximum trigger rate of 1 MHz. These designs are dedicated to the hybrid Pixel-Strip (PS) module of the CMS Outer Tracker upgrade for the High Luminosity LHC (HL-LHC) [1].

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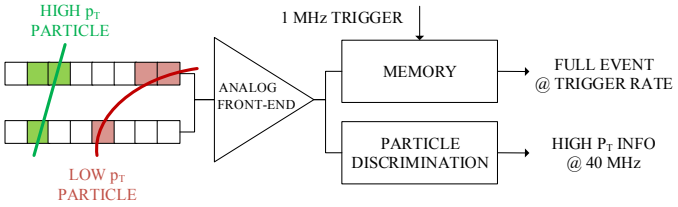

Fig. 1. Simplified view of the front-end electronics for particle discrimination.

II. Design

As shown in Figure 1, a module is composed of two closely spaced silicon sensors in a strong magnetic field providing sufficient sensitivity to measure the particles' transverse momentum over the small sensor separation of a few millimeters. Such a module can be constructed using a pixelated layer and a strip layer sensor. This solution combines the resolution of the pixels with the lower power density of the strips. The pixel matrix, tailored for the CMS Outer Tracker requirements, features macro-pixels of $100 \times 1446\,\mu\mathrm{m}^2$ distributed in 118×16 channels. The strip layer covers the same area with 118 strips of 23 mm length.

The I^2C protocol provides a synchronous, multi-drop, serial communication bus in the CMS Outer Tracker for slow control operation. Therefore, the MPA and SSA chips interface with the back-end through the I^2C bus and exploit a Wishbone bus for internal configuration. An I^2C slave-Wishbone master controls the internal communication through an 8-bit data bus and a 16-bit addressing scheme.

In addition, the chips receive a fast control line operating at 320 MHz in order to encode an 8-bit command per LHC event (40 MHz). A 4-bit unique synchronization sequence provides a recognizable pattern for the alignment of the ASICs, while the remaining 4 bits encode the fast commands using one-hot encoding. The LHC event frequency, also called Bunch Crossing (BX) frequency, represents the internal operation

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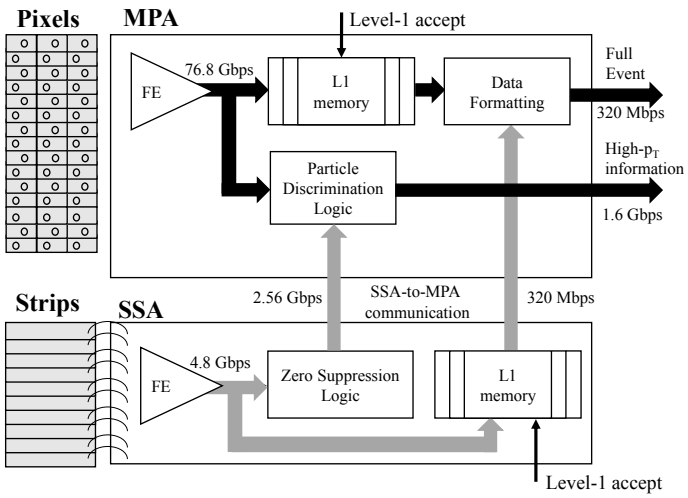

Fig. 2. Block diagram of the MPA and SSA readout architecture.

frequency of the MPA and SSA, while 320 MHz is the system communication frequency.

The maximum hit rate the ASICs will experience in the tracker application is 53 Mhits / s / cm^2. As summarized in Figure 2, the front-end of both ASICs features a binary readout that provides 76.8 Gbps for pixel data and 4.8 Gbps for strip data to the particle discrimination logic. The SSA performs particle cluster reduction with zero-suppression and transmits these strip data to the MPA via 8 parallel differential lines. The aggregated communication bandwidth between MPA and SSA is 2.56 Gbps. The particle discrimination logic in the MPA sorts out high-p_T tracks and transmits in real time p_T information to the experiment off-detector electronics with five parallel differential lines of an aggregated bandwidth of 1.6 Gbps. In parallel the MPA stores full event data in a circular buffer for a period of time which is equal to the response time of the experiment event selection logic. The response time, namely the experiment trigger latency, is 12.8 µs. The selected events are transmitted to the off-detector electronics via a serial link of 320 Mbps. A total bandwidth of 1.92 Gbps is transmitted to the off-detector electronics through a data concentrator ASIC connected to a transceiver ASIC.

To mitigate the effect of radiation related Single Event Effects (SEE), the two ASICs implement a partial Triple Modular Redundancy (TMR) technique. The control logic, including the system clock (but not the sampling clock), and the configuration logic have been triplicated, while a full TMR has been excluded due to the restricted power budget. The maximum Total Ionizing Dose (TID) foreseen in the CMS Outer Tracker is $\sim$50 Mrad (0.5 MGy). A safety factor of two has been considered for this design. As demonstrated in Ref. [3], the degradation induced by high TID in 65 nm MOS transistors is strongly gate-length dependent. For this reason, minimum length transistors are not used in the analog design. On the other hand, the digital design is based on standard cell libraries from the foundry with which the designer cannot size freely the transistor dimension. Based on the results from Ref. [2] and considering the low operating temperature of the tracker, we implemented the digital logic using the 9-tracks standard cell library from the foundry.

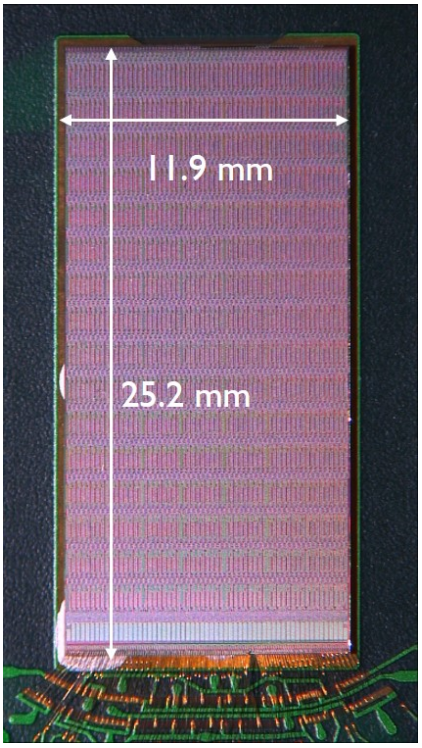

Fig. 3. MPA bare die connected to its test board.

III. Implementation

One of the main challenges for this design is the power consumption. The CMS Outer Tracker application requires a power density < 100 mW / cm^2 for the entire system. Consequently, the ASICs are Multi-Supply Voltage (MSV) designs to strongly limit the digital power consumption without affecting the analog front-end performance. The nominal digital power supply voltage is 1.0 V in order to decrease the power consumption, while the nominal analog and I/O power supply voltages are 1.2 V to avoid performance degradation. The MSV design requires voltage-level shifters for the signals crossing two different domain. To simplify the design, the level shifters are included in the full-custom block (Analog and I/O blocks) and the digital core works only in the digital power domain. In addition, the core logic exploits different threshold voltage standard cells (Multi-V_T design) to locally reduce power consumption or improve performance. Furthermore, memory and clock gating techniques are extensively used in the design.

IV. Results

Test of the MPA and SSA ASICs, shown in Figures 3 and 4, consisted of functional verification of the digital circuitry and performance characterization of the analog front-end circuitry using embedded charge injection capacitor circuits. ASICs with connected sensors were tested using radioactive sources and in test beam experiments.

As extensively reported in Ref. [4], the MPA front-end characterization with internal capacitance pulse injection matched

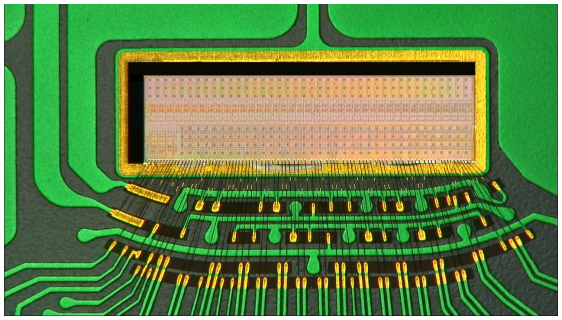

Fig. 4. SSA bare die connected to its test board.

simulations closely, with a pixel-to-pixel threshold spread of 171 e^- r.m.s. after equalization, an Equivalent Noise Charge (ENC) of 188 e^- r.m.s., a peaking time of 24 ns and a time walk < 15 ns. The power consumption is lower than 200 mW per chip and fulfills the very strict CMS Tracker requirements.

The same tests, as reported in Ref. [5], were carried out on the SSA obtaining a strip-to-strip threshold spread of 55 e^- r.m.s. after equalization, a noise without sensor connected of 330 e^- r.m.s. and a peaking time of 19.3 ns.

A special board was developed to test the MPA-SSA high speed communication links. Measurements show a robust communication with a Bit Error Rate (BER) lower than 1×10^{-9} with the lower I/O bias current setting (BER limited by test system, new measurement campaign on-going). During this test, a total consumption of 250 mW for the two ASICs has been measured.

The ASICs' irradiation with X-rays up to 200 Mrad did not show any performance degradation. In addition, a Single Event Upset (SEU) test with Heavy Ions proved SEU tolerance up to an effective Linear Energy Transfer (LET) of $\sim 70\,\mathrm{MeV/(mg/cm^3)}$. Finally, a data error rate evaluation provided a SEU related data error probability lower than 5×10^{-11}.

V. Conclusion

The successful results of the MPA and SSA first full-size and full-functionality prototypes prove the feasibility of on-chip particle discrimination with a power density lower than $100\,\mathrm{mW/cm^2}$ in the harsh environment of the CMS Outer Tracker at the High Luminosity LHC.

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