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Design and characterisation of the CLICTD pixelated monolithic sensor chip

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Abstract

A novel monolithic pixelated sensor and readout chip, the CLIC Tracker Detector (CLICTD) chip, is presented. The CLICTD chip was designed targeting the requirements of the silicon tracker development for the experiment at the Compact Linear Collider (CLIC), and has been fabricated in a modified 180 nm CMOS imaging process with charge collection on a high-resistivity p-type epitaxial layer. The chip features a matrix of 16×128 elongated channels, each measuring 300×30 µm^2. Each channel contains 8 equidistant collection electrodes and analog readout circuits to ensure prompt signal formation. A simultaneous 8-bit Time-of-Arrival (with 10 ns time bins) and 5-bit Time-over-Threshold measurement is performed on the combined digital output of the 8 sub-pixels in every channel. The chip has been fabricated in two process variants and characterised in laboratory measurements using electrical test pulses and radiation sources. Results show a minimum threshold between 135 and 180 e^- and a noise of about 14 e^- RMS. The design aspects and characterisation results of the CLICTD chip are presented.

This work was carried out in the framework of the CLICdp Collaboration

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***Abstract*—A novel monolithic pixelated sensor and readout chip, the CLIC Tracker Detector (CLICTD) chip, is presented. The CLICTD chip was designed targeting the requirements of the silicon tracker development for the experiment at the Compact Linear Collider (CLIC), and has been fabricated in a modified 180 nm CMOS imaging process with charge collection on a high-resistivity p-type epitaxial layer. The chip features a matrix of 16×128 elongated channels, each measuring 300×30 µm^2. Each channel contains 8 equidistant collection electrodes and analog readout circuits to ensure prompt signal formation. A simultaneous 8-bit Time-of-Arrival (with 10 ns time bins) and 5-bit Time-over-Threshold measurement is performed on the combined digital output of the 8 sub-pixels in every channel. The chip has been fabricated in two process variants and characterised in laboratory measurements using electrical test pulses and radiation sources. Results show a minimum threshold between 135 and 180 e$^-$ and a noise of about 14 e$^-$ RMS. The design aspects and characterisation results of the CLICTD chip are presented.**

***Index Terms*—Silicon pixel detectors. Monolithic CMOS sensors.**

I. Introduction

Monolithic CMOS pixel technologies are considered for the tracking detector of the proposed future Compact Linear Collider (CLIC) [1], [2], [3]. The requirements for the CLIC silicon tracker layers are summarized in Table I. For the large active area (137 m^2) silicon tracker in the CLIC detector, this includes a material budget limited to 1 – 1.5% X_0 per detection layer (including sensor electronics, cables, mechanical supports and cooling) and an average power consumption below 150 mW/cm^2. A leak-less liquid cooling scheme is foreseen for the CLIC tracker. The material budget portion corresponding to the silicon sensor layers (including readout electronics) is approximately 200 µm. In order to meet the required power consumption, the detector electronics can be operated in a power pulsed scheme where the main consuming parts of the circuitry are set to a standby power mode between subsequent bunch trains. Given the low duty cycle of the CLIC beam (156 ns long bunch trains repeated every 20 ms), the average power consumption can be significantly reduced by power pulsing and a trigger-less, frame-based readout at a frequency of 50 Hz can be employed. In addition, a ∼ 5 ns hit time resolution is required to suppress beam-induced background particles, along with a measurement of the energy deposited in the sensor to permit time walk correction and cluster position interpolation. A single point resolution of less than 7 µm is required in the transverse direction of the barrel tracking detector, to achieve the required momentum measurement resolution in a magnetic field of 4 T. The granularity in the longitudinal direction, on the other hand, is limited by the occupancy from beam-induced background particles. Detector designs with long pixels or short strips (1 – 10 mm) can therefore be envisaged.

TABLE I: Requirements for the detectors in the CLIC silicon tracker.

Requirement	Value
Single point resolution	<7 µm (transverse plane)
Max. cell size	0.05 – 0.5 mm^2
Time resolution	approx. 5 ns
Hit detection efficiency	> 99.7 – 99.9%
Silicon thickness	≤ 200 µm
Average power consumption	<150 mW/cm^2
Detector area	137 m^2

In this document, the design and characterisation of a pixelated monolithic CMOS integrated circuit, the CLIC Tracker Detector (CLICTD) chip, are presented. The chip features an elongated readout channel geometry with an innovative sub-pixel segmentation scheme, to achieve a high measurement precision while limiting the amount of digital circuitry in the channel [4]. A simultaneous measurement of the time-stamp and the energy deposited in the sensor is performed in each detecting channel (group of eight sub-pixels), while the collection electrodes, analog front-ends and digital processing logic are all integrated in the channel.

Section II describes the process features and the design details of the CLICTD chip. Section III presents the performed characterisation measurements.

II. The CLICTD chip

The CLICTD chip was designed in the framework of the CLIC silicon tracker study and features a sensitive area of

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4.8×3.84 mm^2, with 16 columns by 128 rows of elongated channels, each measuring 300×30 µm^2. In order to minimise the detector capacitance while maintaining a fast signal formation time, the channel is segmented into eight sub-pixels, each with its own collection electrode, analog readout electronics and discriminator. Minimising the detector capacitance is beneficial for achieving a lower power consumption for a given signal-to-noise ratio [5]. The collection electrodes are therefore placed in the long channel dimension on a pitch of 37.5 µm. Based on simulations, the 37.5 µm pitch allows for having the minimum number of collection electrodes in the channel (in order to have an as low as possible detector capacitance) while maintaining a fast charge collection time (of the order of a few ns). Time-stamp and deposited energy information are stored for the combined output of all eight discriminators in the front-ends, as well as the hit pattern of the sub-pixels. In the following sections, a description of the fabrication process and the CLICTD chip design is presented.

A. Chip fabrication process

A modified 180 nm CMOS imaging process, with charge collection on a 30 µm thick highly resistive epitaxial layer, was selected for the design of the CLICTD chip [6]. The epitaxial layer is placed on top of a thicker, low resistivity silicon substrate, resulting in a total silicon thickness of 300 µm. This process offers a small n-type collection electrode (with a diameter of approximately 2 µm) placed on top of the p-type high-resistivity epitaxial layer. The small detector capacitance allows for an important reduction of the analog power consumption and noise of the front-end electronics, compared to a detector of similar performance with larger detector capacitance. Taking advantage of the low noise in the front-end, a low detection threshold can be achieved. All analog and digital on-channel electronics are placed on a deep p-well, which offers an isolation between the electronics and the collection electrode, thus enabling the use of on-channel CMOS digital logic.

In order to fully deplete the epitaxial layer underneath the p-wells, a modification of this process has been developed, including an additional deep n-type implant. To speed up the charge collection for particles impinging between two collection electrodes and reduce the charge sharing within a detection channel, a further modification has been studied [7]. In this case, the deep n-type implant is segmented in the region between neighbouring collection electrodes in order to increase the lateral electric field from the pixel edge to the collection electrode. The increased lateral field reduces the charge collection time, the loss of charges by recombination and the amount of charge sharing between neighbouring electrodes. The cross-sections of the process variants with continuous and segmented deep n-implants are illustrated in Figures 1a and 1b respectively.

To enlarge the depleted region in the sensor volume, two nodes need to be reverse biased: the substrate, which is the physical bulk of the chip (V_{SUB} in Figure 1), and the p-wells where the on-channel electronics are placed (V_{PWELL} in Figure 1). According to simulations and measurements, the

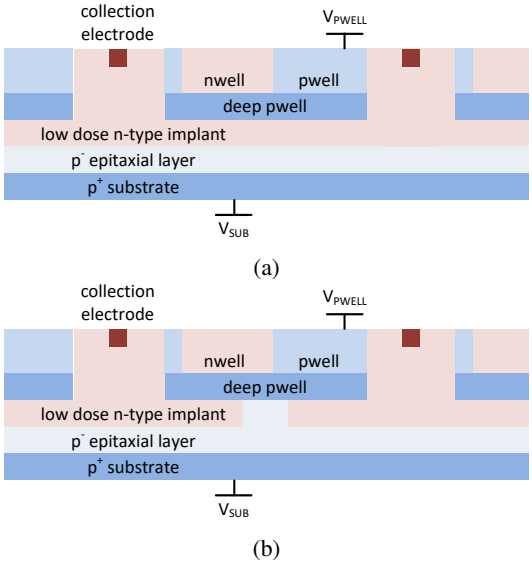


Fig. 1. The two CLICTD process variants: (a) continuous n-implant, and (b) gap in n-implant (not to scale). From [8].

maximum reverse bias that can be applied to the p-wells and the substrate is −6 V, which is sufficient to deplete the epitaxial layer [9]. A TCAD simulation of the electrostatic potential, with the edges of the depleted region marked in black, for a reverse bias of −3 V at the p-wells and substrate is presented in Figure 2a. The same simulation, this time with the p-wells and substrate biased to −6 V is presented in 2b. From the simulations, it is shown that the volume around the collection electrode is further depleted by applying a higher reverse bias, thus minimising the input capacitance [10].

The main contribution to the collected charge comes from the charge carriers that move by drift in the epitaxial layer. An additional diffusion component is collected from the undepleted low resistivity silicon substrate.

The CLICTD chip was fabricated in both process variants. In the case of the segmented n-implant, the segmentation was performed between sub-pixels only in the long channel dimension, in order to achieve a faster charge collection time and reduced charge sharing within a detection channel. No segmentation was performed along the short channel dimension, as charge sharing is desired for improving the spatial resolution in the transverse plane through hit position interpolation.

B. Analog front-end

The CLICTD channel is segmented into eight collection electrodes, resulting in an electrode pitch of 37.5×30 µm^2. The segmentation in the long direction has been chosen in simulation to allow for a prompt charge collection, in view of the required time resolution. A block diagram of the analog front-end is shown on the left side of Figure 3. A level shifter is placed close to the collection electrode in order to keep the input capacitance of the front-end as low as possible. The collection electrode is discharged by using a reset transistor. The voltage pulse at the output of the level shifter is amplified with a voltage amplifier. The amplifier includes a feedback

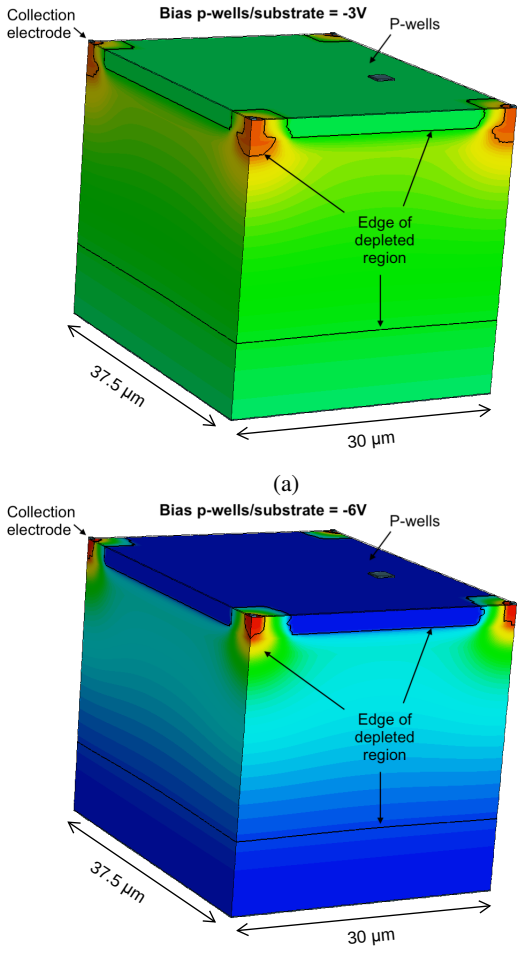


Fig. 2. Simulation of the electrostatic potential for a reverse bias of: (a) −3 V, and (b) −6 V at the p-wells and substrate. The edges of the depleted region are marked in black. TCAD simulation for the process variant with continuous n-implant.

loop with leakage current compensation, similar to the feedback architecture described in [11]. Amplifier parameters such as the DC output (baseline voltage), amplifier rise time and slope for return to the baseline are controllable using biasing DACs that are placed in the analog periphery of the chip. The amplified voltage pulse is connected to a discriminator where it is compared to a programmable threshold voltage that is common to the whole matrix. The signal at the output of the discriminator indicates whether a particle that deposited an energy above the applied threshold was detected, and is processed by the digital logic in order to store Time-of-Arrival and Time-over-Threshold information for the detected particle, as will be explained in Section II-C. To correct for variations in the baseline (and consequently the effective threshold) over the sensitive area, a threshold tuning DAC, implemented as a 3-bit binary weighted current source, is included in each analog sub-pixel. This DAC is connected to the discriminator and can be used to equalise the matrix by tuning the baseline voltage for each sub-pixel such that the threshold dispersion is minimised.

The eight discriminator outputs are connected to the inputs of the on-channel digital logic, where the signals are processed and stored during each acquisition.

Simulations show that the performance of the analog front-end depends on the value of the capacitance of the collection electrode, which is estimated to be between 1.5 and 2.5 fF for the nominal bias of −6 V at the p-wells and substrate. The capacitance value is strongly dependent on the bias voltage since the junction in the modified process is moved away from the collection electrode [10]. For a detector capacitance of 1.5 fF the simulation predicts a gain up to 550 mV/ke$^-$ and a noise of 14 e$^-$ RMS. For a detector capacitance of 2.5 fF, the corresponding simulated values are a gain of 380 mV/ke$^-$ and a noise of 18 e$^-$ RMS. The expected signal rise time at the amplifier output is of the order of 100 ns. The simulated time walk is below 10 ns for a collected charge of 380 e$^-$ or above. A time walk correction can be applied using the energy measurement.

In order to electrically test the CLICTD channel, test-pulses with programmable amplitude, simulating a signal induced by a particle, can be injected to individual sub-pixels. The amplitude of the test-pulse injected to the analog front-end is set by the difference between the $V_{ANALOG1}$ and $V_{ANALOG2}$ voltages in Figure 3, which are controlled by Digital-to-Analog Converters (DACs) in the chip periphery. The option to inject a digital pulse directly to the input of the digital logic in the channel is also foreseen. When a digital test-pulse is injected, all analog front-ends are disconnected from the digital logic in order to decouple the two domains and test the functionality of the digital logic. A masking scheme, where any sub-pixels that malfunction or show higher noise can be excluded from further processing, is also implemented.

C. Digital logic

A block diagram of the circuitry in the CLICTD channel is presented in Figure 3. In the on-channel digital logic, binary hit information is stored for each of the eight sub-pixels. The user can thus identify which, and how many, of the sub-pixels are hit during each acquisition. For the time and deposited energy measurement, all eight discriminator outputs are combined by means of an OR gate. The Time-of-Arrival (ToA) measurement is employed for determining the time of occurrence of the hit. Time bins of 10 ns are expected to be sufficient for achieving the required timing resolution. A 100 MHz clock is distributed along the channel columns, while a global shutter signal, defining the start and stop of the acquisition phase, is used as a time reference. The time-stamp is stored as the number of clock cycles from the moment when the OR of the discriminator outputs is set until the shutter is closed. The ToA counter has a depth of 8 bits, corresponding to a range of 2.54 µs. As the time required for the signal to return to the baseline is proportional to the signal amplitude (and thus to the collected charge), the charge is determined by the time interval for which the discriminator output stays above the global threshold (Time-over-Threshold measurement - ToT). The ToT counter has a depth of 5 bits and a programmable range from 0.6 to 4.8 µs. Asynchronous state machines are implemented in the CLICTD channel digital logic, in order to

minimise the circuit area and the power consumption. In the layout, metal lines are used to shield the analog circuitry from the switching digital lines.

Since the information from the sub-pixels is combined using an OR gate in the CLICTD channel, the time-stamp is stored for the sub-pixel that first detected a hit. The energy information measures the OR of the ToT of all sub-pixels in the channel, in the case of overlapping signals from the sub-pixels. In the case of multiple, discrete hits in the same channel and within the same shutter frame, the sum of the measured time-over-threshold will be accumulated in the ToT counter.

During readout, the digital logic switches to a 40 MHz readout clock, all channels in a column are connected as a long shift register, shifting the acquired data out of the chip serially. The readout clock frequency was selected as it is sufficient for shifting the acquired data out of the CLICTD matrix in a reasonable time (of the order of 1 ms). An optional compression algorithm is implemented to reduce the amount of data that are transmitted. The compression is based on a "hit flag" bit that is set to "high" once the channel detects a hit. For channels that detected a hit, all 22 bits of data (including hit flag, ToA, ToT and binary hit information for the eight sub-pixels) are shifted out of the channel. In the case when the channel did not detect a hit, only the hit flag bit is shifted out. The following 21 bits are skipped and the readout proceeds to the next channel. For the low expected occupancies in the CLIC tracker (of about 1% for the CLICTD channel size), this compression algorithm is expected to reduce the readout time by approximately a factor of 15.

D. Periphery electronics and interface

In the analog periphery of the chip, 20 biasing DACs are included in order to bias the different front-end nodes. For testing and debugging purposes, the option to monitor or overwrite the output of each of the DACs is included. One of the DAC outputs can be monitored or overwritten at a time. In addition, the analog periphery comprises a bandgap circuit that internally generates a voltage reference for the chip.

In the digital periphery, a slow control interface based on a standard I^2C slave is implemented [12]. Through the slow control, the user can read and write all internal registers to control the biasing DACs, to configure the matrix, as well as to send test-pulses, power pulsing and readout commands. Along with the data output, a clock output and a signal indicating the start and end of the transmitted frame are sent during readout to facilitate the synchronisation with the data acquisition system to sample the data.

E. Chip integration and verification

The CLICTD chip was integrated using the digital-on-top approach. During the digital-on-top integration, the digital descriptions of all analog and digital building blocks are used to create a digital netlist that describes the connectivity among all instances. This approach allows for high-level digital simulations and verification of the design.

As a final step, the chip design was verified using the Universal Verification Methodology (UVM) [13]. During the verification stage, the post-layout chip netlist (including delays due to routing lines and parasitic capacitances) was simulated in different corners (power supply, temperature and process variations). Extensive digital verification was proven essential for the CLICTD design, as several issues, including logic mistakes and timing violations, were detected and fixed before production. Two malfunctions of the digital logic were observed in the measurements of the prototype chips. The first was an issue in the configuration state machine and the second in the way the data are read out when the compression algorithm is enabled. Workarounds with negligible impact on the chip performance have been implemented for both issues.

A user's manual with a detailed description of the commands and operation of the CLICTD chip was compiled and made available online [14].

III. Measurement results

First samples of the CLICTD chip were glued and wire-bonded on a custom designed PCB and tested using the Caribou DAQ system [15]. A photo of a CLICTD sample, wire-bonded on the PCB, is presented in Figure 4. First measurement results were presented in [16].

A. Electrical characteristics

Studying the I-V characteristics of the sensor, and in particular the leakage current at the p-wells and substrate, confirmed the differences between the two process variants, as expected from simulations. For the process variant with continuous n-type implant, the substrate can be biased to higher (in absolute value) voltages than the p-wells without significant increase in the leakage current. After the substrate voltage exceeds the p-wells voltage by about 10 V in absolute value, the current increases due to punch-through between the p-wells and substrate. On the other hand, for the process variant with the gap in the n-type implant, a similar bias voltage should be applied to the two nodes such that the current is not dominated by the punch-through current flowing between the p-wells and substrate. These differences are illustrated in Figures 5a and 5b for the process variant with continuous n-type implant and with gap in the n-type implant, respectively. For this measurement, the p-well bias was set to values from $-1\,\mathrm{V}$ to $-6\,\mathrm{V}$ and the substrate bias was scanned. The leakage current plotted in Figure 5 was measured at the p-wells. For both process variants, the collection electrode is biased to about $0.8\,\mathrm{V}$. The measurements were performed in room temperature. The saturation for higher absolute values of the reverse bias voltage in Figures 5a is an effect of the current limit applied for this measurement. The reverse bias that can be applied at the p-wells is constrained to $-6\,\mathrm{V}$, to ensure reliable operation of the transistors in the sensitive area [9]. As the epitaxial layer is expected to be fully depleted at a bias of $-6\,\mathrm{V}$, both at the substrate and the p-wells, this was considered as the target operation point for the sensor. In contrast to the standard planar sensors, a higher negative reverse bias does not necessarily lead to a better performance, due to the complex field in the sensor [7]. As conclusion, although the sensor shows different I-V characteristics for the two process variants,

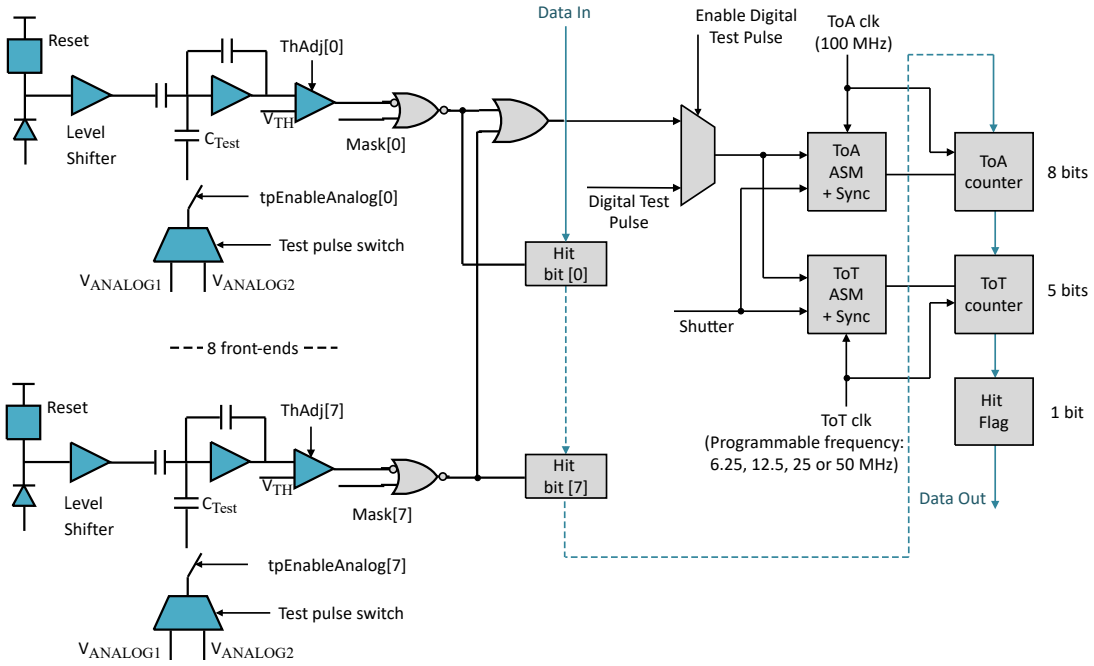


Fig. 3. Block diagram of the analog front-end (in blue) and digital logic (in grey) in the CLICTD detector channel.

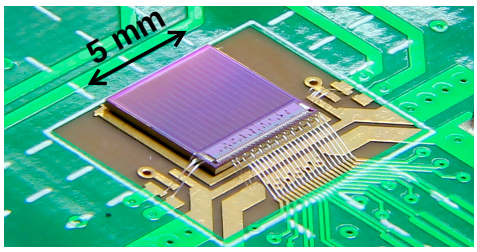
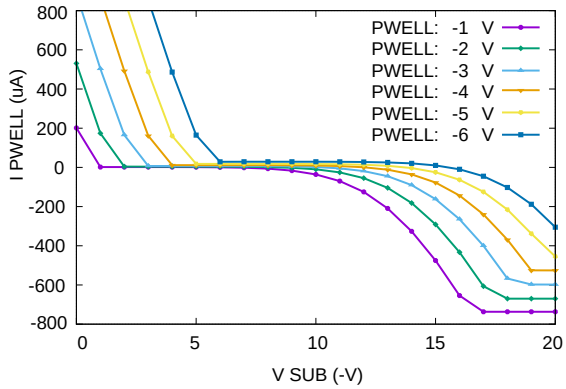


Fig. 4. Photo of a CLICTD sample, glued and wire-bonded on a PCB. Image credit: CLICdp.

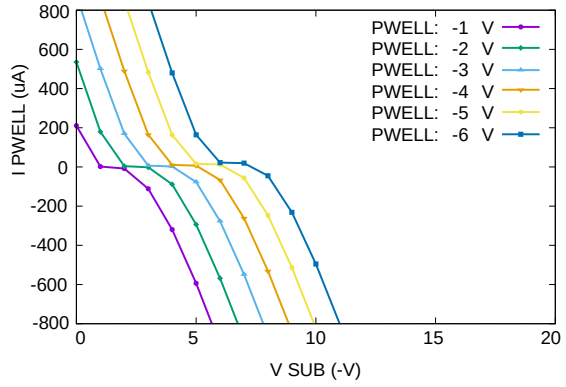
it can be operated in both cases as long as the structure is properly biased. In order to have a straightforward comparison of the two process variants, for the majority of the performed measurements the substrate was kept at the same bias as the p-wells for both process variants.

B. Optimisation of operation parameters

Due to the fact that the on-channel NMOS devices are laid out on the reverse-biased p-well, the transistors are expected to slow down when a higher negative bias is applied. Since the negative bias at the p-wells is not a standard feature of the fabrication process, the effects of the applied reverse bias on the NMOS devices are not well-modelled in simulations. In order to correct for this effect, the operating point of several nodes of the circuit (e.g. the feedback loop in the analog front-end) had to be tuned after biasing the sensor to the nominal −6 V at the p-wells and substrate. Thereby, the NMOS transistors were set back to the desired operation point and the circuit could be operated successfully.



(a)



(b)

Fig. 5. Leakage current measured at the p-wells in the CLICTD matrix as a function of the substrate bias, for different values of the p-well bias. CLICTD sample with (a) continuous n-implant, and (b) gap in n-implant [8].

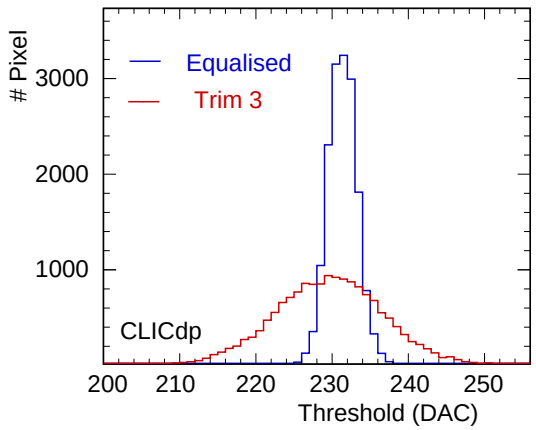


Fig. 6. Baseline dispersion over the CLICTD matrix, before (red curve) and after (blue curve) equalisation. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V.

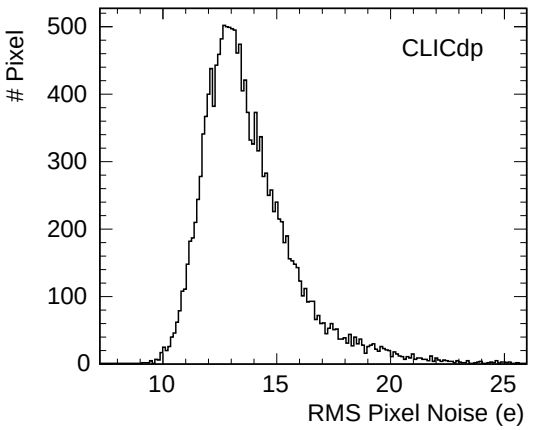


Fig. 7. Histogram of noise RMS per sub-pixel, extracted from threshold scans and measured in electrons. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V.

C. Threshold equalisation

A threshold equalisation algorithm was applied employing the 3-bit threshold tuning DAC in every sub-pixel. Threshold scans were performed for each of the eight codes of this DAC, while the number of detected hits for each applied threshold value was measured for each sub-pixel. The baseline was then extracted on a sub-pixel basis for every DAC code as the mean value of the curve resulting from the number of noise hits that were counted during the threshold scan. A target baseline was selected as the average of the mean values of the resulting baseline distributions for every DAC code. The matrix was then equalised by choosing the DAC code per sub-pixel such that its baseline is closest to the target.

Figure 6 presents the measured baseline for all sub-pixels, before and after equalisation, for a CLICTD sample from the process variant with continuous n-layer, with the p-wells and substrate biased to −6 V. After applying the threshold equalisation algorithm, the threshold dispersion over the CLICTD matrix, estimated as the RMS of the baseline distribution, ranges from 33 to 39 e^- RMS, for the three different CLICTD samples that have been measured and calibrated. Before threshold equalisation, the threshold dispersion is of the order of 100 e^- RMS. The conversion from DAC codes to electrons was done using the calibration presented in Section III-F.

D. Noise

The noise per sub-pixel was calculated as the RMS value of the distribution of the measured noise hits in threshold scans. The mean value for the noise per sub-pixel was extracted to be approximately 14 e^- RMS, for three measured assemblies from both process variants, with the p-wells and substrate biased to −6 V. A histogram of the extracted noise RMS values for all sub-pixels is presented in Figure 7. Figure 8 presents a two dimensional map of the measured noise RMS in electrons over the CLICTD matrix.

A regular pattern can be observed in Figure 8, showing a dependence of the noise on the position of the tested sub-pixel. This pattern results from the regular structure of the layout in the CLICTD matrix. Although the layout of the analog front-end is identical for the eight sub-pixels, the shared digital logic is distributed along the channel. Due to this layout feature, differences in parasitic capacitances or sources of noise coupling can be expected, resulting in the observed pattern that repeats every eight sub-pixel columns in the horizontal direction. The tail in the right-hand side of the noise distribution in Figure 7 results from the columns with higher noise that can be observed in Figure 8. The higher noise in these sub-pixel columns is possibly a result of coupling with noise sources in the digital logic via parasitic capacitances. In the vertical direction, a similar pattern can be observed. The digital logic in one every eight rows includes additional buffers for distributing the clock and shutter signals from the periphery (which is located at the bottom of the matrix) to the top of the matrix. This results in a slightly modified layout for the digital logic in these rows and this structure is also observed in the noise plots.

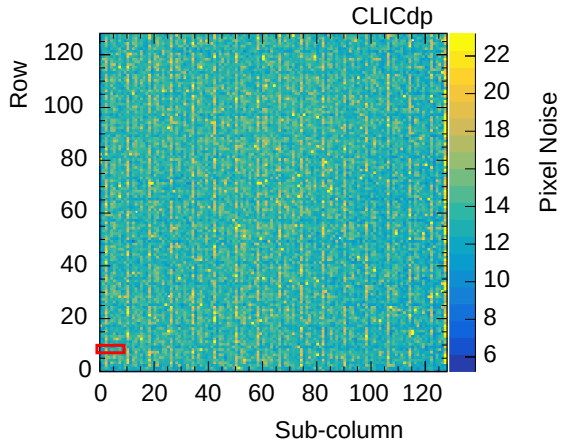


Fig. 8. Two dimensional map of the noise RMS per sub-pixel over the CLICTD matrix, extracted from threshold scans and measured in electrons. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V. The position of one elongated channel in the matrix is marked in red.

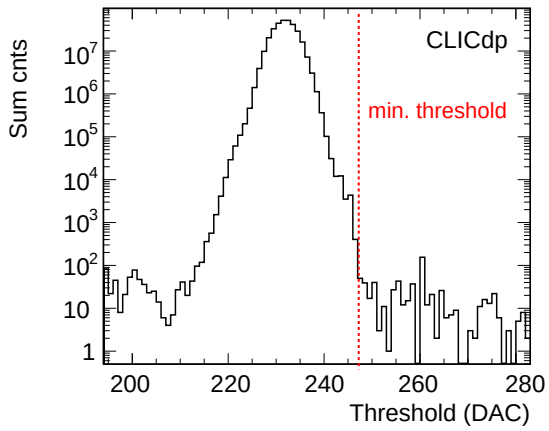


Fig. 9. Number of noise hits detected within a 1 ms shutter as a function of the threshold DAC code. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V. The vertical line indicates the minimum operation threshold for this sample.

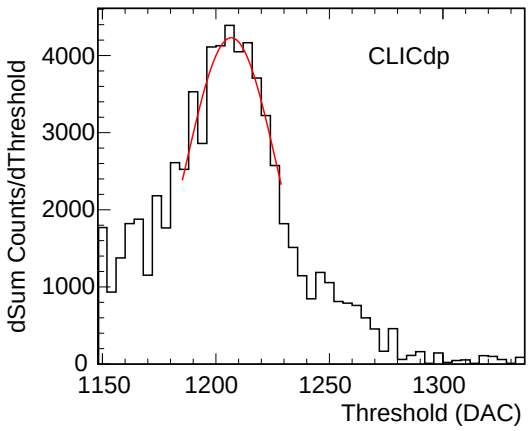


Fig. 10. Fluorescence spectrum and Gaussian fit to the K_α peak, resulting from a measurement with a titanium target. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V.

E. Optimisation of operation threshold

In order to identify the minimum operation threshold, the threshold was set to the lowest value that still ensures a noise-free operation. Figure 9 presents the measured number of noise hits acquired within a 1 ms shutter as a function of the applied threshold DAC code. Sub-pixels that showed a non-Gaussian noise performance, and were detecting noise hits even at higher threshold values, were masked (thus excluded from further processing) in order to achieve a lower operation threshold. After equalisation, the minimum operation threshold of the measured CLICTD samples, is between 135 and 180 e^- with an uncertainty of ±3 e^-, as extracted from the calibration measurements presented in Section III-F. At this threshold, the CLICTD matrix detects no noise hits. For the CLICTD sample used for this measurement, only 0.03% of the sub-pixels were masked.

F. Calibration with radiation sources

In order to obtain physical units for the CLICTD performance parameters, samples were exposed to photons with known energies, using an x-ray machine and the fluorescence spectra of different targets. The K_α peak of the fluorescence spectrum of iron is at 6.4 keV and, with a known mean electron-hole pair creation energy in silicon of 3.62 eV, the charge corresponding to the most probable value of the energy deposited in the sensor is 1.77 ke^-. For the copper target, the equivalent value is 2.22 ke^-, for an x-ray energy of 8.04 keV. Apart from the iron and copper targets, other materials such as calcium and titanium were used to verify the gain linearity of the CLICTD chip, as well as its ability to detect low energy photons.

The calibration was performed by scanning the threshold voltage in the equalised CLICTD chip and counting the number of x-rays detected for each voltage. By this scan, an occupancy curve showing the number of detected x-rays per threshold voltage is produced. The fluorescence spectrum is obtained by the derivative of this occupancy curve and the threshold voltage corresponding the K_α peak is determined as the mean of a Gaussian function fitted to the spectrum. An example spectrum obtained measuring the fluorescence of a titanium target is presented in Figure 10. The Gaussian distribution fitted to the observed K_α peak is plotted in red.

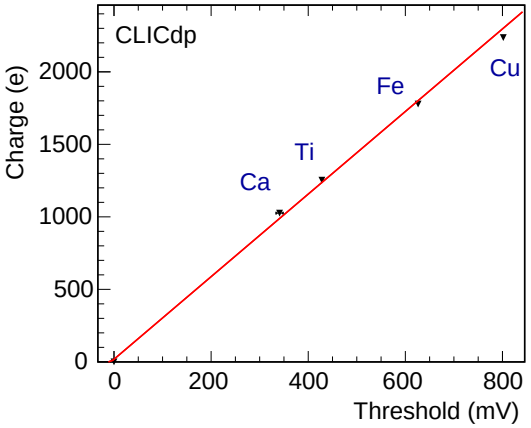


Fig. 11. Gain calibration of the CLICTD amplifier response, extracted from fits of the K_α peaks of the x-ray fluorescence spectra from different target materials. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V. The error bars show the error on the mean of a Gaussian fit to the K_α peaks.

Figure 11 shows the voltage amplitude at the output of the amplifier which corresponds to the K_α peak of the fluorescent x-rays for each material, for a CLICTD sample with continuous n-type implant and with the substrate and p-wells biased at −6 V. The error bars correspond to the fit error of a Gaussian to the K_α peaks. The amplifier gain is determined by the slope of the linear fit, which in this case is approximately 350 mV/ke^-. Comparing this value to the simulated performance presented in Section II-B gives an indication for the input capacitance of the detector.

In addition, the conversion from threshold DAC steps to electrons, used for the results presented in Section III-C, was extracted from the x-ray calibration measurements. For a reverse bias of −6 V at the p-wells and the substrate, one LSB of the threshold DAC corresponds to a step of ~ 9 e^- (from 8.6

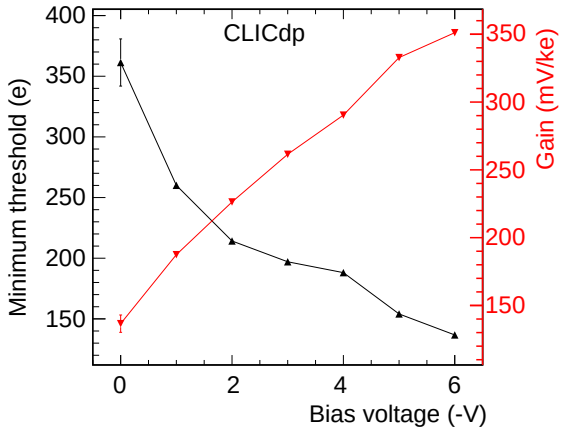


Fig. 12. Amplifier gain, measured with x-ray calibration with different targets, as a function of the reverse bias applied to the p-wells and substrate. The error bars show the error on the mean of a Gaussian fit to the K_α peaks.

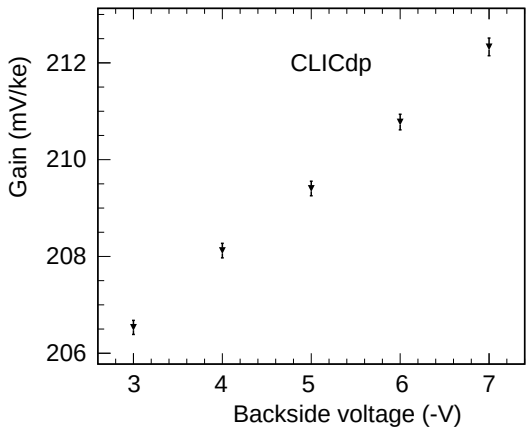


Fig. 13. Amplifier gain, measured with x-ray calibration with an iron target, as a function of the reverse bias applied to substrate, for a fixed bias value of −3 V at the p-wells. Sample with continuous n-type implant. The error bars show the error on the mean of a Gaussian fit to the K_α peaks.

to 9.0 e^- for the three measured assemblies). The fluorescence spectra from the various targets were measured for different values of the reverse bias voltages applied to the sensor, in order to study the effect of the bias voltage on the sensor and the performance of the front-end. Figure 12 presents the measured amplifier gain and minimum operation threshold for different values of the sensor bias. This measurement confirms that with higher reverse bias voltage the gain increases and lower minimum threshold can be achieved due to the reduced sensor capacitance (resulting from the larger depletion of the deep n-type implant around the collection electrode). For this measurement, both the p-wells and the substrate were biased at the same voltage level, indicated on the horizontal axis.

According to TCAD finite-element simulations, the reverse bias applied to the p-wells is expected to have the largest impact on the sensor performance [7]. In order to confirm this, similar calibration measurements were performed with the p-well bias kept at a fixed value, while the reverse bias at the substrate was scanned. The amplifier gain, measured from the fluorescence of an iron target for different values of the substrate bias, is plotted in Figure 13. For this measurement, performed with a CLICTD sample with continuous n-type implant, the p-wells were constantly biased at −3 V. The gain increase of the amplifier is about 0.6% for a step of −1 V at the substrate bias. This confirms that the substrate bias has a negligible impact on the sensor performance, compared to when the two reverse bias nodes are operated at the same voltage.

G. ToT calibration

A calibration of the Time-over-Threshold measurement with test-pulses was performed for the CLICTD chip. Test pulses of different amplitudes were injected at the CLICTD front-end amplifier, in order to parameterise the relationship between the input signal amplitude and the measured ToT. Figure 14 presents the measured ToT as a function of the injected test-pulse signal. The ToT in this measurement is the mean measured ToT of 40 test-pulses that were injected for each signal

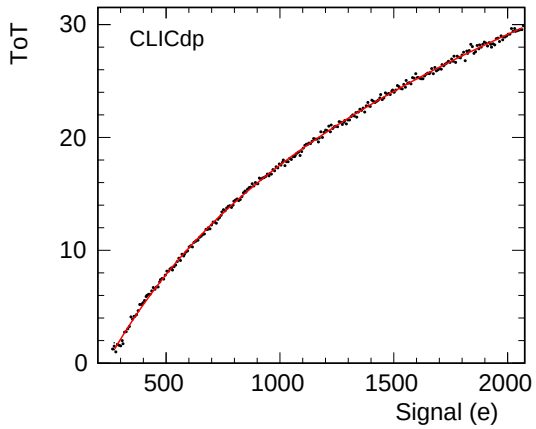


Fig. 14. Measured ToT (in 160 ns bins) as a function of the injected test-pulse signal, for a single sub-pixel in the CLICTD matrix. Fitted with a surrogate function. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V.

amplitude. A surrogate function, described by Equation 1 was fitted to the measured data for each sub-pixel.

$$ToT = ax + b - \frac{c}{x - t} \quad (1)$$

The parameters a, b, c and t are the fit parameters for the function and x is the injected pulse amplitude.

In Figure 15, the value of one of the fit parameters for the surrogate function (parameter b) is plotted across the CLICTD matrix. A pattern that repeats every eight sub-pixels can be observed due to the regular structure of the layout in the CLICTD matrix, similarly to the noise plots in Section III-D.

H. Power consumption

Taking advantage of the low duty cycle of the beam in the CLIC accelerator, introduced in Section I, a power pulsing scheme is implemented for setting parts of the CLICTD circuitry to a low power mode between bunch-trains in order

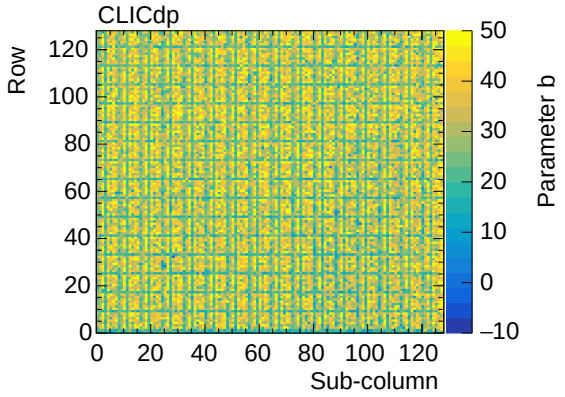


Fig. 15. Parameter b of the surrogate function fit to the measured ToT, plotted across the CLICTD matrix. Sample with continuous n-type implant, with the substrate and p-wells biased to −6 V.

TABLE II: Power consumption of the CLICTD chip.

	Acquisition	Readout[1]	Standby	Average[2]
Analog - matrix [mW/cm^2]	524	2	2	2.8
Analog - periphery [mW]	9	9	9	9
Digital - matrix [mW/cm^2]	279	112	0.6	2.9
Digital - periphery [mW]	40	40	40	40
Total - matrix [mW/cm^2]	803	114	2.6	5.7
Total - periphery [mW]	49	49	49	49

[1] Values extracted from simulations.
[2] Values extrapolated from simulations and static power consumption measurements, averaged assuming a CLIC duty cycle with an acquisition time of 30 µs, a readout time of 340 µs and a standby time of 20 ms.

to minimise the average power consumption. In the analog domain, the main current consuming nodes of the front-end in the sub-pixel (level-shifter, voltage amplifier, discriminator and threshold tuning DAC) are set to standby between subsequent acquisitions. For the digital circuitry, the clock is gated in parts of the logic that only need to be active for short periods of time in order to reduce the number of switching gates. During acquisition, the on-channel state machines enable the clock in the counters only when a hit is detected in the channel. The 100 MHz measurement clock is distributed in the matrix only during the acquisition period. During readout, the 40 MHz readout clock is distributed to only one column at a time, since the data are shifted out on a column-by-column basis.

The CLICTD operation is divided into three distinct phases: acquisition, readout and standby. The measured power consumption for the analog and digital circuitry for each phase, averaged over four measured assemblies, is presented in Table II. For the matrix electronics, the power consumption is noted in mW/cm^2. The CLICTD periphery electronics are continuously powered (no power pulsing is applied) and its power consumption is noted in mW. In view of a future larger version of the CLICTD chip, the periphery is expected to be kept similar in terms of area and power consumption.

For estimating the average power consumption over the CLIC cycle, an acquisition duty cycle of 30 µs/20 ms is assumed. The 30 µs are expected from simulations to be sufficient for the front-end to settle after being set to the nominal power settings for acquisition. The readout time is calculated as the time required for reading out a 1 cm^2 matrix, using a 40 MHz clock and the applied compression algorithm, with an occupancy of 1%. For measuring the power consumption, a current monitoring circuit was connected to the power supplies. However, communication with this circuit is established using the I^{2}C slow control interface, which only allows for static measurements and is not sufficiently fast to measure the power consumption during the short time that the CLICTD readout is active. The values presented for the readout power in Table II are therefore extracted from simulations. The numbers presented for the average power consumption, after power pulsing, are extrapolated from simulated values and static measurements, using the aforementioned acquisition and readout times. Based on this measurement, the average power consumption over the CLIC cycle is expected to be dominated by the power consumption during the standby time. The value for the average power consumption is well within the detector requirements.

I. Detection of minimum ionising particles

First results from measurements in test-beams have been presented in [17]. Preliminary analysis of the acquired data shows a performance close to the requirements for the CLIC silicon tracker. The full analysis is still ongoing.

IV. Summary and Outlook

The main design aspects and characterisation results of the CLIC Tracker Detector (CLICTD) chip have been presented. Slight variations have been observed within the eight sub-pixels in an elongated channel. Based on the measurement results so far, there is no indication of significant impact of these variations on the overall chip performance. Results from three samples of the CLICTD chip show a minimum threshold between 135 and 180 e$^-$ and a noise of about 14 e$^-$ RMS. Based on static power measurements, the expected power consumption, averaged over the cycle of the CLIC beam, is 5.7 mW/cm^2 for the sensitive area, plus about 50 mW for the periphery electronics.

Future studies will focus on a detailed comparison of the charge collection properties and the tracking performance of the two process variants, including test-beam measurements with inclined tracks and for samples thinned to 40 – 100 µm total thickness.

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