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First test results of the CHIPIX65 asynchronous front-end connected to a 3D sensor

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Abstract

This work reports on the main results from the experimental characterization of the asynchronous analog front-end integrated in a 65 nm CMOS mixed-signal chip for the readout of high granularity silicon pixel sensors at the high-luminosity upgrades of the ATLAS and CMS experiments. Such a mixed-signal chip has been designed and submitted in the framework of the CHIPIX65 project, funded by the Italian Institute of Nuclear Physics for the development of an advanced pixel chip in a 65 nm CMOS technology. The project fits the program of the RD53 Collaboration, whose efforts led to the submission, in August 2017, of the large scale chip RD53A, integrating, among three different front-ends, an improved version of the analog processor discussed in this work. The main performance parameters of the asynchronous analog front-end, bump-bonded to a 3D sensor developed by FBK, are discussed in this work.

Key words: Front-end electronics, CHIPIX65, Equivalent noise charge, Low threshold, High Luminosity LHC

1. Introduction

The next generation of readout chips at the High-Luminosity LHC (HL-LHC) will be designed for very intense levels of radiation and particle rates. The experiment upgrades will need new tracker detectors complying with demanding operating conditions. The 65 nm CMOS technology has been chosen by the designer community as the candidate process for the development of pixel readout chips at the HL-LHC. Such a technology enables the integration of very dense in-pixel analog and digital functions, crucial when operating with hit rates of the order of some GHz/cm^2.

A low noise, asynchronous front-end has been designed and integrated in a small scale demonstrator, called CHIPIX65-FE0 [1], also integrating a synchronous architecture, in the framework of the CHIPIX65 project, funded by the Italian Institute of Nuclear Physics (INFN). The demonstrator has been bump-bonded at SLAC with 3D pixel sensors developed by Fondazione Bruno Kessler (FBK). In this work, the design and experimental characterization of the asynchronous architecture is reported.

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CHIPIX65-FE0 features a 64 $\times$ 64 pixel matrix, with 50 μm $\times$ 50 μm pitch, integrating two different analog front-end architectures, based on synchronous [2] and asynchronous [3] hit discriminators. The synchronous and asynchronous submatrices work in parallel and interface to common digital readout and configuration circuits. The demonstrator also includes on-chip bias networks and monitoring and can be configured through an SPI protocol. As far as the design flow is concerned, a digital-on-top approach has been used for the chip assembly, with 16 $\times$ 16 pixels regions making up the pixel matrix.

2. The asynchronous analog front-end

The asynchronous analog front-end integrated in the CHIPIX65-FE0 chip includes a charge sensitive amplifier (CSA) featuring a Krummenacher [4] feedback providing a linear discharge of the feedback capacitance and compensating for the detector leakage current. The CSA has been previously integrated in standalone structures that have been thoroughly tested, also after irradiation, as reported in [5]. A high-speed, low power comparator is DC coupled to the CSA. The discriminator, combined with a 5-bit, dual edge time-over-threshold (ToT) counter clocked at 40 MHz, is exploited for ToT charge conversion. Channel to channel dispersion of the threshold is

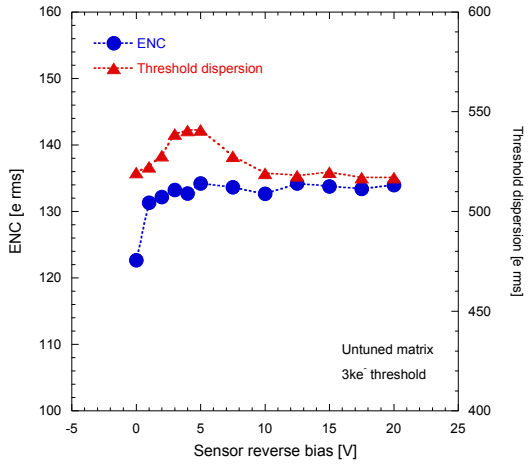

Figure 1: Equivalent noise charge and threshold dispersion as a function of sensor reverse bias voltage. Data obtained for the untuned matrix with 3000 electrons threshold.

addressed by means of an in-pixel trimming DAC featuring a 4-bit binary weighted architecture. At the CSA input an octagonal pad, inscribed in a 16 μm side square, has been designed in the top metal layer enabling sensor bump-bonding.

3. Test results for the bump-bonded chip

A number of CHIPIX65-FE0 chips have been bump-bonded to 3D pixel sensors developed by FBK. Sample prototypes have been coupled to both 50 μm $\times$ 50 μm and 25 μm $\times$ 100 μm sensors at SLAC. Test results shown in this work are relevant to the readout chip connected to the first type of sensors. The main analog front-end features, namely noise, threshold dispersion and time-over-threshold, have been investigated as a function of the sensor reverse bias voltage. Fig. 1 shows results for the equivalent noise charge (ENC) and threshold dispersion for the untuned matrix, with 3000 electrons mean threshold. Except for the data obtained at zero bias, where the ENC is smaller, both the metrics are very slightly affected by sensor reverse bias, with a mean ENC close to 133 e rms and a threshold dispersion before tuning close to 525 e rms. It has to be noticed that the measured ENC is significantly higher with respect to the data obtained for the sensorless front-end [3], due to detector capacitance shunting the preamplifier input. Fig. 2 a) shows the threshold dispersion as a function of the sensor bias in the case of tuned matrix, with a mean threshold set to 600 electrons. Also the tuned threshold dispersion, not exceeding 72 e rms, is not significantly affected by the detector reverse bias voltage. As far as the charge conversion is concerned, Fig. 2 b) shows the mean ToT for an input charge of 6000 electrons with a tuned threshold of 600 electrons.

4. Conclusions

First test results of the CHIPIX65-FE0 asynchronous front-end connected to a 3D sensor have been reported. The main

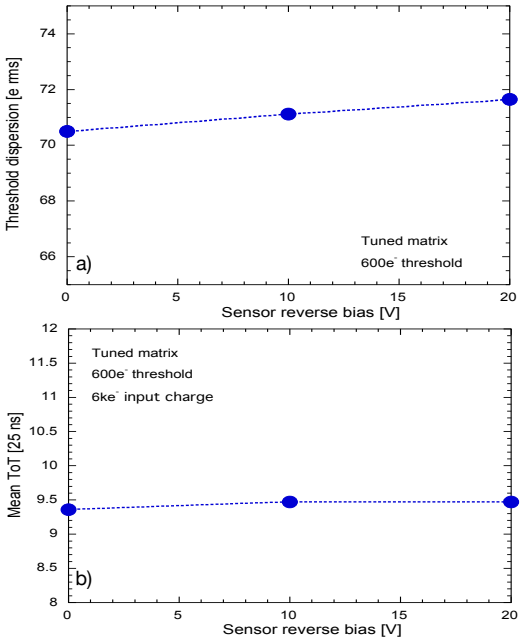

Figure 2: Threshold dispersion a) and Time-over-Threshold b) as a function of sensor reverse bias voltage. Data obtained for the tuned matrix with 600 electrons threshold.

front-end performance parameters have been evaluated for a 50 μm $\times$ 50 μm sensor, developed by FBK, bump-bonded to the readout chip. All the investigated features, such as noise, threshold dispersion and time-over-threshold, are not significantly affected by the sensor reverse bias voltage. The readout chip can be properly operated at 600 electrons threshold, with an equivalent noise charge close to 130 e rms and a threshold dispersion close to 70 e rms, obtained for the maximum investigated sensor bias voltage.

5. Acknowledgement

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