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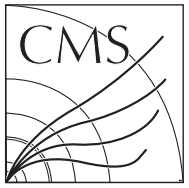

The Compact Muon Solenoid Experiment

Conference Report

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Power hybrids for silicon modules with macro-pixel and strip sensors for the CMS Phase-2 tracker upgrade

Alexander Bogner, Lutz Feld, Waclaw Karpinski, Katja Klein, Martin Lipinski, Irfan Oezen, Alexander Pauls, Gerd Pierschel, Marius Preuten and Michael Wlochal on behalf of the CMS Tracker Group

Abstract

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Presented at *TWEPP2019 Topical Workshop on Electronics for Particle Physics*

PROCEEDINGS OF SCIENCE

Power hybrids for silicon modules with macro-pixel and strip sensors for the CMS Phase-2 tracker upgrade

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1. Introduction

In view of the upgrade of the LHC to the High Luminosity LHC (HL-LHC), the silicon tracker of the CMS detector will be replaced in Long Shutdown 3 with a new and improved device [1]. The new silicon tracker is split into the Inner Tracker or pixel detector, and the Outer Tracker (OT), which features about 13000 silicon modules of two different types, with strip or macro-pixel sensors. The design goals include improved radiation tolerance and higher bandwidth and rate capabilities, to cope with the expected increases in integrated and instantaneous luminosity, higher granularity, and the ability to contribute tracking information to the first trigger level.
The development described in this paper targets one of the OT module types, the Pixel-Strip (PS) module (Fig. 1, left). The module features two silicon sensors on top of each other, with a distance of 1.6-4.0 mm. In the top sensor the cell size is 2.4 cm $\times$ 100 μm, and the strips are read out via wire bonds by Short Strip ASICs (SSAs). The lower sensor is made of 1.5 mm $\times$ 100 μm large macro-pixels, and is bump-bonded to the Macro-Pixel ASICs (MPAs). The SSAs are mounted on folded flexible front-end hybrids (FEHs) at the left and right of the module, together with a concentrator chip, the Concentrator Integrated Circuit (CIC). The strip data are routed from the SSA to the MPA and back to the CIC. From the CIC data are passed to another hybrid, named the readout hybrid (ROH). It carries the Low power Gigabit Transceiver (LpGBT) for data serialization, and the Versatile Transceiver VTRx+ module for opto-electrical conversion. All components are powered from the power hybrid (POH), which carries three DC-DC converters.
A first prototype of the POH has been designed, produced, and characterized.

2. Powering scheme

The PS module requires three power rails, namely 2.5 V for the VTRx+, 1.25 V for the VTRx+, the LpGBT, the analogue domains and I/O parts of the SSAs and MPAs, and the periphery of the CICs, and 1.0 V for the digital domains of the SSAs and MPAs, and the CIC cores. The total power consumption of one module, including inefficiencies of the DC-DC converters, is about 8 W.
The powering scheme is based on DC-DC conversion, where DC-DC converters are used to convert a "high" input voltage, in our case 8-11 V, to a lower output voltage, as required by the consumer. The motivation is that currents on the input are reduced by the conversion ratio, r, of 8-10, reducing in turn voltage drops and Ohmic losses on the supply lines by r and r^2, respectively.

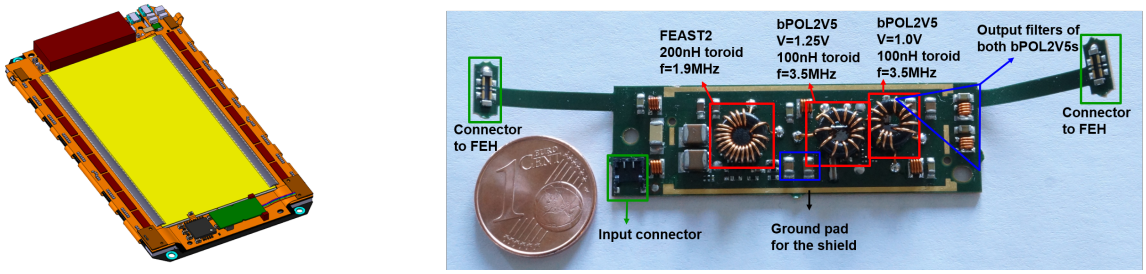

Figure 1: Left: CAD drawing of a PS module, showing the top sensor (yellow), the two front-end hybrids, the readout hybrid towards the front and the power hybrid towards the back. The sensors are 5 cm $\times$ 10 cm in size. Right: photograph of the POH prototype. The shield is not mounted.

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The three required voltages are provided using a two-step scheme, with two DC-DC converters operated in parallel in the second stage. Radiation-tolerant DC-DC buck converters developed by CERN are used. The bPOL12V represents the first stage, delivering about 120 mA at 2.5 V to the VTRx+, and feeding the two bPOL2V5 DC-DC converters [2] in the second stage, which deliver each about 2 A, at 1.0 V and 1.25 V, respectively, to the other consumers on the module.
The power supplies will be located in the experimental cavern, and be connected via cables of about 65 m length to about 12 modules each. Remote sensing is not foreseen, and voltage drops of 2-3 V are expected between the power supplies and the OT modules.

3. The power hybrid

3.1 Design

The POH prototype (Fig. 1, right) is a flexible PCB with four layers of nominally 15 μm thick copper layers and copper-filled stacked micro-vias. Instead of the bPOL12V its predecessor, the FEAST2 ASIC [3], is used, while prototype bPOL2V5 converters are used in the second stage. The air-core inductors are custom toroids with inductances of 200 nH and 100 nH for the FEAST2 and bPOL2V5, respectively, and the switching frequencies are set to 1.9 MHz and 3.5 MHz. Input and output filters in pi-topology are used to filter noise. Flexible tails are needed to connect to the FEHs by folding around the outer module edge (Fig. 1). All voltages are provided to both sides. The input voltage and the status signal of the FEAST2 are also routed to the connector. In the PS module the ROH will receive all voltages and signals via the FEHs, for monitoring by the LpGBT. All CERN DC-DC converters are specified for output currents of 3 A. They feature a soft-start, several protection features, output a status signal, and can be enabled from remote. While the FEAST and bPOL12V are packaged, the bPOL2V5 is mounted via bump-bonding as bare die, with 300 μm pitch, to increase long-term reliability (by reduction of inductance).
The prototypes allow us to gain experience with the bPOL2V5 and, in particular, with the two-stage powering scheme with parallel operation of two DC-DC converters in the second stage, and to support PS module prototyping.

3.2 Dynamical behaviour

The dynamical behaviour during switching on, switching off, and large load changes has been studied, in order to check e.g. for transients or oscillations. A prototype power supply is connected via a 60 m long prototype supply cable and an adapter, which allows us to access the various lines, to the POH. A custom active load is used to draw configurable currents from the POH. The switch-on measurement is shown in Fig. 2, left. Realistic loads were drawn on both sides (50 mA on 2.5 V, 1.2 A on 1.25 V, 0.8 A on 1.0 V, per side). The DC-DC converters are enabled via a voltage divider and lowpass filter from their respective input voltage. The FEAST2 starts up when its enable signal reaches the threshold of about 0.85 V, and the bPOL2V5s are enabled for a FEAST2 output voltage of about 2 V. A clean startup of all three DC-DC converters is observed. The small overshoots at the end of the voltage ramp are expected due to the behaviour of the chips [2]. During switch-off (Fig. 2, right) we observe a staged turn-off (FEAST2 first), as expected. No voltage spikes are seen. In addition, tests were made where the full load was removed or applied to the powered POH (not shown). Again, no adverse effects were revealed.

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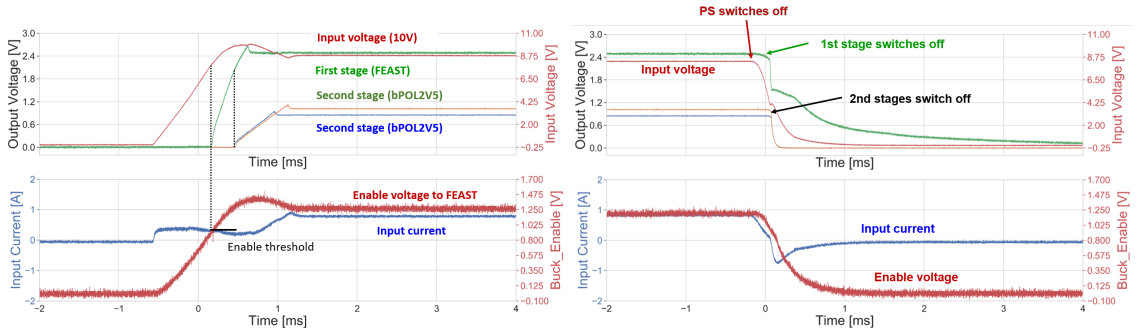

Figure 2: Oscilloscope measurements of the switch-on (left) and switch-off (right) phases. The upper panels show input and output voltages, the lower ones shows the FEAST2 enable voltage and the input current. Non-zero input currents before the enabling of the FEAST chip (left), as well as negative currents after disabling (right), are caused by charging, respectively discharging, of the input capacitors.

3.3 Voltage drops

Voltage drops across the board should be as low as possible, in order to deliver the output voltages within the specification of typically $\pm 10\,\%$ to the powered ASICs, under all load conditions. The voltage drops have been measured for all rails, with the aforementioned loads, across the output pi-filters and from the pi-filter towards the connectors. While the total drops for the 2.5 V rail are with about 60 mV acceptable, those of the other rails range between 90 mV (1.0 V left) to 215 mV (1.25 V right). With 40-60 mV lost across the pi-filter, the path towards the connector is the dominating source. One reason is that the copper layer thicknesses of 8-14 μm are smaller than specified, due to manufacturing problems. The voltage drops have been confirmed with simulations that use the real thicknesses. As a counter-measure for these prototypes we have studied to move the sense point of the DC-DC converters' feedback loops towards the connector. This is very promising, as the dynamical behaviour remains almost unchanged and no instabilities are observed.

It should be noted that voltage drops will also be present on the FEHs, and are in particular relevant for the supply voltages that are passed through the FEHs to the ROH. While the discussion of these drops is beyond the scope of this paper, a viable voltage distribution scheme must of course take all voltage drops into account.

3.4 Power efficiency

The power efficiency is another important parameter, as it influences the total power to be delivered to the front-end, and the local heat load on the module. We have concentrated on the bPOL2V5 efficiencies. Efficiencies on both rails were measured as a function of load. During each measurement, the other two DC-DC converters were effectively removed from the PCB. The efficiency was determined by measuring at the filter capacitors closest to the chip, with toroids and commercial solenoids (used in the measurement reported in the chip data sheet), as well as by measuring the output voltage at the output connector (i.e. including the voltage drops). With solenoids (toroids) the efficiencies are 82.3 % and 86.3 % (80.4 % and 83.2 %) for 1.0 V and 1.25 V, respectively. Measuring at the connector, the efficiencies with toroids decrease (as expected), to

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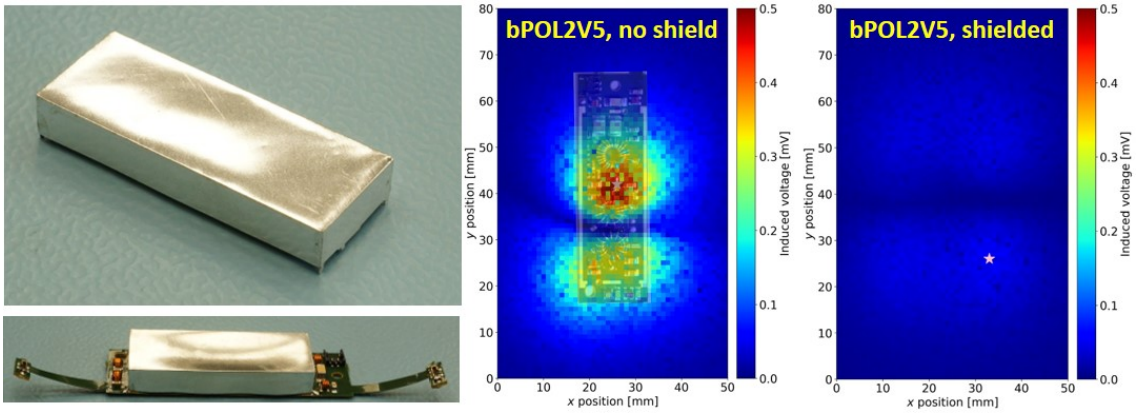

Figure 3: The shield and a shielded POH (left), and scans of the bPOL2V5 emissions at 3.5 ± 0.1 MHz without (center) and with (right) shield.

75.4 % and 77.8 %, respectively.
The total board efficiency has also been measured, using realistic loads and adding up all output powers (three rails, both sides). The efficiency amounts to 54.3 %. This is about 10 % points less than the expectation of 75 % (bPOL12V) $\times$ 85 % (bPOL2V5) $\approx$ 64 %. The difference can be explained by the reduction of efficiency due to the different inductors and due to the voltage drops.

3.5 Shielding and radiated and conducted noise emissions

It is important to shield the electromagnetic emissions radiated from the DC-DC converters' air core coils. A shield prototype has been developed that is made from a 127 μm thin etched aluminium foil, folded into a box-shape (Fig. 3, left). The output pi-filters are outside the shield and thus protected from the emissions. The performance of the shield has been studied by scanning the magnetic field above the DC-DC converters. The emissions are measured as an induced voltage in a pickup probe mounted in a scan table, and at any position the biggest peak within a frequency band is recorded with a spectrum analyzer. Figure 3 shows that the shield is very effective, reducing the induced voltage in the bPOL2V5 frequency band by a factor of about five. This applies also for the FEAST2 emissions, which are however larger by a factor of 3-4 than those of the bPOL2V5s.
Conducted noise has also been studied. Noise spectra in differential and common mode were measured at the input and output. The spectra are dominated by peaks originating from FEAST2, and are comparable to those of a previous board that worked well with silicon strip modules [1].

4. Conclusions and outlook

A prototype of the PS power hybrid has been developed and characterized. The performance is satisfactory except that the voltage drops must be reduced in future versions. Further studies will include measurements with more final cables and power supplies, and optimization of the thermal management. Tests with PS modules will be conducted when such modules are available, and are of utmost importance for evaluation of the module performance when operated with the POH.

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