PROCEEDINGS OF SCIENCE

Caribou — A versatile data acquisition system

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Caribou is a flexible data acquisition system for prototyping silicon pixel detectors. The core of the system consists of the Control and Readout (CaR) board, a versatile module providing the hardware environment for various target ASICs, including powering and slow-control infrastructure, and high-speed full-duplex GTX links up to 12.5 Gbps. The CaR board connects to a Zynq system-on-chip board which runs a fully-featured Yocto-based Linux distribution (Poky) and a data acquisition software (Peary). Using the Caribou system significantly reduces the time required to test and debug detector prototypes by providing ready-to-use peripheries and their software interfaces together with a widely adjustable data acquisition framework that is suitable for a variety of detectors. The paper describes the hardware and software architecture of the system, its capabilities, and examples of projects where it has been used.

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1. Motivation and introduction

Developing new detectors requires the design of an adequate readout and control system. Such a system typically consist of hardware in form of a readout board containing programmable logic to provide an interface to the detector chip, power supplies for biasing the sensor, as well as DACs and ADCs for setting and measuring operation parameters, generating test pulses, etc. One also needs to write software for controlling the detector and hardware peripherals and for data readout. This process needs to be repeated for each new chip developed, which requires different voltage levels or different number of data lines. The Caribou system [1][2], on the other hand, provides a robust, versatile and modular open-source DAQ system, which can be easily adjusted to the needs of different detectors. Figure 1 shows an overview of a complete working setup. Using such a system therefore saves development cost and reduces the time needed to get first data from the detector. Caribou hardware can be also easily reused for another detector after the work on one detector is finished. The system originally targeted pixel detector prototypes for the ATLAS Inner Tracker (ITk) upgrade project and for the future CLIC vertex detector.

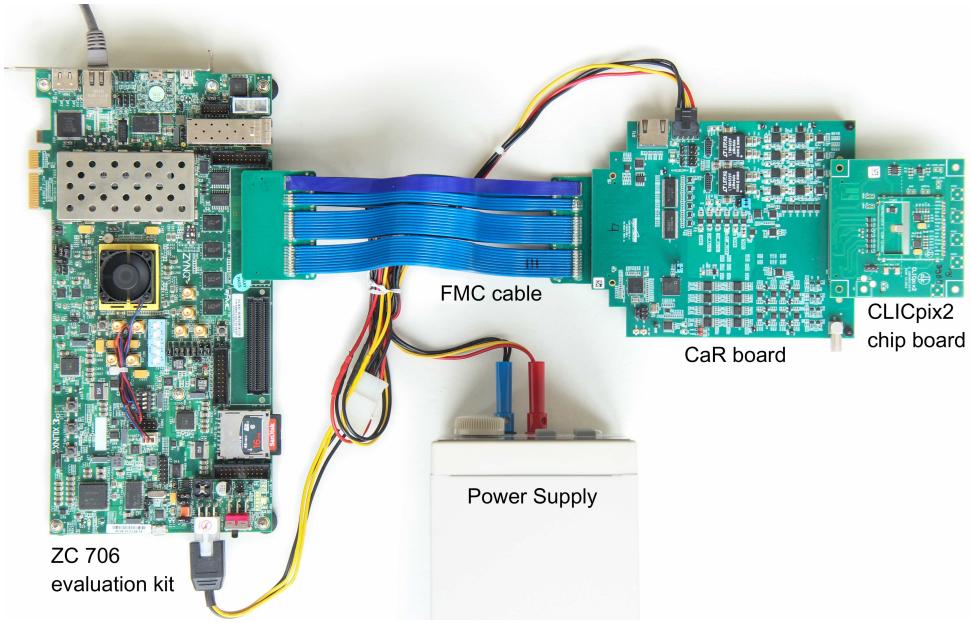

Figure 1: A complete Caribou DAQ setup.

2. Caribou hardware architecture

The hardware architecture of the current Caribou system is based on the Xilinx Zynq System-on-Chip (SoC) platform. The Zynq 7000 series is currently supported and porting to Zynq Ultra-Scale+ is in progress. A range of peripherals, mostly programmable power supplies and voltage references, is connected to the SoC via an I^2C bus. The present version uses a ZC706 evaluation board as a base board. An extension Control and Readout (CaR) board is connected via an FPGA Mezzanine Card (FMC) interface to the evaluation board. The FMC connection to the CaR board

can be extended by a cable. The CaR board contains all peripherals needed to interface and run the chip, namely:

- 8 adjustable power supplies with monitoring
- 8-input 12-bit ADC with 50 kSamples/s (I^2C interface)
- 16-input 14-bit ADC with 65 MSamples/s (parallel interface)
- 4 injection pulsers with adjustable pulse amplitude
- 32 adjustable voltage references
- 8 adjustable current references
- 10 output and 14 input single-ended links with adjustable voltage level
- 17 bidirectional LVDS links (up to 1.1 Gb/s)
- 8 full-duplex high-speed differential links (0.8-12 Gb/s)
- programmable low-jitter clock generator with external reference input
- interface for trigger and time reference (3 LVDS I/O + 1 LVDS clock)

The CaR board has a 320-pin SEARAY connector for interfacing it to a detector-specific chip board carrying the detector, passive components and eventually some detector-specific circuits that are missing on CaR board. Most of active circuits that are typically needed for operating a silicon pixel detector are included in the CaR board. Figure 2 shows a schematic overview of the hardware architecture. The FPGA fabric of the SoC can be used to implement a detector-specific hardware interface to the detector or some provided existing modules can be used. The FPGA registers are connected to the CPU via an AXI bus and are mapped to a memory space of the processor. Thus software can access it easily by reading or writing a corresponding memory address.

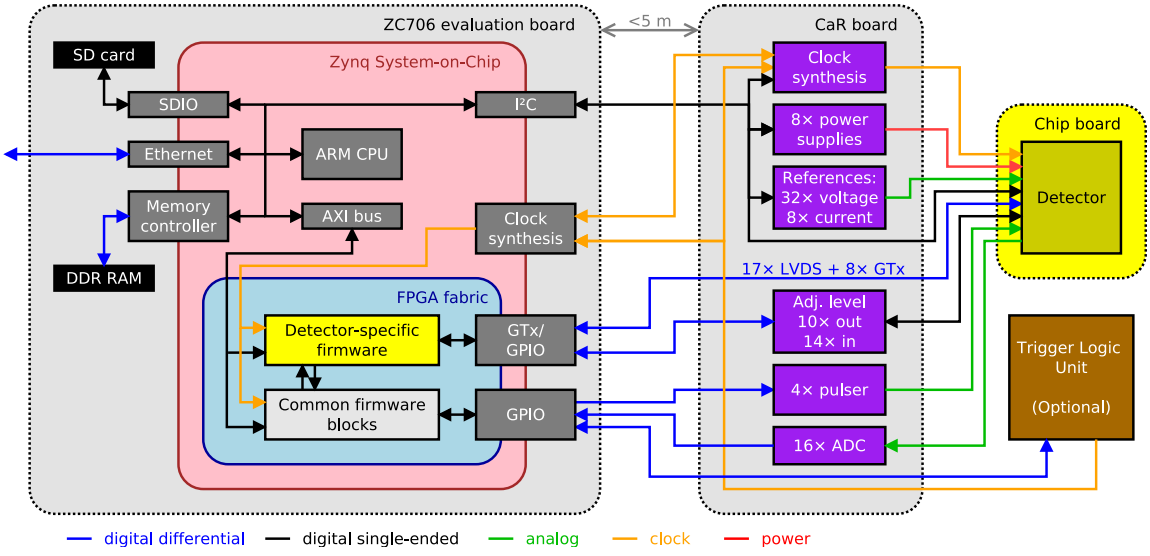

Figure 2: Simplified schematics of the Caribou hardware architecture.

3. Caribou software architecture

The SoC allows to run a fully-featured Linux system with a network connection and all necessary applications. A Yocto and Openembedded-based Linux distribution (Poky) is used to which a

DAQ software called Peary is added. Figure 3 shows an overview of the Peary software layers. The software contains a Hardware Abstraction Layer (HAL) that creates an interface between physical hardware components and software. It allows to handle hardware peripherals as objects in C++. In addition to the HAL, Peary contains templates for creating device-specific functions, a device manager to handle multiple devices at the same time, logging with different verbosity levels, a command line interface (CLI) and application interface (API). The CLI can be also be used for standalone operation, e.g. to do lab measurements. The API can be used to operate the system within a superior DAQ (e.g. as EUDAQ [4] producer). Running a full Linux distribution allows to run user applications and even some data analysis (e.g. in Python) directly on the Caribou machine.

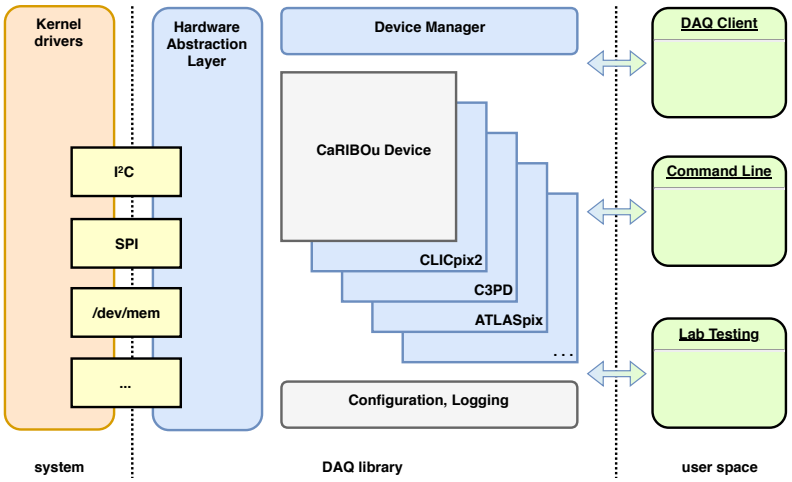

Figure 3: Peary DAQ software architecture.

4. Supported detectors and testbeam integration

Peary and firmware modules as well as Caribou-compatible chipboards are already available for HV-CMOS pixel detector prototypes for ATLAS ITk upgrade [5] (H35Demo/FEI4, ATLASPix, ATLASPix2, ATLASPix3) and for the future CLIC vertex and tracking detector [3] (CLICTD, CLICpix2/C3PD). The Caribou hardware platform (without Peary) has been used for RD50 HV-CMOS prototypes (RD50-MPW1).

A new modular concept of the FPGA firmware was introduced for CLICTD. It is built using independent and widely configurable firmware blocks for each function. Peary software modules for each of the firmware blocks are also provided. The modular approach allows an easy reuse of these block with a minimal programming effort while implementing new detectors that require similar functionality.

An example of such a block is so called Pattern Generator which allows to define states of its outputs in time with a possibility to make transactions between states dependent on trigger inputs. It also allows configurable number of repetitions. The software part in Peary configures the firmware block accordingly to a configuration text file.

Another example is a timestamp generator block, that allows the user to configure a condition of its input signals in Peary software and a timestamp of such event will be stored each time the condition is met.

The Caribou system has been used for operating a Device Under Test (DUT) in the CLICdp Timepix3 beam telescope at the SPS North Area at CERN. There it was synchronised with the Timepix3 using the SPIDR readout and with a custom run control. Caribou has been recently integrated also into a EUDET telescope at the DESY where it was controlled by EUDAQ2 [4]. An EUDAQ2 producer is provided as part of the project, and any detector supported by Caribou and Peary can be operated without further development within the EUDAQ framework.

5. Work in progress and future plans

Porting to the Zynq UltraScale+ architecture has been completed up to the Peary software. The UltraScale+ architecture will allow higher data throughput thanks to a 64-bit 4-core CPU. Implementation of DMA data transfer to the processing system is also planned in order to further increase the data throughput.

6. Summary

Caribou is a compact stand-alone DAQ system framework for detector prototypes. It has been successfully used to characterize silicon pixel detectors for ATLAS ITk upgrade [5] as well as for a future CLIC vertex and tracking detector [3]. The source code of software as well as design files for hardware boards are open-source [6]. The system can be easily adjusted to almost any silicon pixel detector by writing a piece of code performing an interface between the chip-specific features and the standard data and control interface of the Caribou system. The SoC-based architecture combines the power of an FPGA and a full Linux operating system allowing to run software in a high-level programming language. With the new modular approach that was recently introduced also in the FPGA firmware, a lot of firmware code including the corresponding Peary functions can be reused as well.

References

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